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System Design & Test

Architecture Synthesis for Cost Constrained Fault Tolerant Biochips

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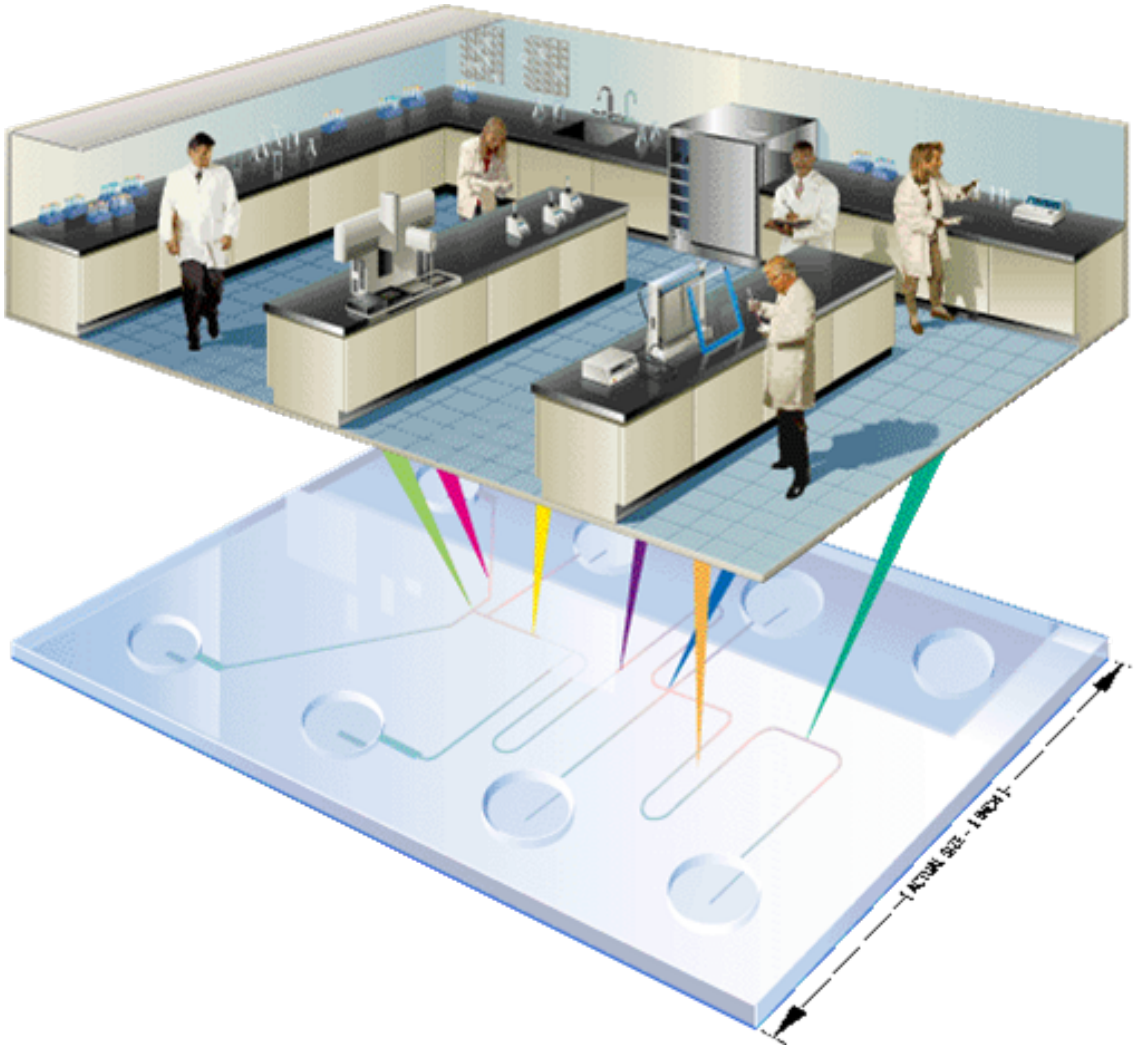
DTU

Outline

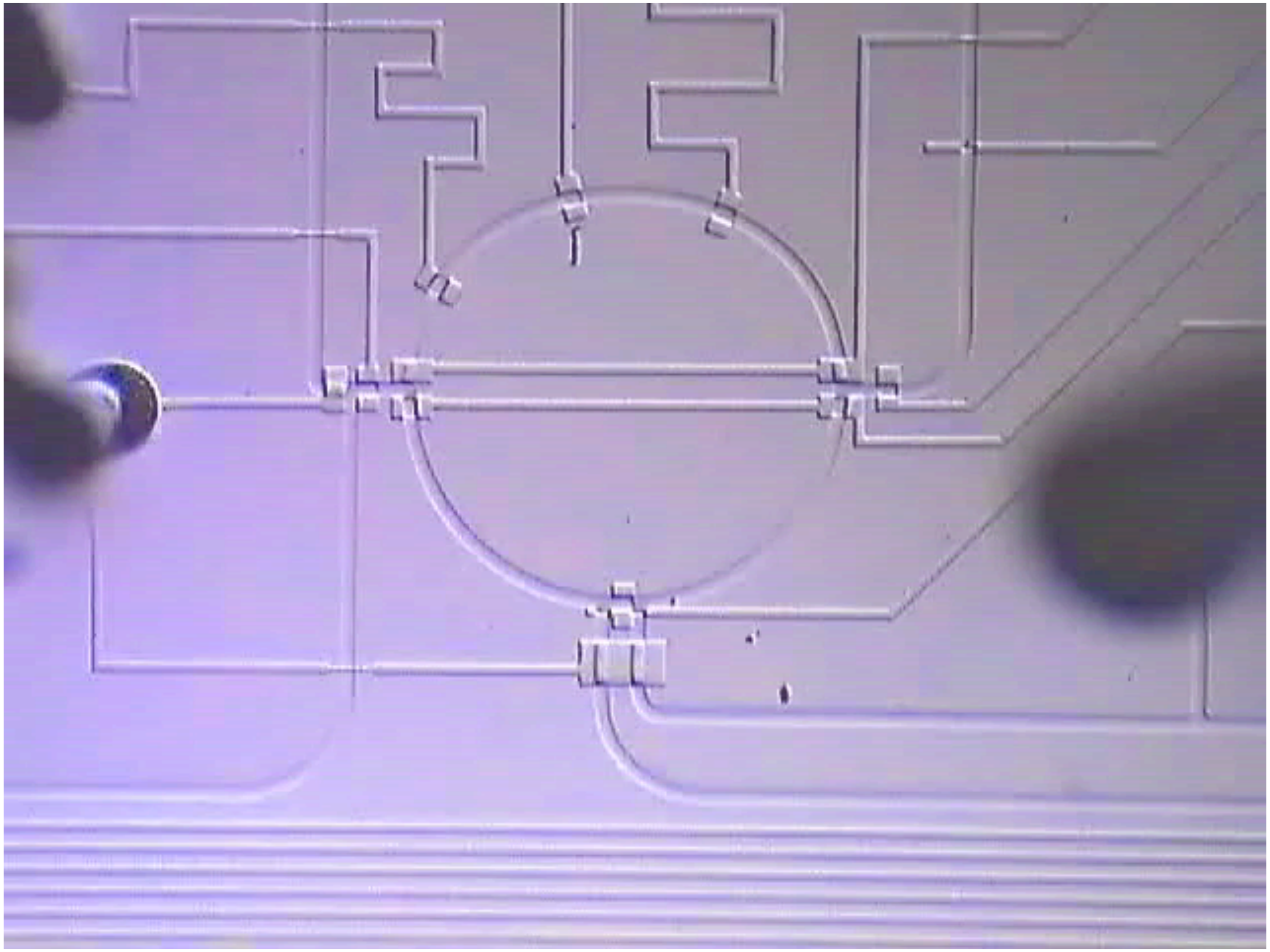
- Introduction to mVLSI
- Flow-based biochips
- Defects and need for reliability
- Fault model and fault tolerant components
- Motivational example
- Problem formulation and objective
- Optimization strategy
- Experimental results
- Conclusions

Introduction to mVLSI



Source: W. Grover, “Designing, fabricating and using flow-based microfluidics: Past successes and future challenges”, Tutorial, VLSI Design 2015

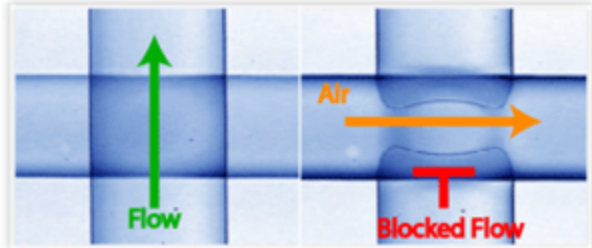
Flow-based (FB) Biochips



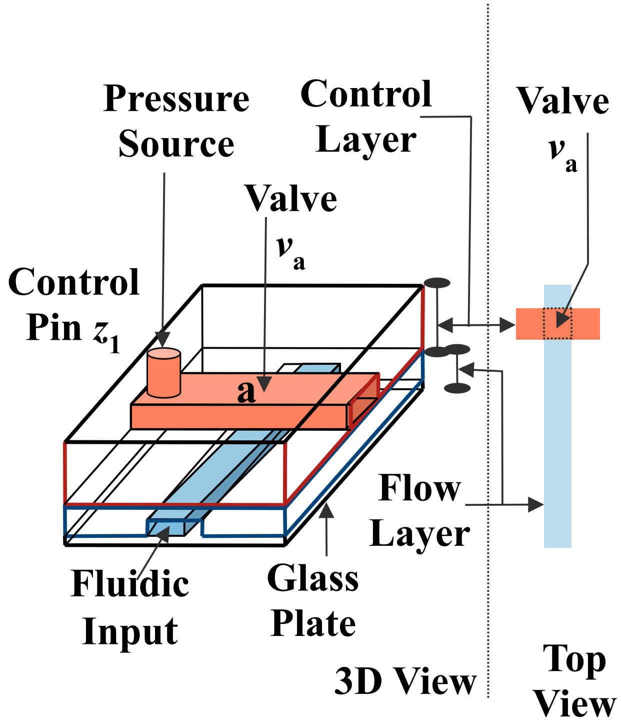
Source: http://groups.csail.mit.edu/cag/biostream/

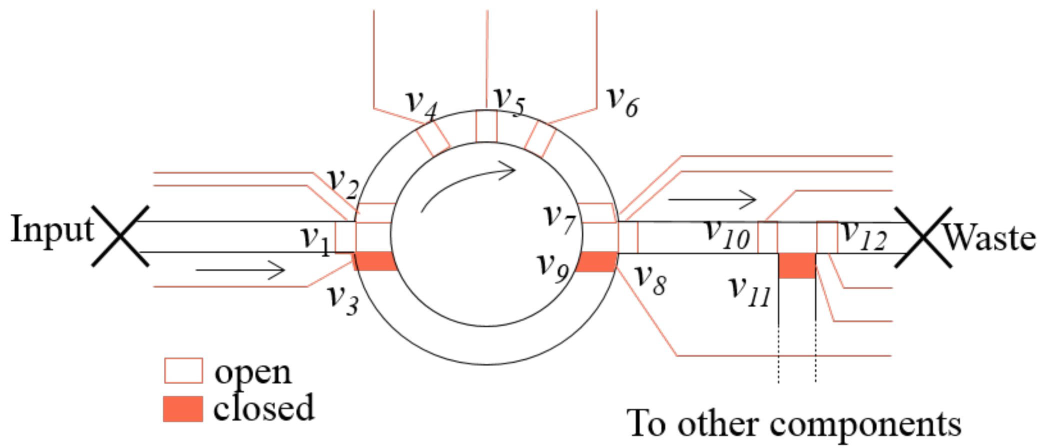
Technology and high level abstraction

- Technology:
  - Multi-layer soft lithography
  - Fabrication substrate – elastomers (PDMS)

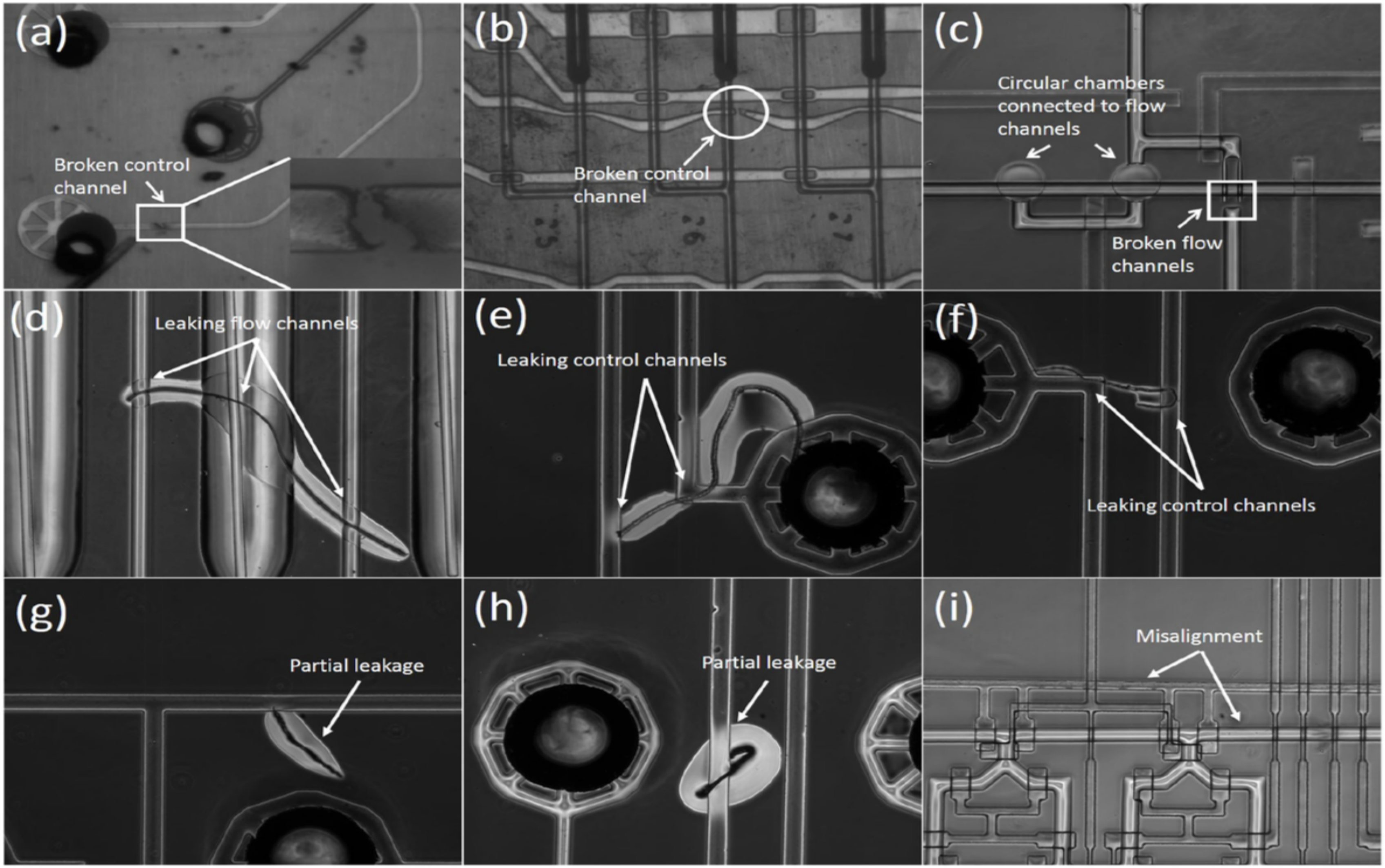


Source: S. R. Quake et al, “From micro- to nanofabrication using soft materials”, Science 2000





Defects in microfabrication of FB biochips



Source: K. Hu et.al, "Testing of Flow-based Microfluidic Biochips: Fault Modeling, Test Generation and Experimental Demonstration", IEEE TCAD, 2014

Need for Reliability

Sensitivity= positivity in disease, expressed as a % = TP/ (TP+FN) × 100

Specificity = absence of a particular disease, expressed as % = TN/ (FP+TN)× 100

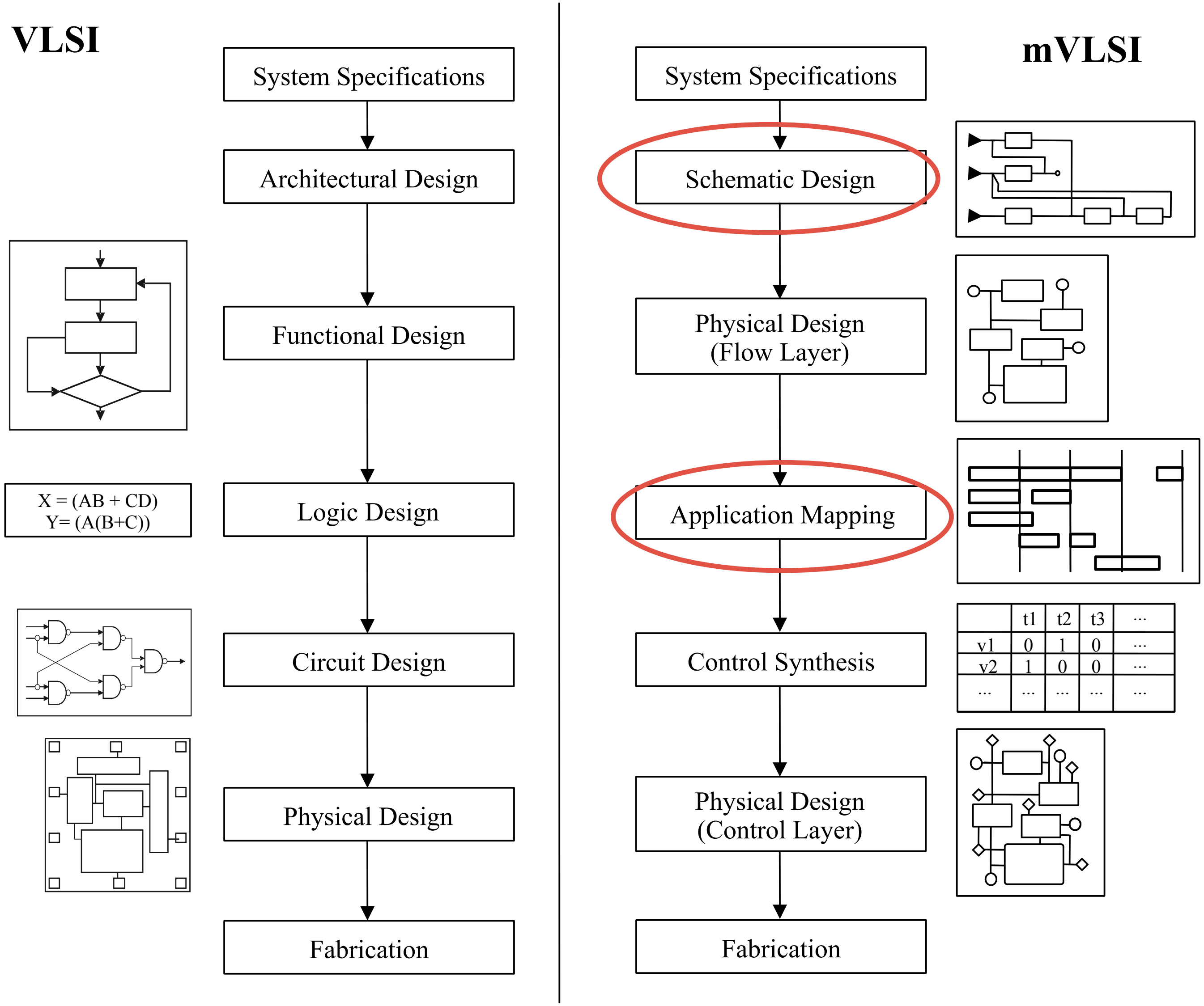
TP = True Positives, the number of diseased patients correctly classified by the test

TN = True Negatives, number of non-diseased patients correctly classified by the test

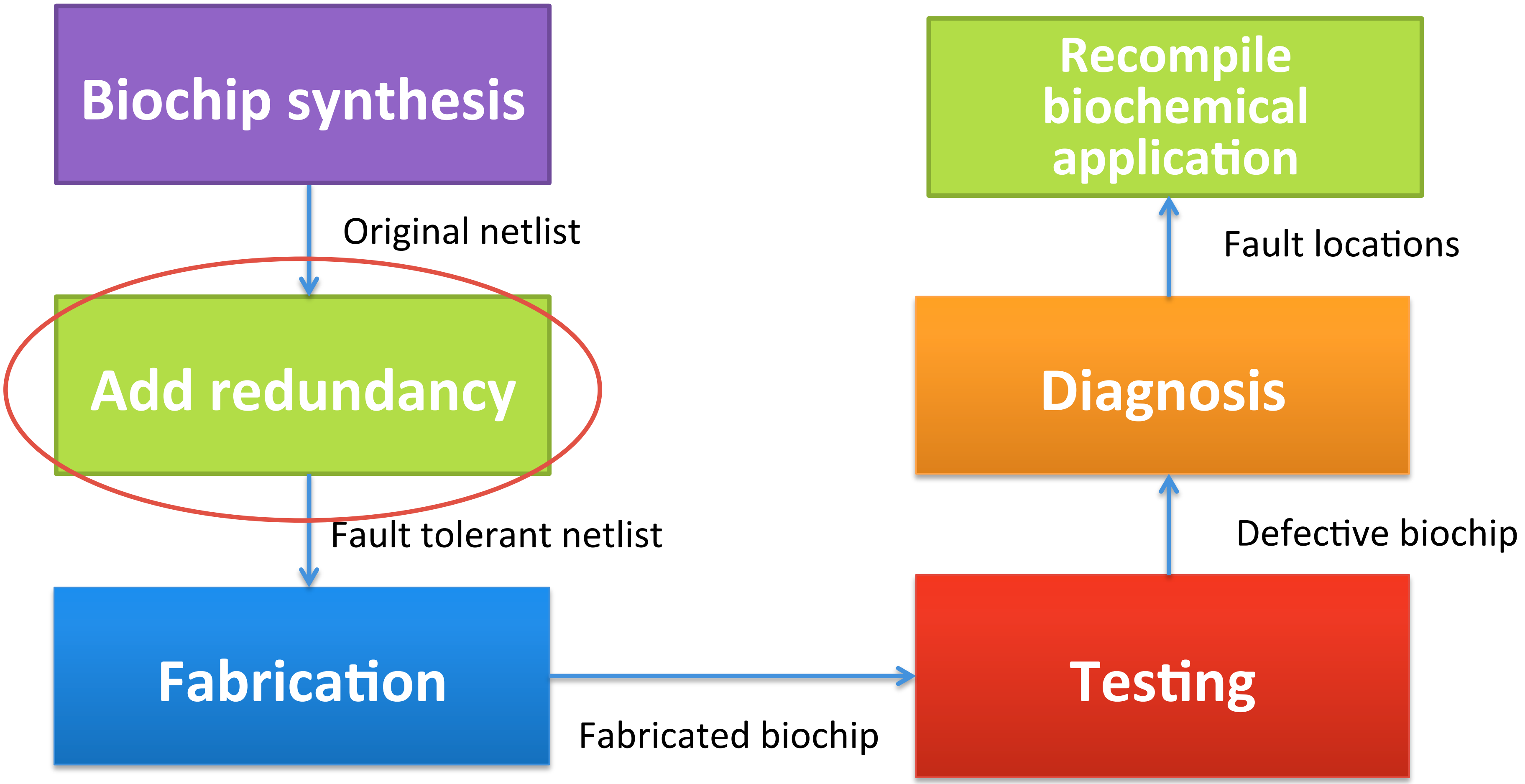
FP = False Positives, the number of non-diseased patients misclassified by the test

FN = False Negatives, the number of diseased patients misclassified by the test

The big picture



The big picture



Fault model

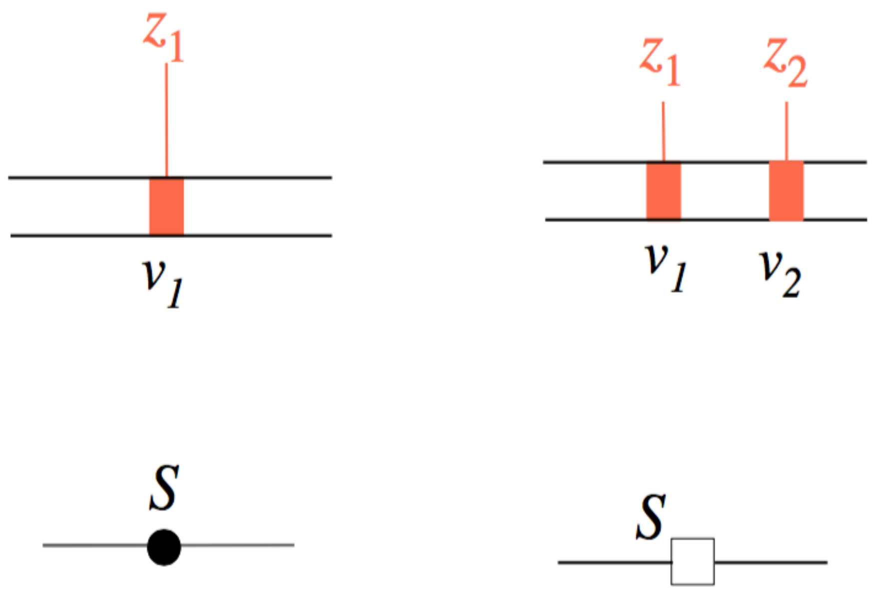
	Flow Layer	Control Layer
Block	Valve is stuck closed	Valve is stuck open
Leak	Fluid flow in one channel contaminates adjacent channels	Control channels of two independent valves are unintentionally connected. Pressure on either valve closes both valves

$$\mathcal{Z} = (\mathcal{VF}, \mathcal{CF}, 2, 2)$$

Name	**Component** $(M \in \mathcal{N}, \notin \mathcal{S})$ / **Connection** $D_{i,j} \in \mathcal{D}$	**Type** (t)
CF_1	$Heater_1$	Block
CF_2	$Filter_1$	Block
CF_3	$S_2 \rightarrow$ Storage-8	Block
CF_4	$S_1 \rightarrow Mixer_1$	Block

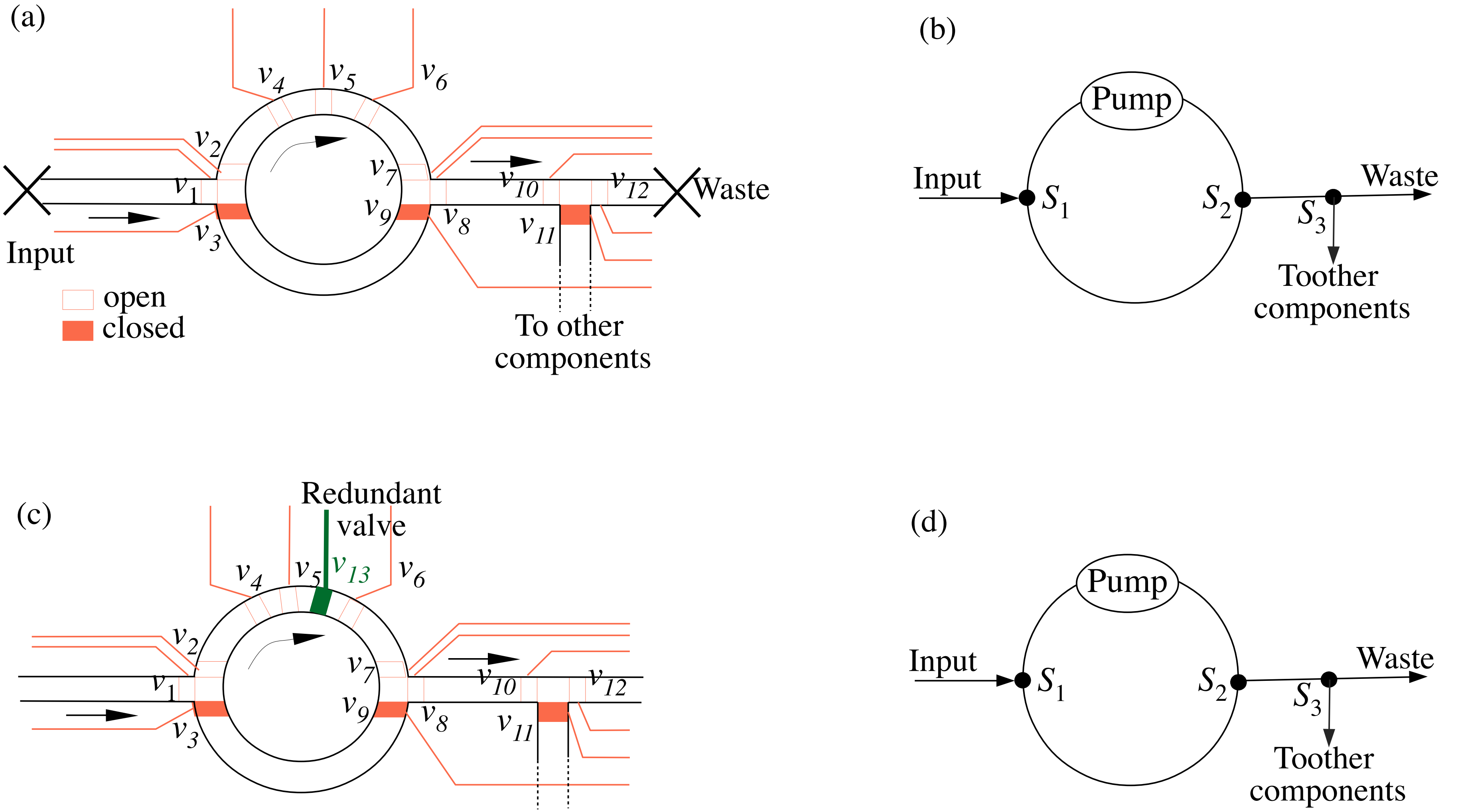
Name	**Vertex** $(N \in \mathcal{N})$	**Valve affected** (w)	**Type** (t)
VF_1	$Mixer_1$	v_5	Open
VF_2	S_6	v_3	Open
VF_3	S_5	v_2	Open
VF_4	S_3	v_3	Open

Fault-tolerant switch design



Cost overhead: 1 extra valve per switch

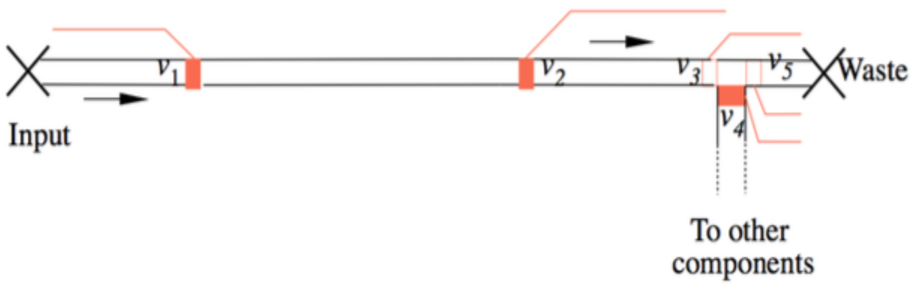
Fault-tolerant pump/mixer design



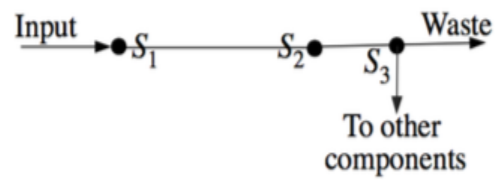
Cost overhead: 1 extra valve per pump

Fault-tolerant channels

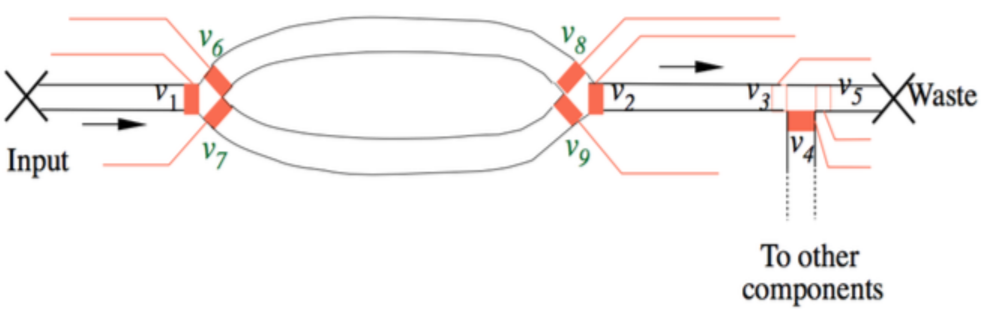
(a) The component



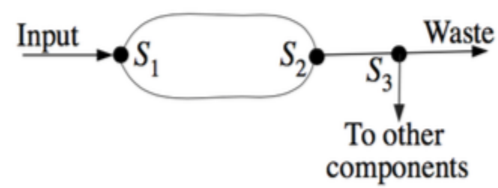
(b) Conceptual view of the component



(c) The fault-tolerant component

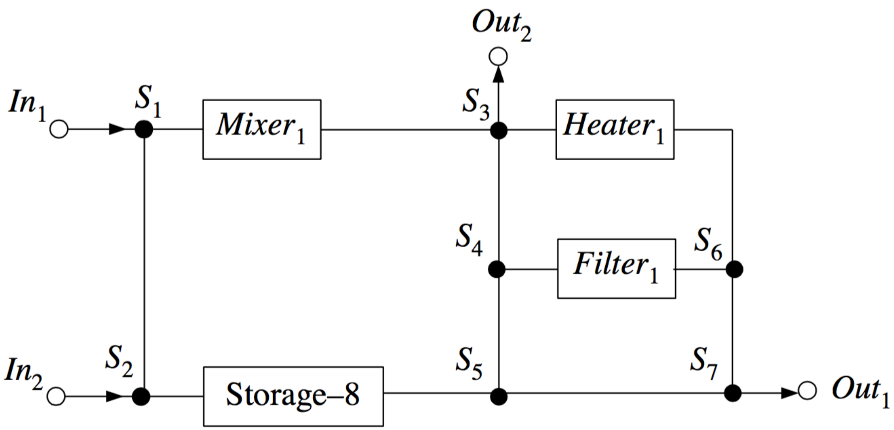


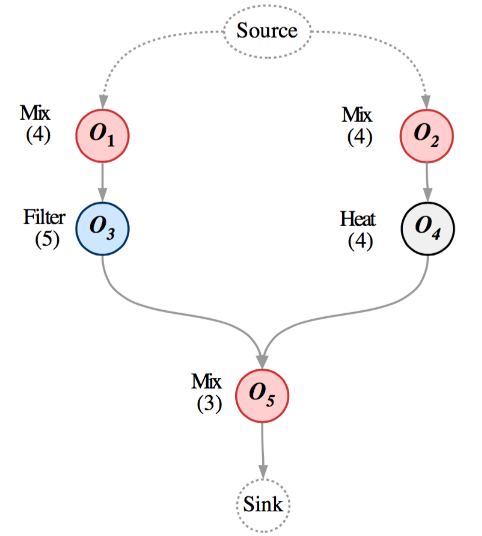
(d) Conceptual view of the fault-tolerant component



Cost overhead: 4 extra valves and 3 extra channels

Motivational example





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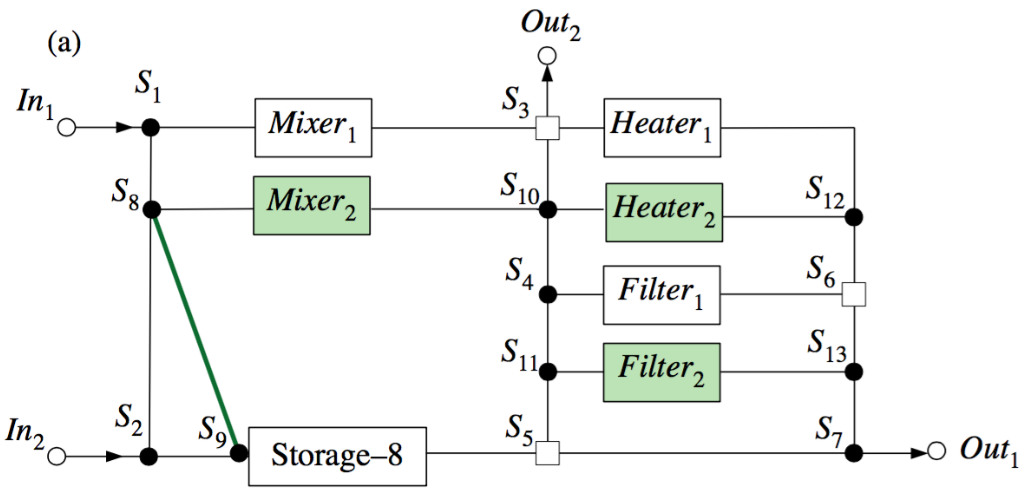
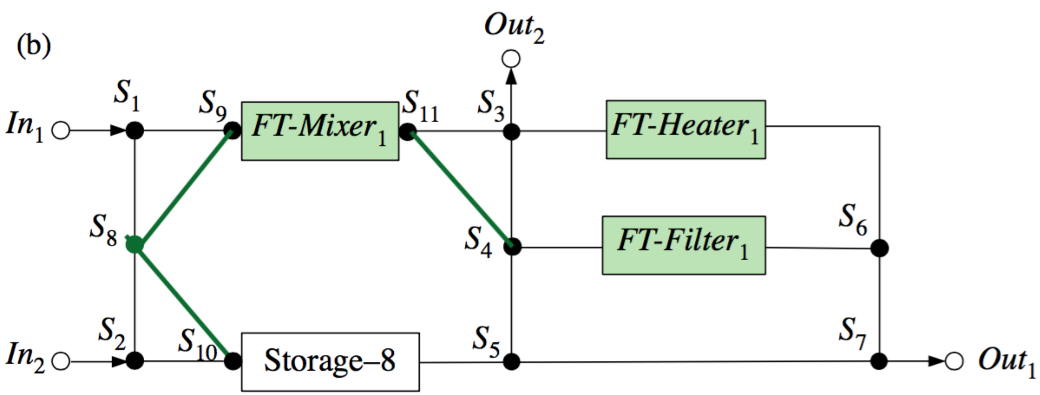
VF_3	S_5	v_2	Open
VF_4	S_3	v_3	Open

Straightforward vs. optimized synthesis



- **Straightforward solution: redundancy not optimized; biochip architecture cost: 129**



- **Optimized solution: optimal addition of redundancy biochip architecture cost: 96**

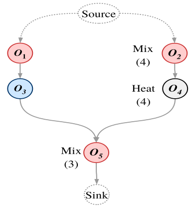
Problem formulation

Fault Tolerant Architecture Synthesis (FTAS)

- **Given**
  - **A biochemical application and a fault model**
  - **Characterized component model library (including fault-tolerant components)**
- **Synthesize**
  - **A biochip architecture**
  - **Deciding on:**
    - **Component allocation**
    - **Fault-tolerant *netlist* generation**
    - **Schedule for routing of fluids through the microfluidic channels**
- **Such that**
  - **the cost of the architecture is minimized**
  - **Satisfying the fault-tolerance, dependency and resource constraints**

Cost = total number of valves + total number of channels in the architecture

Problem formulation



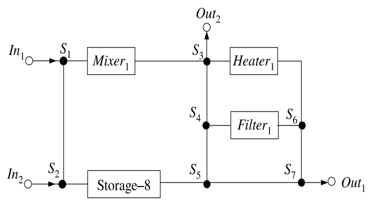
Application model

Component library&
Design constraints

COMPONENT LIBRARY ($\mathcal{L}$): FLOW LAYER MODEL

Component	Phases($\mathcal{P}$)	C	H
Mixer	Ip1 / Ip2 / **Mix** / Op1 / Op2	0.5 s	30 × 30
FT-Mixer	Ip1 / Ip2 / **Mix** / Op1 / Op2	0.5 s	30 × 30
Filter	Ip / **Filter** / Op1 / Op2	20 s	120 × 30
FT-Filter	Ip / **Filter** / Op1 / Op2	20 s	120 × 60
Detector	Ip / **Detect** / Op	5 s	20 × 20
FT-Detector	Ip / **Detect** / Op	5 s	20 × 40
Separator	Ip1 / Ip2 / **Separate** / Op1 / Op2	140 s	70 × 20
FT-Separator	Ip1 / Ip2 / **Separate** / Op1 / Op2	140 s	70 × 40
Heater	Ip / **Heat** / Op	20° C/s	40 × 15
FT-Heater	Ip / **Heat** / Op	20° C/s	40 × 30
Storage	Ip or Op	-	90 × 30
FT-Storage	Ip or Op	-	90 × 40
Metering	Ip / **Met** / Op1 / Op2	-	30 × 15
Multiplexer	Ip or Op	-	30 × 10

Initial architecture



Fault model

Table: The set of valve faults $\mathcal{VF}$

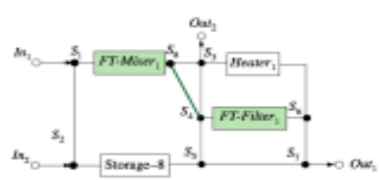
Name	Vertex ($N \in \mathcal{N}$)	Valve affected (w)	Type (t)
VF_1	$Mixer_1$	v_5	Open
VF_2	S_6	v_3	Open
VF_3	S_5	v_2	Open
VF_4	S_3	v_3	Open

Table: The set of channel faults $\mathcal{CF}$

Name	Component ($M \in \mathcal{N}, \notin \mathcal{S}$) / Connection $D_{i,j} \in \mathcal{D}$	Type (t)
CF_1	$Heater_1$	Block
CF_2	$Filter_1$	Block
CF_3	$S_2 \rightarrow$ Storage-8	Block
CF_4	$S_1 \rightarrow Mixer_1$	Block

Fault Tolerant Architecture
Synthesis (FTAS)

Fault tolerant architecture

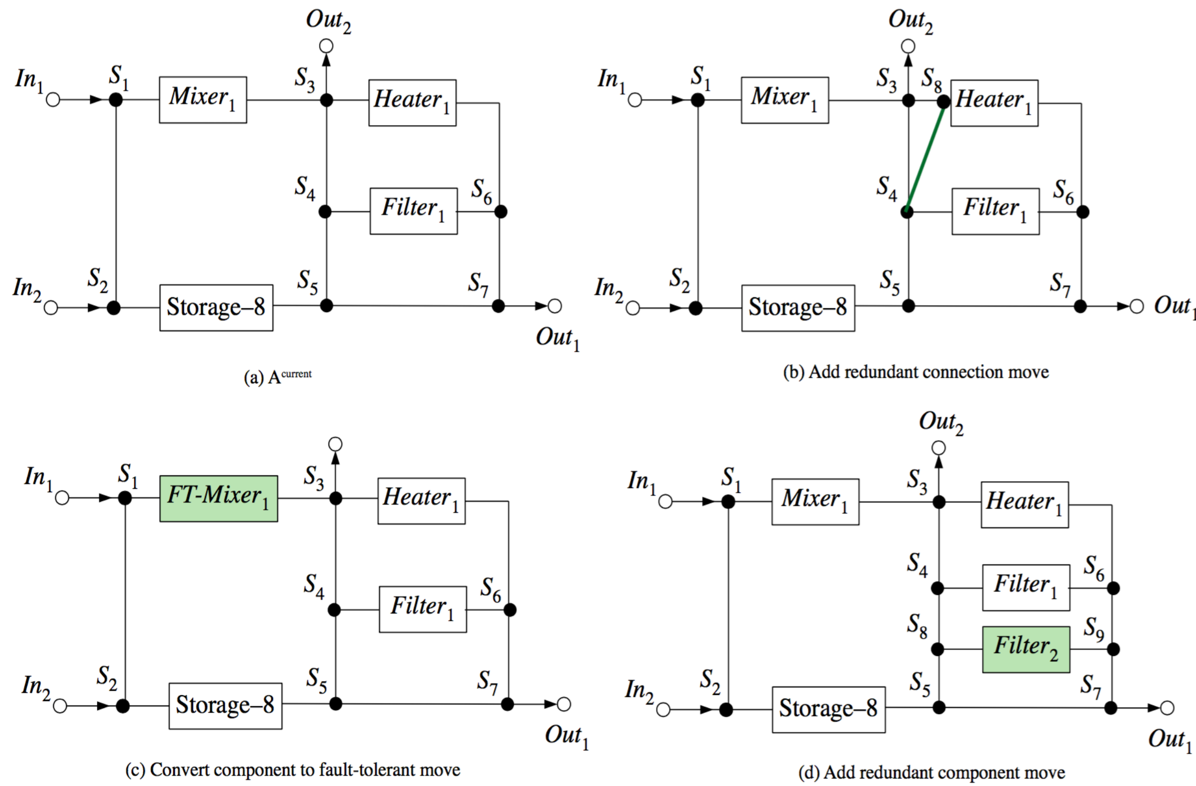


Cost = total number of valves + total number of channels in the architecture

Optimization strategy (FTAS)

Design transformations

- Add redundant component
- Make component fault-tolerant
- Add redundant connection
- Remove redundant component
- Make component non fault-tolerant
- Remove redundant connection



Optimization strategy (FTAS)

- **Metaheuristic optimization**: Greedily Randomized Adaptive Search Procedure (GRASP)
  - Searches the solution space to minimize the objective function

  - Fault scenario generation: subset of all the possible scenarios
    - Each iteration applies design transformations visits a neighboring solution
      - Applies a fault scenario: injects the faults in the scenario

      - Determines connectivity: can I still move fluids around?

      - Finish time of the application: will the application finish correctly?

    - Evaluates them based on the objective, to pick or drop the neighboring solution.

Optimization strategy (FTAS)

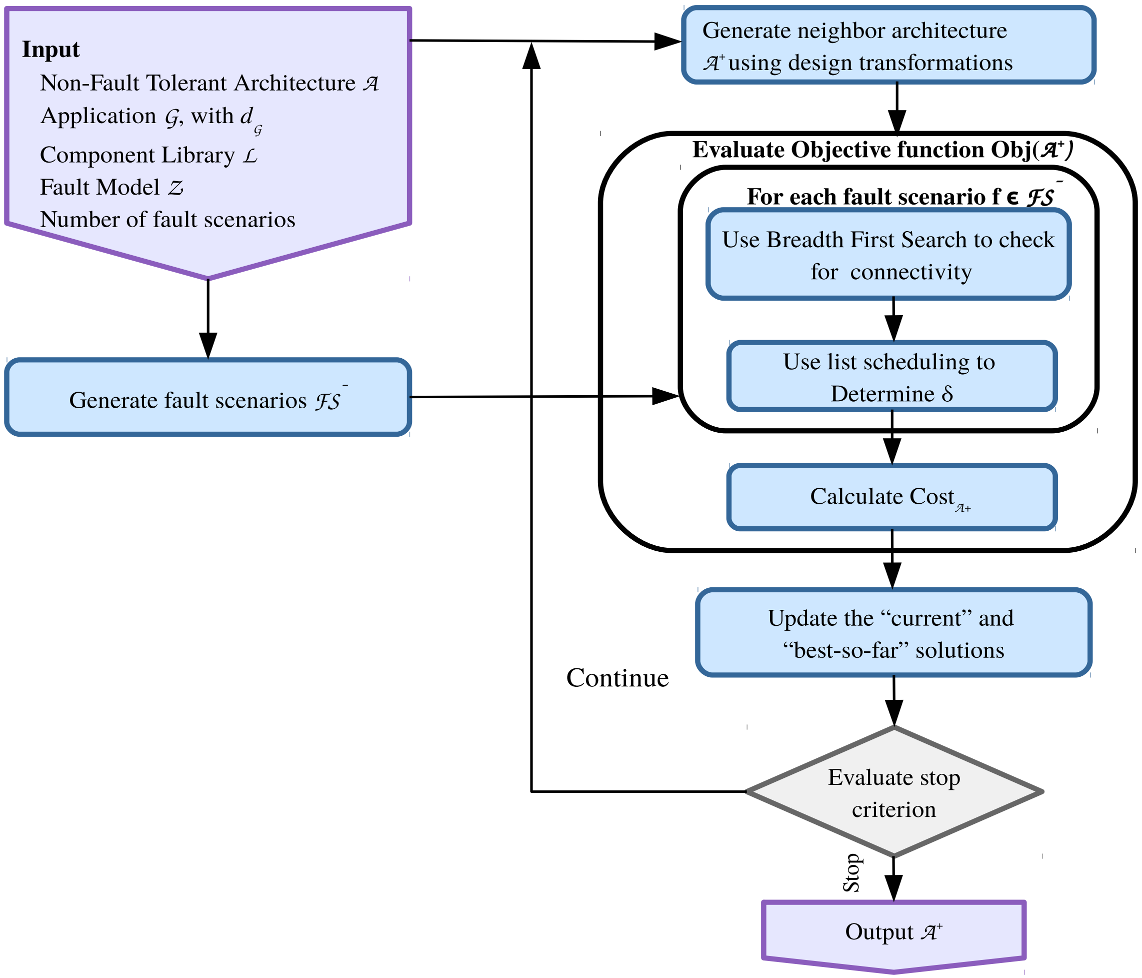
$$Objective(\mathcal{A}) = \left(\sum_{f \in \mathcal{FS}}^{\mathcal{FS}} \neg ft\right) \times W_{ft} + \left(\sum_{f \in \mathcal{FS}}^{\mathcal{FS}} max(0, \delta - d_{\mathcal{G}})\right) \times W_s + Cost_{\mathcal{A}}$$

- Connectivity
  - 1 if connected, 0 otherwise
  - Determined by Breadth First Search
  - Considers blocked route and valve faults on switches

- Physical constraints
  - Sum of
    - Total number of valves
    - Total number of connections

- Scheduling
  - Maximum of 0 or δ - application deadline
  - Determined by List Scheduling
  - Routes determined by Breadth First Search

Optimization strategy (FTAS)



Experimental Results

A: Original biochip architecture

A_{SFS}^{+} : Biochip architecture obtained using straightforward fault solution

A_{FTAS}^{+}: Biochip architecture obtained using proposed FTAS approach

$\mathcal{N}$: Set of all microfluidic components in the biochip

$\mathcal{D}$: Set of all microfluidic channels in the biochip

Name	A			$\|\mathcal{FS}\|$	$\|\mathcal{FS}^{-}\|$	A_{SFS}^{+}			A_{FTAS}^{+}		
	$\|\mathcal{M}\|$	$\|\mathcal{D}\|$	Cost			$\|\mathcal{M}\|$	$\|\mathcal{D}\|$	Cost	$\|\mathcal{M}\|$	$\|\mathcal{D}\|$	Cost
S-1	15	17	84	121	100	20	27	133	15	20	102
PCR	14	16	88	77	50	18	25	135	14	17	92
IVD	52	78	274	841	100	57	92	379	52	78	279

Yield Results for S-1 benchmark

$\mathcal{FS}$: Exhaustive set of fault scenarios based on the fault model

$\mathcal{FS}^{-}$: Chosen fraction of fault scenarios

$\mathcal{FST}$: Set of fault scenarios tolerated by the architecture

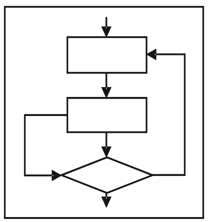
$\lvert\mathcal{FS}^{-}\rvert$	A_{FTAS}^{+}			$\lvert\mathcal{FST}\rvert$	%Yield
25	16	20	98	105	86.8%
50	15	19	99	117	96.7%
121	15	19	102	121	100%

Thank you!

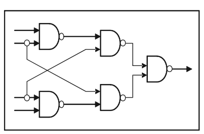
Microfluidic Large Scale Integration

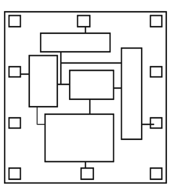
VLSI

1. System Specifications
2. Architectural Design
3. Functional Design
4. Logic Design
5. Circuit Design
6. Physical Design
7. Fabrication



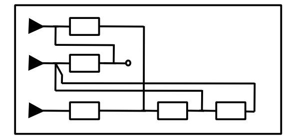
X = (AB + CD)
Y= (A(B+C))

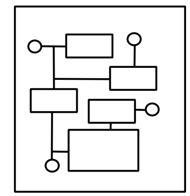


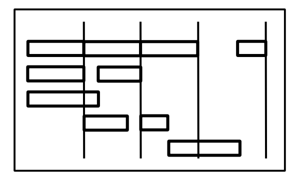


mVLSI

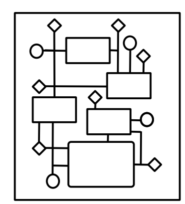
1. System Specifications
2. Schematic Design
3. Physical Design (Flow Layer)
4. Application Mapping
5. Control Synthesis
6. Physical Design (Control Layer)
7. Fabrication







	t1	t2	t3	…
v1	0	1	0	…
v2	1	0	0	…
…	…	…	…	…



Component library

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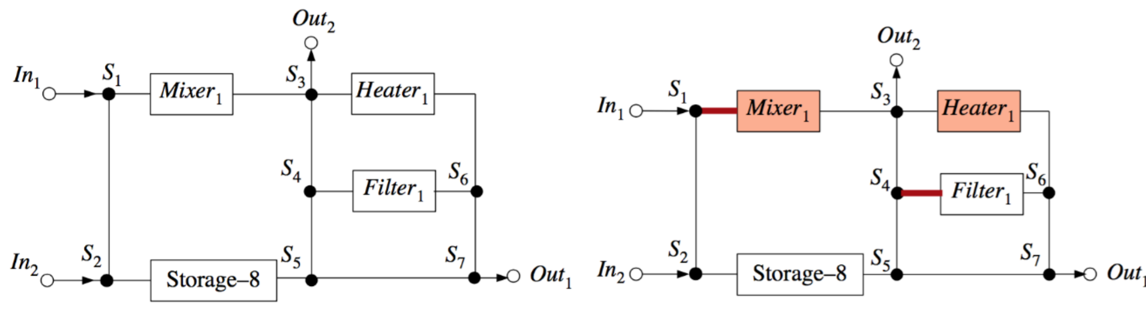
Metering	Ip / **Met** / Op1 / Op2	-	30×15
Multiplexer	Ip or Op	-	30×10

Optimization strategy

- Fault scenario generation
  - Each iteration
    - Applies a fault scenario
    - Determines connectivity
    - Finish time, δ, of the application



(a) $A^{original}$

(b) A affected by fault scenario

Channel $S_1 \rightarrow Mixer_1$ is blocked, Channel of $Heater_1$ suffers from a block defect.

A valve in the pump of $Mixer_1$ and the valves controlling the channel towards S_3 and the channel towards S_5 of S_4 are stuck open

$$Objective(\mathcal{A}) = \left(\sum_{f \in \mathcal{FS}}^{\mathcal{FS}} \neg ft \right) \times W_{ft} + \left(\sum_{f \in \mathcal{FS}}^{\mathcal{FS}} max(0, \delta - d_{\mathcal{G}}) \right) \times W_s + Cost_{\mathcal{A}}$$

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  - Maximum of 0 or δ - application deadline
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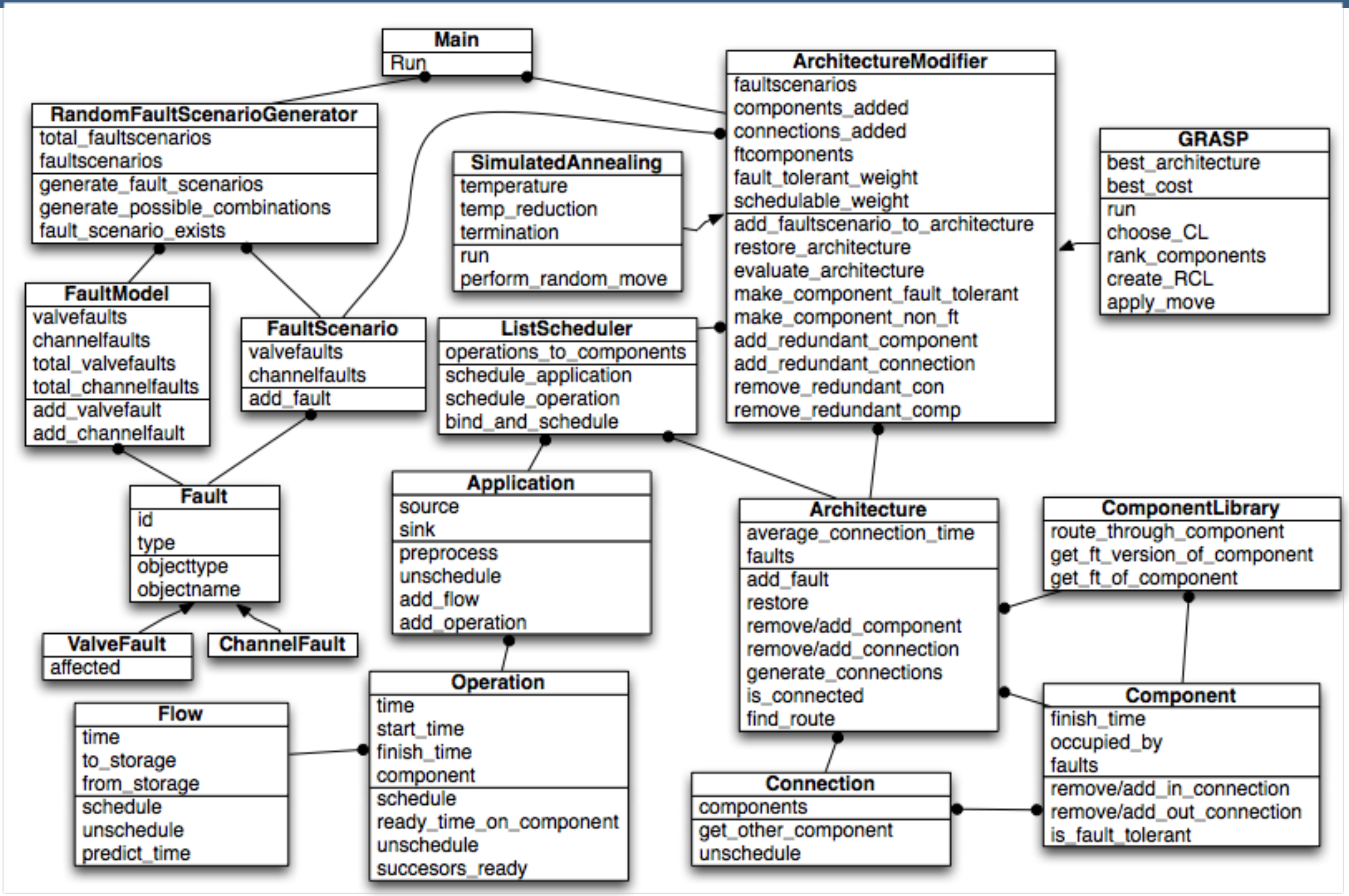
- Physical constraints
  - Sum of
    - Total number of valves
    - Total number of connections

Implementation



Experimental Setup

Implemented in

- **Python 3.4**
- **Intel Xeon X5550 processor**
- **Running at 2.65 GHz, with 24 GB RAM**
- **One synthetic benchmark S-1**
- **Two real-life benchmarks**
  - **IVD (In-Vitro-Diagnostics)**
  - **PCR (Polymerase-Chain-Reaction)**

Experimental Results

#	Name	Type	$\mathcal{A}_{initial}$		$\lvert\mathcal{O}\rvert$	$\lvert\mathcal{FS}\rvert$	$\mathcal{A}_{SA}$	$\mathcal{A}_{GRASP}$
			$\lvert\mathcal{N}\rvert$	$\lvert\mathcal{D}\rvert$				
1	S-1	Synthetic	15	17	5	100	06:23:54	01:22:36
2	S-1	Synthetic	15	17	5	25	-	00:23:23
3	S-1	Synthetic	15	17	5	50	-	00:45:23
4	S-1	Synthetic	15	17	5	85	-	01:15:45
5	S-1	Synthetic	15	17	5	121	-	01:43:26
6	PCR	Real-life	14	16	7	50	16:05:57	02:23:52
7	IVD	Real-life	52	78	12	100	184:50:28	27:40:37