Fast Prototyping Techniques Applied to the Hardware Simulation of Telecommunication Systems

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Abstract

In this paper, an application of fast prototyping techniques to the hardware simulation of telecommunication systems is shown. In particular, a hardware simulator, based on FPGA board, of a non-stationary satellite link for mobile communication is developed. For this kind of systems, the complexity of the software simulation in term of computation time is often unacceptable, especially when the estimation of global quality factors, such as the Bit Error Rate (BER), must be carried out. The hardware simulation of the system guarantees the reduction of the simulation time of several orders of magnitudes.

1. Introduction

This paper illustrates the use of fast prototyping techniques applied to the hardware simulation of telecommunication systems. The problem of the simulation of complex telecommunication systems in terms of global quality factors such as the Bit Error Rate (BER) is a well know issue.

In fact, in order to evaluate BER factors of 10E-4 ÷ 10E-5 we need to roughly use a number of samples at least 2 or 3 orders of magnitude bigger (10E+6, 10E+7). Consequently, the complexity of the software simulation in terms of simulation time is often unacceptable.

Different techniques have been developed to lower the simulation complexity in the software simulation of telecommunication systems, such the importance sampling and the bootstrap technique [1, 2, 3, 4, 5]. These methods lower the simulation complexity by using specific techniques for the choice of the input probability density function at the input of the system. In this way, an acceptable estimation of the BER can be reached by using a smaller number of input samples.

In parallel to the use of software techniques, the hardware simulation of the system guarantees a smaller simulation time of several order of magnitudes. At present, the availability of very dense Field Programmable Gate Arrays (FPGAs) permits a very low cost implementation of the prototype. The new approach known as *"fast prototyping"* is particularly suited to simulate telecommunication systems in hardware, because the possibility to run a lot of simulations with different parameters is a very important issue for these systems.

In this work, a very flexible hardware simulator of a satellite constellation for mobile communications has been developed. This simulator is suitable for the simulation of systems based on UMTS standard. In particular, a constellation composed by three non geo-stationary satellites has been implemented. The simulator is based on a board equipped with six Xilinx XCV-1000 FPGAs [6].

The paper is organized as follows: in section 2 further details on the telecommunication system to be modeled are given. Section 3 shows the architecture of the hardware emulator. In section 4, conclusions are drawn.

2. Telecommunication system description

A telecommunication system simulator should reproduce at best the real operating environment. Software simulation of a complex system does not allow an efficient evaluation of performance, especially when quality factors like BER must be measured. In these cases, the hardware emulation of the more complex parts of the telecommunication system allows to obtain significant evaluations in a fraction of time with respect to the full software approach.

In our case, the hardware simulator has been used as the core unit for the simulation of the degenerative effects of a satellite communication system. In particular,

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using the developed hardware simulator, the following effects can be modeled:

- different delays on different paths
- different path losses
- multi-path fading
- Doppler shift
- inter-channel cross-talk

Moreover, functional aspects such as beam hand-over, satellite hand-over and diversity reception can be modeled.

Our hardware simulator is able to emulate a constellation composed by three non geo-stationary satellites. Each satellite hosts seven beams with different path loss, delay and Doppler shift. Furthermore, different input signals can be combined to reproduce the interference between different users.

Thanks to those features, the developed system is suitable for the simulation of channel effects in mobile communications. In particular, non-stationary satellite constellations, like the UMTS one [7], can be easily simulated.

3. Hardware simulator architecture

The hardware simulator is composed by devices emulating three satellites equipped with seven beams each one. Six input signals are available for the simulator. The input signals can be delayed and attenuated. The satellite output signal is obtained combining the signals coming from the seven beams. The hardware simulator can provide the output signals in analog or in 12 bit LVTTL digital format.

The overall system architecture is sketched in Fig. 1.

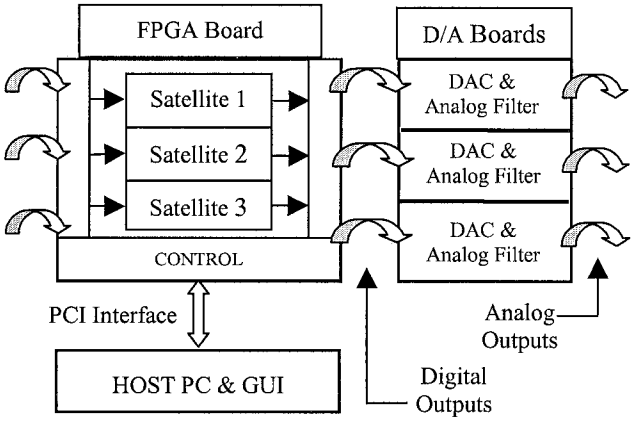

Figure 1: Hardware block diagram

From the figure, the following main blocks can be identified:

1. the *FPGA section*, which is used to implement the signal datapath;
2. the *Control section*, used to change the parameter settings;
3. the *Analog section*, including digital to analog converters, which is used to evaluate immediately the output signal quality by using a spectrum analyzer or an oscilloscope;
4. the *Host Personal Computer,* used to interface the board by using the PCI bus; the PC is used to send the messages to the FPGA board by using a Graphical User Interface (GUI).

A commercial PCI hosted board equipped with six Xilinx Virtex XCV1000-4 is used for the FPGA section. The DN2000K10 PCI Hosted board [6] has been selected. The DN2000K10 is a complete logic emulator system with up to six interconnected FPGAs. It can be hosted in a 32/64 bit PCI slot, or can be used stand alone. The overall architecture of the board is shown in Fig. 2.

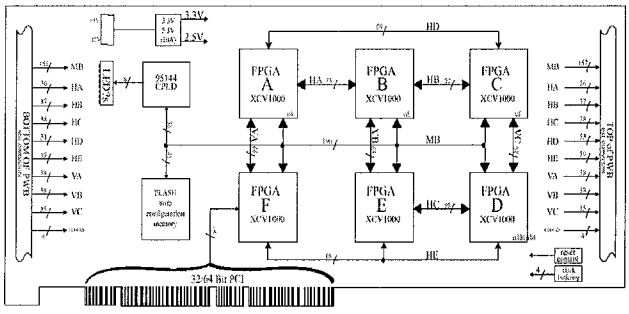

Figure 2: FPGA Board

Particular attention has been paid to the partitioning of the project. A single satellite unit is implemented on a single FPGA. We implemented three satellites, which is the minimum number needed to simulate the satellite handoff in permanent diversity condition, as required by UMTS standard [7].

The control section has been implemented on the FPGA F. It provides a PCI Target interface to the host PC. By using a specific Graphic User Interface (GUI) it is possible to select the simulator configuration, changing the values of attenuations, Doppler shifts, delays, etc.

The block diagram of a single satellite is sketched in Fig. 3. By configuring the input switching matrix three input signals are routed to the selected beams.

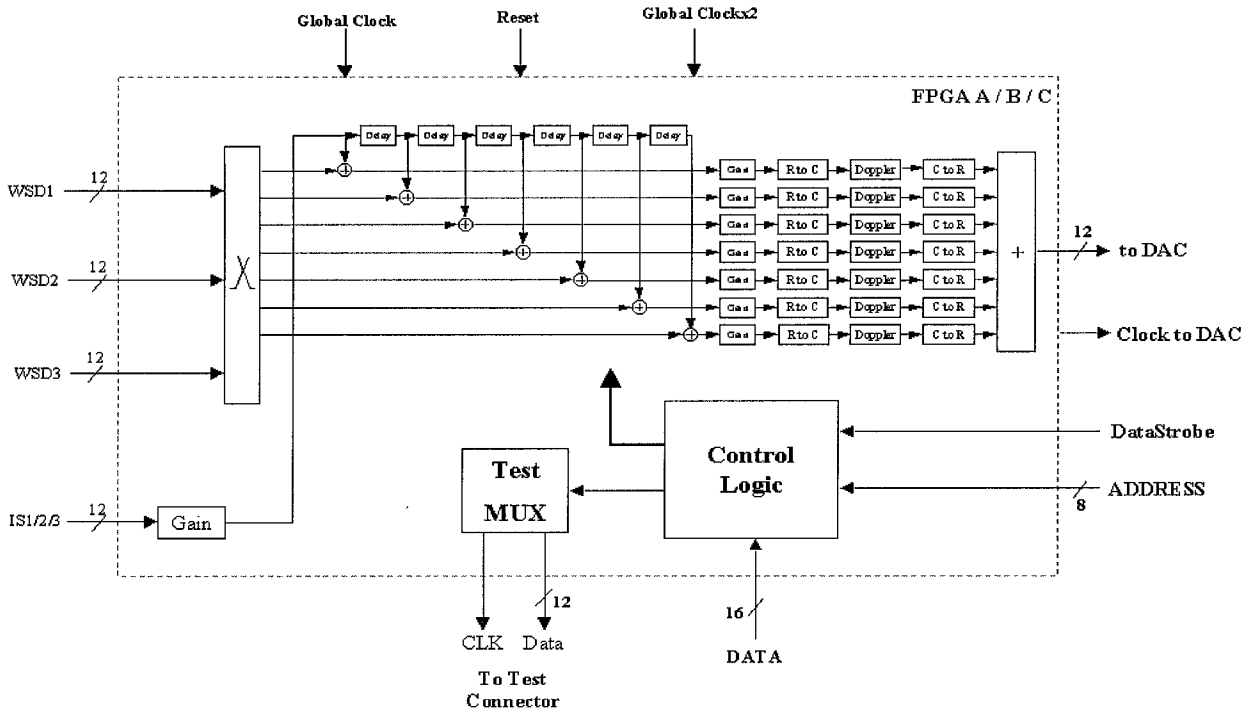

Figure 3: Satellite Block Diagram

The incoming signals can be delayed of a number of samples up to 8192. In that way, it is possible to simulate the effect of different delays in different paths.

A fourth signal is used to simulate interferences due to the presence of more than one user. The power of the interference signal can be adjusted by using a digital 72 dB programmable attenuator. The interference signal is delayed before being injected on each satellite beam. By changing the value of that delay we can obtain coherent or non coherent interference.

On each beam, the power of the signal coming from the linear combiner is adjusted by using a 36 dB programmable attenuator. In that way, it is possible to simulate the effects of different path losses. Moreover, it is possible to shift the signals in the frequency domain by using a Numeric Controlled Oscillator (NCO), used to simulate the Doppler effect. Changing the value of the Doppler shift in the range (–15 KHz : +15 KHz) the behavior of different delays on different paths (multi-path fading) can be simulated.

Finally the output signals coming from the seven beams are combined to obtain the satellite output. The output signal is available both in 12 bit two's complement format and in analog format. For the analog section, three AD9762-EVB boards by Analog Devices are used. Moreover, three custom PCBs, one for each output, are used to host the anti-aliasing filter and 50Ω de-coupling buffers. A full custom board has been developed to host a number of input/output connectors and test points, the digital to analog conversion boards, and to grant power supplies to the analog section.

A specific GUI has been developed to change the simulation parameters. The user can select the simulator configuration, changing separately any of the foreseen parameter. At the time the user wants his changes to be applied, he chooses the "SendtoPCI" button and the displayed configuration is downloaded to the control section. The last writes the values on the data bus in the right registers, according to the content of the address bus. This operation can be performed in run time, if needed. The GUI main window is shown in Fig. 4.

4. Conclusions

In this paper, a very flexible hardware simulator of a satellite constellation for mobile communications has been developed. In particular, a constellation composed by 3 non geo-stationary satellites has been implemented by using a prototype board equipped with six FPGAs.

The developed system is suitable for the simulation of satellite telecommunication systems even with mobile terminals. In particular, it can be used for simulations of systems based on UMTS standard.

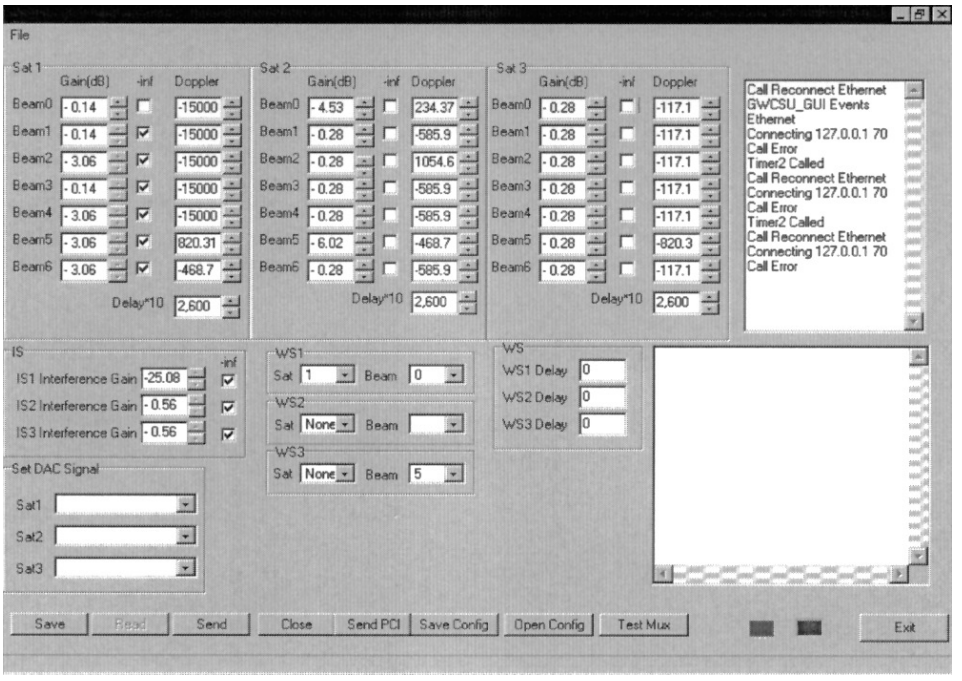

Figure 4: GUI main window

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