

CURRICULUM VITAE

ALBERTO NANNARELLI

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CURRENT POSITION

Associate professor at Technical University of Denmark, Department of Informatics and Mathematical Modelling.

EDUCATION

- **Ph.D. in Electrical and Computer Engineering**, June 1999.
University of California, Irvine (USA).
- **M.S. in Electrical and Computer Engineering**, June 1995.
University of California, Irvine (USA).
- **Eng. Degree *Laurea* in Electrical Engineering**, May 1988.
University of Rome La Sapienza, Roma, Italy.

EXPERIENCE

- **Dept. of Informatics and Mathematical Modelling, Technical University of Denmark**, Kongens Lyngby (Denmark)
Associate professor (May '03 - current).
- **Dept. of Electrical Engineering, University of Rome Tor Vergata**, Rome (Italy)
Post-doc Researcher (Sept.'99 - May '03).
- **Dept. of Electrical & Computer Engineering, University of California**, Irvine (USA)
Research Assistant (Jan'94 - June'99)
- **Rockwell International**, Newport Beach (CA), USA
Summer Intern (July'95 - Sept'95)
- **Ericsson Telecomunicazioni**, Rome (Italy)
System & Software Engineer (Sept'91 - Aug'93)
- **STMicroelectronics** (formerly SGS-Thomson Microelectronics), Agrate Brianza (Italy)
Design Engineer (Apr'90 - Aug'91)
- **Military Service in the Italian Army** (Mar'89 - Mar'90)
- **I.P.I.A. High School**, Orvieto (Italy) (Sept.'88 - Mar.'89)
Teacher of digital and analog electronics.

TEACHING EXPERIENCE

Years 2003-(today)

Courses currently taught at the **Technical University of Denmark**.

- *Design of Integrated Circuits* (terms: spring 2004 – spring 2009)
- *Advanced Digital Design Techniques* (terms: fall 2004 – fall 2008)
- *Design of Arithmetic Processors* (terms: spring 2007 – spring 2009)
- *Digital Systems* (terms: spring 2004 and spring 2005)

Years 1999-2003

- **University of Rome Tor Vergata**, Roma, Italy
 - *Digital Electronics* (Academic Years 2000/2001, 2001/2002)
 - *Signal Processing in Measurement Systems* (Academic Years 2000/01, 2001/02, 2002/03)
- **University of Perugia**, Orvieto campus, Italy
 - *Design of Data Acquisition and Processing Systems* (Ac. Years 1999/2000, 2000/01, 2001/02, 2002/03)
 - *Electronic Instruments and Measurement* (Academic Year 2000/01)

Previous years

- **Dept. of Electrical & Computer Eng., University of California**, Irvine (USA)
Teaching Assistant (1994 - 1999)

OTHER ACTIVITIES

Reviewer for several conferences and journals, including: *IEEE Trans. on Computers*, *IEEE Trans. on VLSI Systems*, *IEEE Trans. on CAD*, *IEEE Trans. on Circuits and Systems*, *Design Automation Conference (DAC)*.

PUBLICATIONS

Journal Articles (Peer Review)

- [1] T. Lang, and A. Nannarelli. “A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture“, *IEEE Transactions on Computers*, June 2007. Vol. 56(6), p. 727-739, June 2007.
- [2] E. Antelo, T. Lang, P. Montuschi and A. Nannarelli. “Digit-Recurrence Dividers with Reduced Logical Depth“, *IEEE Transactions on Computers*, Vol. 54, p. 837-851, July 2005.
- [3] L. Benini, A. Macii and A. Nannarelli. “A Code Compression Architecture for Cache Energy Minimization in Embedded Systems“, *IEE Proceedings - Computers and Digital Techniques. Special Issue on Low-Power Systems-on-Chip*. Vol. 149, Iss. 4, p. 157-163, July 2002.
- [4] A. Nannarelli and T. Lang. “Low-Power Divider“, *IEEE Transactions on Computers*, Vol. 48, p. 2-14, Jan. 1999.

Conference Papers (Peer Review)

- [5] W. Liu and A. Nannarelli. “Net Balanced Floorplanning Based on Elastic Energy Model“, *Proc. of 26th Norchip Conference*, p. 258-263, Tallinn, Estonia. November 2008.
- [6] W. Liu and A. Nannarelli. “Power Dissipation in Division“, *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 1790-1794. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 2008.
- [7] A. Nannarelli, M. Re, and G.C. Cardarilli, “Reducing Power Dissipation in Pipelined Accumulators“. *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 2098-2101. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 2008.
- [8] G.C. Cardarilli, A. Nannarelli and M. Re, “On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters“, *Proc. of 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, p. 37-41. Rodos, Greece. October 2008.
- [9] L. Dadda and A. Nannarelli. “A Variant of a Radix-10 Combinational Multiplier“, *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3370-3373. Seattle, USA. May 18-21, 2008.
- [10] G.C. Cardarilli, L. Di Nunzio, A. Nannarelli and M. Re. “ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations“, *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3434-3437. Seattle, USA. May 18-21, 2008.
- [11] G.C. Cardarilli, A. Nannarelli and M. Re. “Residue Number System for Low Power DSP Applications“, *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1412-1416. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. November 4-7, 2007.
- [12] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Impact of RNS Coding Overhead on FIR Filters Performance“, *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1426-1429. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. November 4-7, 2007.
- [13] T. Lang and A. Nannarelli. “Combined radix-10 and radix-16 division unit“, *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 967-971. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. November 4-7, 2007.
- [14] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Low-power adaptive filter based on RNS components“, *Proc. of 2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3211-3214. New Orleans (USA), May 28-31, 2007
- [15] T. Lang and A. Nannarelli. “A Radix-10 Combinational Multiplier“, *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 313-317. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 29 - November 1, 2006.
- [16] A. Nannarelli, M.S. Rasmussen, and M.B. Stuart. “A 1.5 GFLOPS Reciprocal Unit for Computer Graphics“, *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1682-1686. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 29 - November 1, 2006.
- [17] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “A hybrid RNS adaptive filter for channel equalization“, *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1706-1710. Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 29 - November 1, 2006.

- [18] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Low Power and Low Leakage Implementation of RNS FIR Filters“, *Proc. of 39th Asilomar Conference on Signals, Systems, and Computers*, p. 1620-1624, Asilomar Hotel and Conference Grounds, Pacific Grove, CA, USA. October 30 - November 2, 2005.
- [19] E. Antelo, T. Lang, P. Montuschi and A. Nannarelli. “Low Latency Digit-Recurrence Reciprocal and Square-Root Reciprocal Algorithm and Architecture“, *Proc. of 17th Symposium on Computer Arithmetic*, p. 147-152, Cape Cod (USA), June 27-29, 2005.
- [20] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Programmable Power-of-two RNS Scaler and its Application to a QRNS Polyphase Filter“, *Proc. of 2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 1002-1005, Kobe (Japan), May 23-26 2005.
- [21] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Low-Power Implementation of Polyphase Filters in Quadratic Residue Number System“, *Proc. of 2004 IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. II, p. 725-728, 23-26 May 2004.
- [22] A. Del Re, A. Nannarelli, and M. Re. “A tool for automatic generation of RTL-level VHDL description of RNS FIR filters“, *Proc. of 2004 Design, Automation and Test in Europe Conference (DATE)*, Vol. 48, p. 686-687, Paris (France), Feb. 16-20, 2004.
- [23] A. Nannarelli, G.C. Cardarilli, and M. Re. “Power-delay tradeoffs in residue number system“, *Proc. of 2003 IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. V, p. 413-416, 25-28 May 2003.
- [24] G.C. Cardarilli, A. Del Re, R. Lojaco, A. Nannarelli, and M. Re. “RNS implementation of high performance filters for satellite demultiplexing“, *Proc. of the 2003 IEEE Aerospace Conference*, Vol. 3, p. 1365-1379, March 8-15, 2003.
- [25] E. Antelo, T. Lang, P. Montuschi, and A. Nannarelli. “Fast Radix-4 Retimed Division with Selection by Comparisons“, *Proc. of IEEE 13th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2002)*, p. 185-196, San Jose, California (USA), July 17-19, 2002.
- [26] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Residue Number System Reconfigurable Datapath“, *Proc. of 2002 IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. II, p. 756-759, Phoenix, Arizona (USA), May 2002.
- [27] G.C. Cardarilli, A. Del Re, A. Nannarelli and M. Re. “Power Characterization of Digital Filters Implemented on FPGA“, *Proc. of 2002 IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. V, p. 801-804, Phoenix, Arizona (USA), May 2002.
- [28] A. Del Re, A. Nannarelli, and M. Re. “Implementation of Digital Filters in Carry-Save Residue Number System“, *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1309-1313, Asilomar Hotel and Conference Grounds, Pacific Grove, California (USA), Nov. 2001.
- [29] A. Del Re, A. Nannarelli, and M. Re. “Fast Prototyping Techniques Applied to the Hardware Simulation of Telecommunication Systems“, *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1314-1317, Asilomar Hotel and Conference Grounds, Pacific Grove, California (USA), Nov. 2001.
- [30] A. Nannarelli, M. Re, A. Del Re, G.C. Cardarilli and R. Lojaco. “High Speed RNS A/D Front End“, *Proc. of 6th Euro Workshop on ADC Modelling and Testing*, p. 19-22, Lisbona (Portugal), Sep. 2001.
- [31] L. Benini, A. Macii and A. Nannarelli. “Cached-Code Compression for Energy Minimization in Embedded Processors“ *Proc. of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 322-327, Huntington Beach, California (USA), Aug 2001.
- [32] A. Nannarelli, M. Re and G.C. Cardarilli. “Tradeoffs between Residue Number System and Traditional FIR Filters“, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. II, p. 305-308, Sydney (AUS), May 2001.
- [33] M. Re, A. Nannarelli, G.C. Cardarilli and R. Lojaco. “FPGA Implementation of RNS to Binary Signed Conversion Architecture“, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. IV, p. 350-353, Sydney (AUS), May 2001.
- [34] A. D’Amora, A. Nannarelli, M. Re and G.C. Cardarilli. “Reducing Power Dissipation in Complex Digital Filters by using the Quadratic Residue Number System“, *Proc. of 34th Asilomar Conference on Signals, Systems, and Computers*, p. 879-883, Asilomar Conference Grounds, California (USA), Nov. 2000.
- [35] G.C. Cardarilli, A. Nannarelli and M. Re. “Reducing Power Dissipation in FIR Filters using the Residue Number System“, *Proc. of 43rd IEEE Midwest Symposium on Circuits and Systems*, p. 320-323, Lansing, USA, Aug. 2000.

- [36] R. Lojaco, G.C. Cardarilli, A. Nannarelli and M. Re. “Residue Arithmetic Techniques for High Performance DSP“, *Problems in Modern Applied Mathematics*, World Scientific Engineering Society Press, p. 314-318, Sep. 2000.
- [37] A. Nannarelli and T. Lang. “Low-Power Radix-4 Combined Division and Square Root“, *Proc. of IEEE International Conference on Computer Design (ICCD)*, p. 236-242, Austin, Texas (USA), Oct. 1999.
- [38] A. Nannarelli and T. Lang. “Low-Power Division: Comparison among implementations of radix 4, 8 and 16“, *Proc. of 14th Symposium on Computer Arithmetic*, p. 60-67, Adelaide (AUS), Apr. 1999.
- [39] A. Nannarelli and T. Lang. “Low-Power Radix-8 Divider“, *Proc. of IEEE International Conference on Computer Design (ICCD)*, p. 420-426, Austin, Texas (USA), Oct. 1998.
- [40] A. Nannarelli and T. Lang. “Power-Delay Tradeoffs for Radix-4 and Radix-8 Dividers“, *Proc. of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 109-111, Monterey, California (USA), Aug. 1998.
- [41] A. Nannarelli and T. Lang. “Low-Power Radix-4 Divider“, *Proc. of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 205-208, Monterey, California (USA), Aug. 1996.

Other Publications

- [42] A. Nannarelli. “Low-Power Division and Square Root“, Ph.D. Dissertation, University of California, Irvine, June 1999.
- [43] A. Nannarelli. “Power Evaluation Tool: modeling and implementation“, COMPASS User’s Group Conference, San Jose, CA, Apr. 1996.
- [44] A. Nannarelli. “Implementation of a Radix-512 Divider“, M.S. Thesis, University of California, Irvine, June 1995.
- [45] A. Nannarelli and T. Lang. “Implementation of Division and Square Root: Modeling and Evaluation“, Final Report for MICRO Project #94-070, University of California, 1995.
- [46] A. Nannarelli and T. Lang. “Implementation of Division with Prescaling: Modeling and Evaluation“, Final Report for MICRO Project #93-088, University of California, 1994.