Hybrid Digital-Analog Feedback Audio Amplifiers

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in cooperation with

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Abstract

This thesis is concerned with the topic of digital control of the power stage of a Class D amplifier with digital input. The thesis contains an examination of the error sources in the analog power stage, where the main contributors to distortion are identified.

The analog control system for digital class D amplifiers, PEDEC, is explained, and it's influence on the amplifiers performance is shown.

The two digital modulation forms dAIM and WPWM are described. The quantization noise caused by $\Delta\Sigma$ modulation is examined as both modulators contain elements of the $\Delta\Sigma$ modulator.

A Simulink model is implemented in MATLAB, to allow for simulation of modulator and power stage. This model is verified against existing real amplifiers, and serves as a simulation platform for development of control systems.

The demands on digital control systems is determined in terms of allowable delay and required bandwidth.

Two forms of feedback are discussed and implemented in Simulink, using the previous designed amplifier model. The first model is with a simple feedback of timing information, while the second is with feedback of amplitude information as well. The second is designed by discretizing the analog control system PEDEC.

Resumé

Denne rapport omhandler emnet digital regulering af effekttrinnet i en klasse D forstærker med digitalt input. Rapporten indeholder en gennemgang af fejlkilderne i det analoge effekttrin, og de største bidragydere til forvrænging bliver identificerede.

Det analoge reguleringssystem, PEDEC, til digitale klasse D forstærker er forklaret, og der er redegjort for dets inflydelse på forstærkerens performance.

De to digitale modulationsmetoder dAIM og WPWM bliver beskrevet. Da begge modulatorer indeholder elementer af $\Delta\Sigma$ modulatoren er kvantiseringsstøjen forårsaget af denne modulering blevet undersøgt.

En Simulink model er blevet implementeret i MATLAB for at kunne simulere både modulator og effekttrin. Denne model er blevet sammenlignet med virkelige forstærkere og tjener som evalueringsgrundlag for test af reguleringssystemer.

kravene til et digitalt reguleringssystem bliver bestemt udfra den krævede båndbredde, og den tilladelige forsinkelse .

To forskellige feedback metoder bliver diskuteret, og bliver ved hjælp af den designede forstærkermodel implementeret i Simulink. Den første model anvender et simpelt feedback af timinginformation. Den anden model anvender et feedback af amplitudeinformation. Reguleringssystemet i det andet system er skabt ved at diskretisere det analoge system PEDEC.

Preface

This thesis was written to fulfill the requirements to obtain a master of science degree in engineering from the Technical University of Denmark.

The project was written in cooperation with IMM and Bang & Olufsen ICEpower A/S. This ensured me a fertile environment in which I could develop the project, with contributions from the academic as well as the commercial world.

I would like to thank my two supervisors, Steen M. Munk and Jan Larsen, who have supplied me with invaluable critics and ideas to the further development of my project. Especially Steen has been a constant source of inspiration and relevant comments.

During this project my colleagues from Bang & Olufsen ICEpower A/S have all been extremely helpful, especially in the subject of analog power electronics where I have only a limited experience. I would like to thank them all for their help.

I would like to thank my girlfriend, and now wife, Line Wolff, for her support during my project, her trust in me, and for proofreading my thesis.

I would like to thank Martin Rune Andersen, for relevant technical discussions relating to my thesis, technical proofreading and a beer now and then.

Finally, I would like to thank my parents in law for planning a magnificent wedding for me and my wife while I was busy writing my thesis.

Crilles Bak Rasmussen, 31. august 2004, Lyngby

Contents

Abbreviations

Abbreviation:	Description:
A/D	Analog/Digital (converter)
CD	Compact Disc
AIM	Astable Integrating Modulator
D/A	Digital/Analog (converter)
dAIM	digital Astable Integrating Modulator
DPMA	Digital Pulse Modulating Amplifier
DSP	Digital Signal Processing
ICE	Intelligent Compact Efficient
i.i.d.	indefinite independent distribution
IMD	InterMoDulation
kSps	kilo Samples per second
LPWM	Linear Pulse Width Modulation
MSps	Mega Samples per second
NPWM	Natural Pulse Width Modulation
PAE	Pulse Amplitude Error
PEDEC	Pulse Edge Detection and Error Correction
PMA	Pulse Modulating Amplifier
PSD	Power Spectrum Density
PSRR	Power Supply Rejection Ratio
PTE	Pulse Timing Errors
PWM	Pulse Width Modulation
SACD	Super Audio Compact Disc
THD	Total Harmonic Distortion
UPWM	Uniform Pulse Width Modulation
VLSI	Very Large Scale Integration (chip technology)
WPWM	Weighted Pulse Width Modulation

Symbols

Variable:	Description:
A_d	AMplitude of fourier components of error signal caused by blanking delay
A_m	Harmonic amplitudes relative to V_s
b	Number of bits
b_{rq}	Number of bits after requantization
c	Function for [-1 1] into [0 1] mapping (WPWM)
c_1	Current mapped sample (WPWM)
c_2	Next mapped sample (WPWM)
D	Dynamic range
e	Quantization error
E_{n}	Error on output (noise shaper)
E_{rq}	Quantization error (noise shaper)
f_{bw}	Bandwidth
f_{c}	Switch freqyncy (cycle frequency)
f_{ovs}	Frequency after oversampling
f_s	sampling frequency
f_{sampling}	Sampling frequency
G	Gain factors for dAIM
I_{l}	Load current
$\mathrm{IMD}(M)$	Intermodulation caused by power supply perturbations
I_{t}	Transistor current
k	Difference between to concurring samples (WPWM)
L	Oversampling factor
m	Index used in analysis of harmonics
M	Modulation index
NTF	Noise Transfer Function
NTF_α	Noise Transfer function in baseband (Noise shaper)
NTF_β	Noise Transfer function in high frequency area (Noise shaper)
q	Quantizer stepsize
Q_b	Quantizer noise in baseband
Q_n	Quantizer noise level
Q_{OVS}	Quantizer noise in baseband after oversampling
s_n	Amplitude of component n in noise spectra
s_{ee}	Power spectra density of $\Delta\Sigma$-modulator quantization error
STF	Signal Transfer Function
s_{xx}	Power spectra density of $\Delta\Sigma$-modulator input
s_{yy}	Power spectra density of $\Delta\Sigma$-modulator output

t_c	Switching period (cycle time)
t_d	Time delay (blanking delay)
t_{df}	Fall Time Delay
t_{dr}	Rise Time Delay
t_p	Estimated crossing time (WPWM)
THD_d	Total Harmonic Distortion caused by blanking delay
u	Quantizer input
u_n	Quantizer input at time n
v_e	Error voltage
$v_o(t)$	Amplfier output voltage
$v_r(t)$	Amplifier reference voltage (input)
V_s	Power supply voltage
v_{sp}	Power supply perturbation voltage
y_e	Error output
y_{x}	Signal output
α_d	blanking delay / switch period ratio
β	DC Input for noise model of $\Delta\Sigma$ modulator
Δ	Quantizer step size
γ_{m}	Phase margin
ω_b	Upper limit of baseband [rad/s] (Noise shaper)
ω_m	Frequency of the m^{th} harmonic power supply perturbation
ω_r	Frequency of amplifier input [rad/s]
ω_s	Sampling frequency [rad/s] (Noise shaper)

Chapter 1

Introduction

The classic approach to electronic audio amplification is the class A/B amplifier which consists of two variable resistors connected in series between a positive and a negative power rail. The midpoint between the two resistors is then used as the amplified output, referred to ground. To obtain proper operation of the amplifier the resistors should be varied according to the incoming audio signal, where the resistor connected to the positive power rail ideally approaches infinity when the input signal is negative, and approaches a short circuit at maximum input. The resistor connected to the negative power rail operates opposite. In practice this type of resistors can be realized by transistors operated within their linear region. This very basic amplifier is shown in Figure 1.1. This type

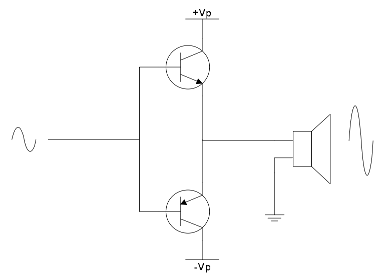

Figure 1.1: Basic layout of the class A/B amplifier.

of amplifier is captivating as the function is easy perceived. To obtain good performance the only thing needed is sufficiently good transistors. However there is one major disadvantage; the efficiency.

$$P = I^2 \cdot R \tag{1.1}$$

Having a resistor in the high current path causes a significant power loss, especially at mid level. At low levels the losses are small as the resistance is large and thus only a small current is conducted, at high levels the loss is low as the resistance is quite small. However in the mid range, where most music lies, the losses are significant. These properties are easily seen from Equation 1.1.

They are illustrated by Figure 1.2, where the power dissipated is plotted as a function of output voltage for an ideal class A/B power stage. For a non-ideal power stage the loses will be larger. A transistor is usually unlinear in the outer

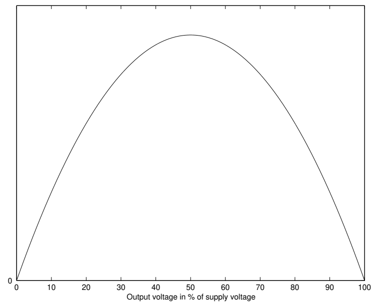

Figure 1.2: Power dissipated, plotted as function of output voltage. y-axis is linear, starting from 0 at the bottom.

ranges which prevents operating it in the areas with very low or high resistance. The losses induced are unwanted as they are costly; more power is consumed, better components are required throughout the amplifier to handle the power required and heat sinks are required for cooling the transistors.

By instead operating the output transistor as switches, and thus having only two levels, *on* and *off* the mid-level with the greatest losses is avoided. This is fundamentally different from the class A/B amplifier where the transistors are operated in their linear region, and the extreme regions are avoided. This is the basic principle of class D amplification.

It is not possible to use a standard audio signal for controlling the switching elements, some kind of pulse modulation is required. This modulation can be done in different ways depending on the nature of the input; analog or digital. This thesis is mainly concerned with the digital modulation, however the analog is treated briefly.

In the recent years class D amplifiers has experienced large success in the audio industry. This is mainly due to advanced analog feedback schemes which allows for performance comparable to class A/B amplifiers at significantly lower price. The class D amplifier's main advantage is a very high efficiency about 90% whereas the classic class A/B amplifier only offers about 60%. This is a great advantage as this greatly reduces the power dissipated in the amplifier, and thus allows the use of smaller components and heat sinks. This ultimately allows for a lower size and cost.

As mentioned earlier the success of class D amplifiers is heavily dependent on the analog feedback systems used. However it would only seem reasonable to employ a digital feedback system when having a digital input. This can be beneficial in several ways; lower cost, as less circuitry is required, and the feedback system furthermore can be implemented with almost no cost if excess computing power is available in existing systems. The larger integration might also lead to smaller systems, and thus pave the way for the use of digital class D amplifiers in mobile applications.

The processing power required to implement the control system might seem unreasonable when a suitable analog system is available. A WPWM modulator requires almost all processing power supplied by many low and mid range digital signal processors, but given the continuous rise in the processing power available in consumer electronics this will only be a minor problem within a few years.

The available digital signal processing power in consumer audio today is rising fast as more and more audio systems include surround sound. Current research is concerned with compensation of the loudspeakers using digital pre-compensation. These digital compensated speakers will boost the use of DSP further.

In the light of the widespread use of DSP it will seem naturally to implement the amplifiers control system in DSP as well. This will allow for a system wide control system which will be able to correct any audio distortion occurring between the source and the ear. The change into DSP based compensation will further ease implementation as the amplifier performance can be changed through software instead of hardware changes. This increased flexibility will ease product development, and shorten the development time required to complete a product.

Chapter 2

Digital class D amplifiers in theory

The theory presented in this chapter is based on an extensive literature study. It consists of contributions from many sources relating to class D amplification, and should be seen as a summary of these. Some of these sources are cited directly in the text while others serve as background knowledge. To facilitate further investigations in the subjects treated here, a graphical overview of the references are presented in Figure 2.1. The subject of each piece of literature read is

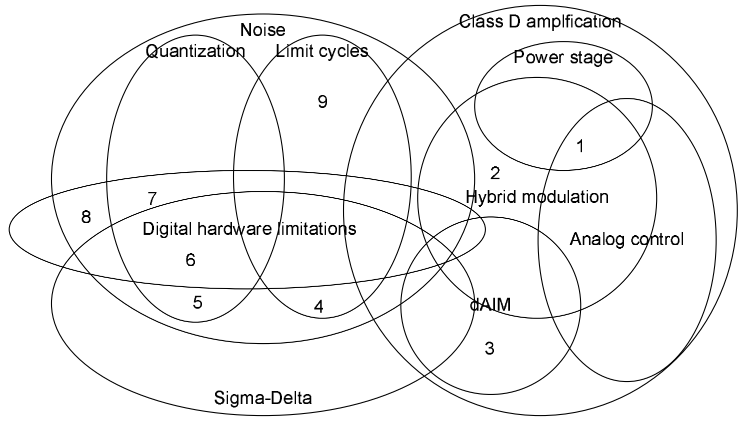

Figure 2.1: Visualization of the subject treated during the literature study.

indicated by the placement in the figure. Each location containing literature is designated by a number, which refers to the related description below.

1. This group contains literature concerning class D amplifiers, both describing analog and digital design. The sole piece in the group is [Nie98] which describes both analog amplifiers and digital hybrid amplifiers with analog control.

2. This group describes hybrid modulation schemes for digital class D amplification. [Hio94, JN99]

3. This group contains literature describing digital astable integrating modulation for digital class D amplification. This group includes [And03, Kje03].

4. This group contains literature about limit cycle oscillations which occur in $\Delta\Sigma$ modulators when idling. [FH01]

5. This group contains literature concerning quantization noise in $\Delta\Sigma$ modulators. [Ker00, DTWL03, NL94, Del92, MP02, Gra89, RMGW89, WCG89, Gra90, Gal93, Gal94, RL94, GCM97, GT02, JV92]

6. This group contains literature concerning quantization noise in $\Delta\Sigma$ modulators originating from digital hardware limitations. [Won90]

7. This group contains literature on other hardware limitations, not related to quantization errors. [JdlRRV99]

8. This grouping concerns hardware noise not related directly to quantization. [ASVL99]

9. This Grouping concerns general limit cycles in oversampling converters. [MJ93]

The groupings listed here are not fully covering, however they should be sufficient to uncover the basic topics of the literature.

2.1 The analog class D amplifier

The basic principle is to encode the audio signal as a pulse modulated signal. This pulse modulated signal can then be used as a control signal for the switching elements. This generates a power pulse modulated signal, still containing the audio signal. By low pass filtering this signal, the audio signal can be reconstructed in an amplified version.

The basic analog class D pulse modulator, modulates the signal into a pulse width modulation (PWM) signal. The basic modulator is basically created by a comparator which has two inputs: a carrier wave and the signal which is to be modulated. The carrier wave are typically some sort of saw tooth, which is modified according to the modulation used eg. single sided, trailing or leading edge or double sided. This type of pulse width modulation is called Natural Pulse Width Modulation (NPWM).

The amplifier currently used by Bang & Olufsen ICEpower A/S is based on the COM/MECC (Controlled Oscillation Modulation/ Multivariable Enhanced Cascade Control) topology as the above principle does not allow for implementation of a control system suitable to correct the errors caused by the power stage. The overall layout of a COM/MECC system is shown in Figure 2.2. Taken from left, the diagram starts with the input which is analog (or digital through a D/A converter). This analog signal is pulse modulated in the COM/MECC Block. The pulse modulated signals are then amplified by a power switch, and finally demodulated using a 2^{nd} order low pass filter. The open-loop transfer function of a pure COM system contains a 1^{st}order low pass filter with a cut-off frequency of 80 kHz and 2 additional poles designated as “COM poles”. These two poles are located at the amplifier's switching frequency (f_c). This gives at total phase lag of 180 degrees at f_c and thus causes the amplifier to oscillate. This feedback loop furthermore has an error correcting effect.

The COM/MECC system is a hybrid system created of a MECC system with an embedded COM modulator. The COM/MECC system currently offers some of the best performance available for analog class D amplification. For information on the actual operation of this system please refer to Bang & Olufsen ICEpower A/S' homepage where articles relating this technology are available.

2.2 Power stage

The digital class D amplifiers available operates without a global feed back around both modulator and power stage, opposite to COM/MECC where the power stage is an embedded part of the system. The power amplification is done by using the PWM signal to control a power switch which is connected to the amplifier's power supply. Finally the signal is demodulated using a 2^{nd} order low pass filter, to retrieve the original audio waveform. The basic principle is shown in Figure 2.20, the two feedbacks should be ignored. The basic layout for the power switches can be seen in Figure 2.3. This configuration is created by two switching legs with the load connected in between. The switching elements are then operated diagonally. The benefit of this configuration is that it allows $2 \cdot V_{cc}$ over the amplifier's load (the speaker). Simpler configurations exist where only one switching leg is employed. In these configurations the output voltage is then referred to ground and the lower switching element is connected to $-V_{cc}$.

The errors occurring in the power stage can be divided into Pulse Timing Errors (PTE) and Pulse Amplitude Errors (PAE). PTE errors occur whenever the edges of the pulse signal is misplaced. Amplitude errors mainly origin from a non-ideal power supply and components.

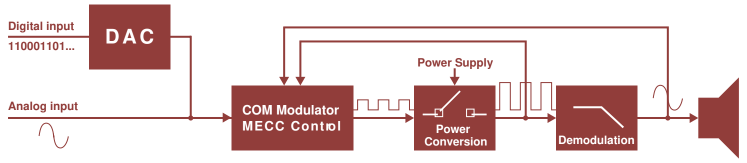

Figure 2.2: Overall layout of COM/MECC based analog amplifier. Taken from Bang & Olufsen ICEpower A/S marketing material.

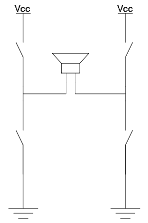

Figure 2.3: Basic powerstage (H bridge)

2.2.1 Pulse Timing Errors

Pulse Timing Errors (PTE) are characterized by causing a misplacement of the rising and falling transitions of the pulse train.

Blanking Delay

When considering PTE the main error source is the blanking delay. The blanking delay is a short amount of time where all switches in the power stage are off. This blanking delay is used to avoid the phenomenon "shoot through" or "cross conduction", caused by the transistor's dead time, and resulting in excessive strain on the switching elements and lower efficiency.

The error caused by the blanking delay is reflected in the error voltage, v_e, given by Equation 2.1. In this expression t_d is the blanking delay and t_c is the switch cycle time. The power supply voltage is considered to be unity.

$$v_e = \begin{cases} \frac{-2t_d}{t_c} & (I_L > 0) \\ \frac{2t_d}{t_c} & (I_L < 0) \end{cases} \tag{2.1}$$

When considering a sinusoidal output current the harmonic distortion caused by the blanking delay can be written as a fourier series, where the component's amplitude is expressed by Equation 2.2.

$$A_d(m) = -2\frac{t_d}{t_c}\frac{\sin\left(m\frac{\pi}{2}\right)}{m\frac{\pi}{2}} \tag{2.2}$$

This leads to the expression for THD caused by the blanking delay, Equation 2.3. In this expression the ratio between switching period and blanking delay are given by α_d, Equation 2.4.

$$\mathrm{THD}_d\left(M, \alpha_d\right) \approx \frac{\sqrt{\sum_{i=2}^{N_{\max}}\left[2\alpha_d\frac{\sin\left(i\frac{\pi}{2}\right)}{i\frac{\pi}{2}}\right]^2}}{M - \alpha_d\frac{4}{\pi}} \tag{2.3}$$

$$\alpha_d = \frac{t_d}{t_c} \tag{2.4}$$

The expression derived is based on a sinusoidal output current, this however limits the use as the output current is seldom sinusoidal. Typically the output current contains a ripple, controlled by eg. the output filter. Instead another expression is derived.

When operating at low modulation depths, and thus having a low current, blanking free operation can be obtained. When in blanking free operation the distortion is reduced significantly. The criteria for blanking free operation is that the output current is smaller than the transistor current, ($\hat{I}_L < \hat{I}_T$). This situation is possible due to the output inductor.

Equation 2.7 offers a solution considering non-sinusoidal output current. To expand this expression to cover blanking free operation as well, Equation 2.6 is used to choose $\Delta(\alpha_I)$.

$$\alpha_I = \frac{\hat{I}_T}{\hat{I}_L/M} \tag{2.5}$$

$$\Delta(\alpha_I) = \begin{cases} 0 & I_L \leq I_T \\ \frac{\frac{\pi}{2}-\sin(\alpha_I)}{\frac{\pi}{2}} & I_L > \hat{I}_T \end{cases} \tag{2.6}$$

$$\mathrm{THD}_d\left(M, \alpha_d, \alpha_I\right) \approx \frac{\Delta\left(\alpha_I\right)\sqrt{\sum_{i=2}^{N_{\max}}\left[2\alpha_d \frac{\sin\left(i\frac{\pi}{2}\right)}{i\frac{\pi}{2}}\right]^2}}{M - \alpha_d \frac{4}{\pi}\Delta(\alpha_I)} \tag{2.7}$$

The main disadvantage to this method is that the ripple currents should be determined. A better model of the power stage and demodulation filter is thus required.

Delay distortion

Delay distortion is caused by the delay from whenever a control signal, to a switching element, is changed, to the change is reflected in the switching element. The delay is controlled by the parasitic capacities in the switching elements. The delays are different for rise (t_{dr}) and fall (t_{df}). Thus both should be calculated to determine the total impact of the delay distortion. The delay distortion is according to [Nie98] under 10 ns absolute delay, and insignificant for the differential delay, and the delay distortion should thus be no problem as long as it is considered during the power stage design in order to minimize the differential delay.

Rise and fall times

Rise and fall time errors are caused by the time from the switch output starts to change until the transition is completed. Rise and fall times errors can both be characterized as PTE and PAE as they influence both amplitude and timing. As the delay distortion, the error is dependent on the direction of the transition. According to [Nie98] the effect is moderate in comparison with other sources.

2.2.2 Pulse Amplitude Errors

Pulse Amplitude Errors are errors in the pulse amplitude. They are typically caused by non-ideal power supplies and finite resistance in the circuits used. These flaws cause an amplitude error correlated with the output current.

Power supply perturbations

The power supply perturbations occur as the power supplies in audio amplifiers typically have a much lower bandwidth than the amplifier. The worst case supply is created by a transformer with a rectifier bridge and a capacitor. This type of power supply is often used though it offers the worst performance. The basic property of a power amplifier is shown in Equation 2.8. In this equation $v_o(t)$ is the output voltage, V_s is the supply voltage and $v_{sp}(t)$ is the perturbation on the power supply, and $v_r(t)$ is the reference signal controlling the amplifier (e.g. audio).

$$v_o(t) = v_r(t)V_s + v_r(t)v_{sp}(t) \tag{2.8}$$

In [Nie98] the harmonic perturbation in Equation 2.9 is then considered. In this equation A_m is the amplitude relative to $v_r(t)$. The reference voltage is given by Equation 2.10.

$$v_{sp}(t) = \sum_{m=0}^{M_{\max}} A_m \cos(m\omega_m t) \tag{2.9}$$

$$v_r(t) = M\cos(\omega_r t) \tag{2.10}$$

From Equation 2.8, 2.9 and 2.10 the expression for the perturbed output can now be written, Equation 2.11.

$$v_o(t) = \frac{1}{2}M \sum_{m=0}^{M_{\max}} A_m \left[\cos(\omega_r t + m\omega_m t) + \cos(\omega_r t - m\omega_m t)\right] \tag{2.11}$$

It can be seen that the perturbations intermodulate with the reference signal. The intermodulation components caused by the power supply perturbations can then be determined from Equation 2.12.

$$\mathrm{IMD}(M) \approx \frac{\sqrt{2\sum_{m=1}^{M_{\max}} \left(\frac{1}{2}MA_m\right)^2}}{M(1+A_0)} = \frac{\sqrt{2\sum_{m=1}^{M_{\max}} A_m^2}}{2(1+A_0)} \tag{2.12}$$

The intermodulation caused by perturbations of the power supply is quite severe, thus it is not possible to design a PMA with a unregulated power supply unless error correction or a very expensive power supply is used. The perturbed power supply is quite interesting, as a parameter usually specified for amplifiers, is the power supply rejection ration (PSRR), which is a measure of the influence the power supply variations have on the audio output. This influence can be minimized by a proper control system.

Finite switch impedance

The error occurring due to finite switch impedance is caused by the voltage drop across the switch whenever it is conducting. The voltage drop is dependent on the conducted current. The analysis of the switch impedance is quite complex, it can be found in [Nie98]. Here it is concluded that the influence of finite switch impedance can be minimized by selecting the power components properly.

2.2.3 Summary on power stage errors

As described there are many sources of errors in the power stage. According to [Nie98] the main error sources are the blanking delay and the power supply perturbations. These error sources should thus be included when simulating to obtain a sufficiently good simulation.

These error sources are primarily the parasitic components within the circuit. This is especially important for the demodulation filter which has an inductor with many un-linearities. If needed, more error sources can be added after the initial simulation to allow for more accurate simulations.

2.3 Digital class D amplification

As the audio industry moves towards digital audio, amplifiers that accept a digital input are required. This is easily made by buying a good D/A converter and connecting it to an analog class D amplifier. Instead, by converting the digital signals in the digital domain the D/A converter could be left out, and an expensive component could be spared. A great amount of research has taken place into designing class D amplifiers which has a PCM (Pulse Code Modulation) input, and thus making a power D/A converter. The main objectives for this research have been to reduce the signal path by integrating the D/A converter and the amplifier into one circuit. This further leads to a cost reduction as the overall component count is reduced, while the overall complexity of the system does not increase.

When considering class D amplifiers people typically tend to categorize all class D amplifiers as digital, as they operate in a finite number of levels (often two), however they neglect the fact that the width of the pulse is analog as the flanks are defined in continuous time. Thus the pulse modulated output from any modulator, analog or digital, should be considered an analog signal. The modulator itself can be both digital or analog, depending on the input.

The fundamental strategies in class D amplification are divided into the hybrid modulators where the WPWM modulator is explained, and the $\Delta\Sigma$ modulators where dAIM is explained.

2.3.1 Uniform Pulse Width Modulation (UPWM)

The power stages used in class D amplifiers require a 1-bit signal to control the switching elements, thus a conversion is required from the standard PCM coded signal to a pulse coded signal; uniform pulse width modulation. This modulation is one of the simplest, and is performed by having a counter with same bit-resolution as the signal (e.g. 16 bit). This counter is incremented in each clock cycle. In the simplest form, the single sided trailing edge modulator, the 1-bit output is then created by comparing the counter with the input signal sample. If the input is larger than the counter value the input is 1, otherwise -1. Each time the counter overflows a new sample is latched into the comparator. The switch frequency of the amplifier is thus equal to the sampling frequency of the input signal. The basic implementation can be seen in Figure 2.4. This implementation consists of an SR-latch which is set whenever a sample is received. The sample is at the same time loaded into a down-counter, and the SR-latch is reset when the counter reaches zero, and underflows. The resulting waveforms are shown in Figure 2.5. The shown Figure displays modulation on the trailing edge. Leading edge modulation is obtained by mirroring the carrier.

More complex modulation schemes can be employed to obtain double sided modulation. The nature of these are thoroughly described in [Nie98], however the basic properties are illustrated in Figure 2.6. This double sided modulation can be desirable as it reduces the distortion caused by UPWM. The main disadvantage in double sided modulation is that it requires a clock of twice the frequency required for single sided modulation. Schemes creating a pseudo double sided modulation have been developed as part of the Texas Instruments Equibit technology.

A further expansion to the UPWM modulator is three level modulation.

This modulation is described in [Nie98]. Three level modulation can be realized for both single and double sided modulation. The main advantage is that the EMI caused by the switching elements are reduced considerable.

The implementation of UPWM seems reasonable however it contains a limit on the allowable bit rate; the system clock for the counter. The clock frequency needed to obtain a given resolution at a given switch frequency grows exponentially with the bit resolution. This relation is given by equation 2.13.

$$f_{\text{system}} = 2^b \cdot f_c \tag{2.13}$$

The main disadvantages for UPWM are:

- For an audio signal from a CD (16 bit, 44.1kHz) a 2.89 GHz clock is required. If considering the high quality format available today this gets far worse; for DVD audio in it's best quality (24 bit, 192 kHz) over 3 THz would be required.

- The UPWM process is inherent unlinear, and thus creates harmonic distortion.

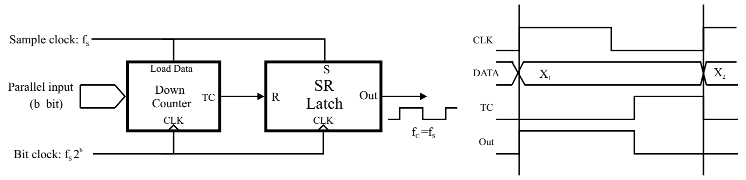

Figure 2.4: UPWM implementation (From [Nie98]).

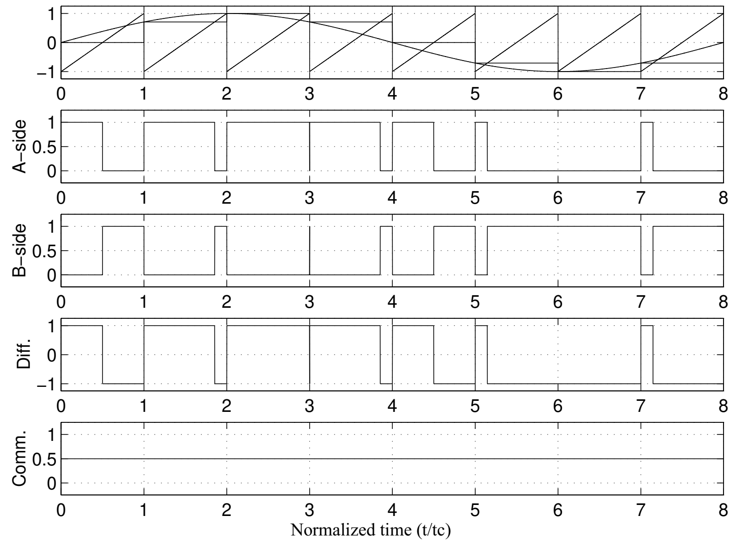

Figure 2.5: Single sided two level UPWM (From [Nie98]).

These problems have to be dealt with, the clock requirements have to be decreased, and the distortion reduced. The following sections describe methods to obtain these requirements.

2.3.2 Weighted Pulse Width Modulation (WPWM)

To improve the digital pulse modulation, different methods have been developed to approximate natural pulse width modulation which benefits from no harmonic distortion. These modulators are based on feed forward precompensation.

The precompensation is not necessarily required however it approximates the analog NPWM. This is an advantage as the NPWM has no harmonic distortion and the distortion caused by UPWM can thus be compensated. Many schemes have been developed for this throughout the time, among those can be mentioned Linear PWM, Weighted PWM and Pseudo Natural PWM. WPWM is an approximation of LPWM, but later research shows that LPWM and WPWM approximate NPWM equally well. The WPWM algorithm is preferable as it only uses additions and multiplications. This makes it easier to implement in hardware as divisions are hard to implement as they can only be approximated through several iterations.

To perform WPWM the input first has to be mapped from [-1 1] into [0 1] as the pulse width modulation is only valid for positive numbers. The mapping is shown in Equation 2.14. The WPWM works on two successive samples, c_1 and c_2 given by Equation 2.15 and Equation 2.16.

$$c(x) = 0.5x + 0.x5 \tag{2.14}$$
$$c_1 = c(x_n) \tag{2.15}$$
$$c_2 = c(x_{n+1}) \tag{2.16}$$

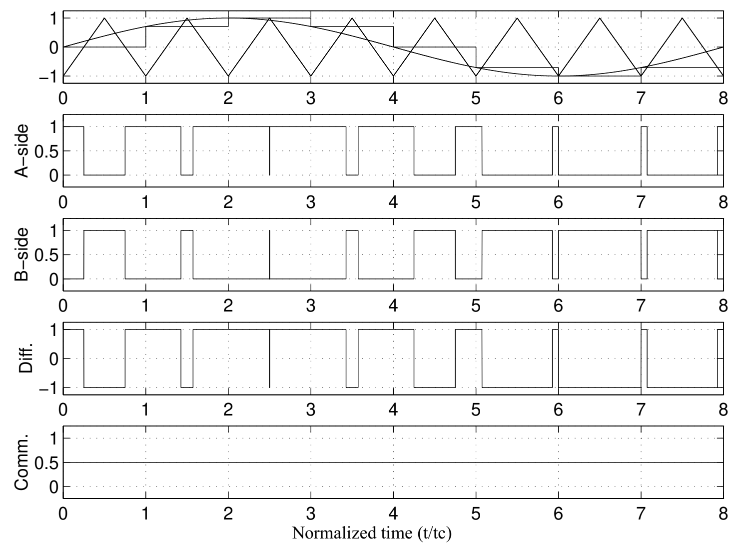

Figure 2.6: Double sided two level UPWM (From [Nie98]).

To simplify the expressions for WPWM the difference between the two samples is expressed as k, Equation 2.17.

$$k = c_2 - c_1 \tag{2.17}$$

The general expression for WPWM is shown in Equation 2.18. This expression can be shown to converge towards LPWM as i approaches infinity [JN99].

$$t_{p,n} = \sum_{i=0}^{N} c_1 k^i \tag{2.18}$$

With 5 or more iterations WPWM can be shown to be identical to LPWM within 16 bit precision. However this is not necessary as LPWM in itself is an approximation to NPWM. Instead it can be shown that 2 iterations are sufficient to obtain satisfying performance. This expression is shown in Equation 2.19.

$$t_{p,2} = c_1(1 + k + k^2) \tag{2.19}$$

To allow for hardware implementation within limited bit resolution elaborate schemes have been developed to avoid numerical cancellation. However these will not be treated here. These schemes, based on the two iteration WPWM, are currently undergoing development into a final product.

2.3.3 Noise Shaping

The basic function of the noise shaper is to maintain dynamic range within the baseband, while quantizing the signal to a lower resolution. Requantization is needed as the system clock required by UPWM grows exponentially with the number of bits in the output signal, as explained in Section 2.3.1.

The basic noise shaper layout is shown in Figure 2.7. It can be seen that the noise shaping resembles the deterministic dithering topology shown in Figure 2.16. The noise shaper is in fact a $\Delta\Sigma$ modulator with a multi-bit output.

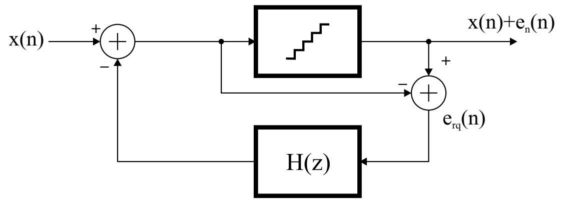

Figure 2.7: Noise shaping topology (From [Nie98]).

The signal transfer function (STF) can be determined for the noise shaper, it is shown in Equation 2.20. Similarly the Noise Transfer Function (NTF) can be determined. This is shown in Equation 2.21.

$$\mathrm{STF}(z) = 1 \tag{2.20}$$

$$\mathrm{NTF}(z) = \frac{E_n(z)}{E_{rq}(z)} = 1 - H(z) \tag{2.21}$$

This equation yields that the input signal passes the noise shaper unaltered while the quantization noise is modified by the function $H(z)$. By choosing $H(z)$ correctly the quantization noise can be suppressed.

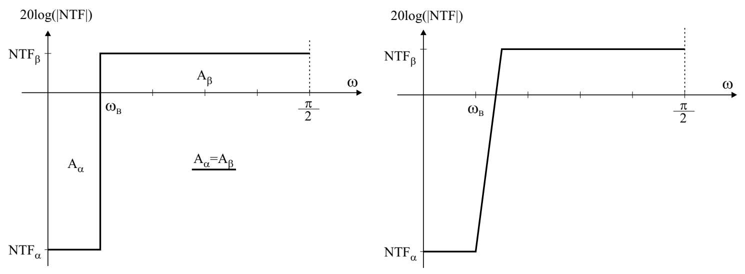

Figure 2.8: Noise Transfer Function, ideal and modified (From [Nie98]).

In [Nie98] it is shown that a filter of the form shown in Figure 2.8 satisfies this requirement. The basic requirement given by the Gerzon/Craven "optimal noiseshaping theorem" [Nie98], is that the area $A_\alpha = A_\beta$. To fulfill this requirement a minimum phase filter is needed. The second filter shown in Figure 2.8 is a modified version of the optimal filter which has a less steep slope, as an infinite steep slope requires a filter of infinite order. The levels NTF_α and NTF_β can then be determined:

$$\mathrm{NTF}_\alpha = 2^{b_{rq}-1}\sqrt{L\left(6D^{-1} - 2^{-2(b-1)}\right)} \tag{2.22}$$

$$\mathrm{NTF}_\beta = 2^{\left[\frac{-\omega_b}{\omega_s/2-\omega_b}\log NTF_\alpha\right]} \tag{2.23}$$

In these equations ω_b is the upper bandwidth limit, typically 20 kHz for audio, ω_s is the sampling frequency, L is the oversampling ratio, D the dynamic range, b_{rq} the number of requantized bits, and b the number of input bits.

The noise shaper currently used at ICEpower is using a 7^{th} order filter. This enables reproduction of audio in CD quality while requantizing to only 8 bits. The current ICEpower amplifiers are currently running at f_s=384 kHz and thus a system clock of 98.304 MHz is required. This is easily obtained in the digital circuits available today.

2.3.4 Complete Hybrid System

By combining WPWM, the noise shaper and UPWM a complete PCM→PWM converter is created. The system is seen in Figure 2.9. When applying modula-

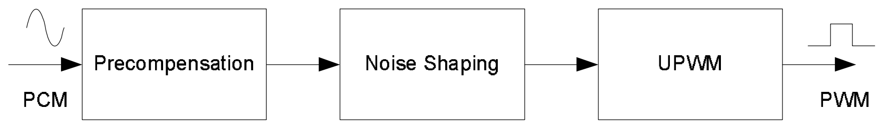

Figure 2.9: Scheme for PCM→PWM conversion.

tors based on precompensation and noise shaping oversampling (interpolation) of the signal is always used. This is because better linearity is obtained when oversampling the signal. Furthermore noise shaping can only be performed when excess bandwidth is available in the high frequency area. The signal is typically upsampled to $f_s = 384$ kHz$(= 8 \cdot 48k$ Hz).

This system is currently finding it's way into a product line from Sanyo Semiconductors.

2.4 digital Astable Integrating Modulator (dAIM)

Recent research has dealt with the use of 1 bit $\Delta\Sigma$ modulators for pulse width modulation. A $\Delta\Sigma$ derived modulator called dAIM has been developed, which provides comparable performance to the previous schemes used, using a simpler and easier perceivable modulation scheme. The basic structure for a first order dAIM modulator is shown in Figure 2.10. The structure of dAIM is in spite of the similarity to $\Delta\Sigma$ derived from the analog modulator AIM. The dAIM modulator will however be treated as a $\Delta\Sigma$ modulator here, as these are well described in literature.

For class D amplification the switch frequency of the $\Delta\Sigma$ output is typically too high. The dAIM modulator developed by Bang & Olufsen ICEpower A/S presents a simple work-around to this, which lowers the frequency. The basic layout of the dAIM is a $\Delta\Sigma$ with an added hysteresis loop around the quantizer. The difference between $\Delta\Sigma$ and dAIM is easily seen when comparing Figure 2.10 and the basic $\Delta\Sigma$ modulator in Figure 2.17.

These modulators have been evaluated both with and without oversampling, but yield the best results with oversampling, as excess bandwidth is needed similar to the noiseshaper.

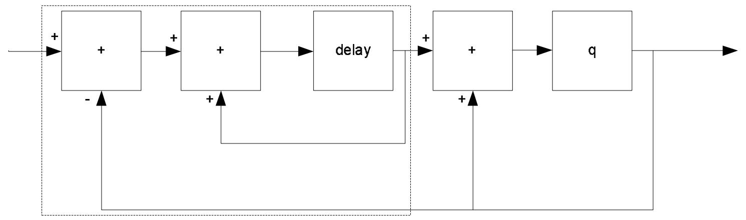

Figure 2.10: First order dAIM modulator.

To obtain better performance dAIM modulators of higher order have been considered, and currently a third order dAIM seems to offer the best trade off between complexity and audio quality. When referring to the order of dAIM, a multi loop configuration is considered. The order of the modulator is increased by cascading multiple integrators (the outlined part in Figure 2.10). The structure when cascading is shown in Figure 2.11.

In this figure the dAIM modulator is further expanded from the basic modulator by including the G-factors. These factors are usually chosen as fractions of two as this allows for the use of shift operations instead of dedicated multipliers. The G-factors are quite essential to the dAIM as they control the operation of the modulator. In [Kje03] it is shown that an increase of the G-factors cause an increase in the signal to noise ratio, however an increase in switching frequency is also obtained. Thus the G-factors should be chosen as a trade off between the maximum allowable switching frequency, and the required dynamic range.

Using the z-domain dAIM can be described by deriving the signal and noise transfer functions like for the noise shaper. These functions are shown in Equation 2.24 and 2.25.

$$\mathrm{STF}(z) = \frac{Y_x(z)}{X(z)} = \frac{G}{1+(G-2)z^{-1}+z^{-2}} = \frac{z^2 G}{z^2+(G-2)z^1+1} \tag{2.24}$$

$$\mathrm{NTF}(z) = \frac{Y_e(z)}{X(z)} = \frac{1-z^{-1}}{1+(G-2)z^{-1}+z^{-2}} = \frac{z(z-1)}{z^2+(G-2)z^1+1} \tag{2.25}$$

A corresponding expression can be derived for higher order dAIM modulators. For third order dAIM they are:

$$\begin{aligned}\mathrm{STF}(z) &= \frac{Y_x(z)}{X(z)}\\ &= \frac{G_1G_2G_3}{1+(-4+G_1G_2G_3+G_1G_2+G_1)z^{-1}+(6-G_1G_2-2G_1)z^{-2}+(-4+G_1)z^{-3}+z^{-4}}\\ &= \frac{G_1G_2G_3z^4}{z^4+(-4+G_1G_2G_3+G_1G_2+G_1)z^3+(6-G_1G_2-2G_1)z^2+(-4+G_1)z+1}\end{aligned} \tag{2.26}$$

$$\begin{aligned}\mathrm{NTF}(z) &= \frac{Y_e(z)}{X(z)}\\ &= \frac{\left(1-z^{-1}\right)^3}{1+(-4+G_1G_2G_3+G_1G_2+G_1)z^{-1}+(6-G_1G_2-2G_1)z^{-2}+(-4+G_1)z^{-3}+z^{-4}}\\ &= \frac{(z-1)^3z}{z^4+(-4+G_1G_2G_3+G_1G_2+G_1)z^3+(6-G_1G_2-2G_1)z^2+(-4+G_1)z+1}\end{aligned} \tag{2.27}$$

These expression are quite complex but nonetheless useful for understanding the dAIM modulator. These expressions have the same basic properties as the noise shaper, where baseband noise is suppressed at the cost of the high frequency noise, which increases. Estimating the noise caused by the dAIM modulator is unfortunately quite complicated as a 1 bit quantizer is used. This prevents the use of white noise models, which are not valid at coarse quantization. Another noise estimate thus has to be used.

The dAIM differs from the hybrid modulators by being a complete integrated modulator, and thus seems to be a more elegant solution. The dAIM and the

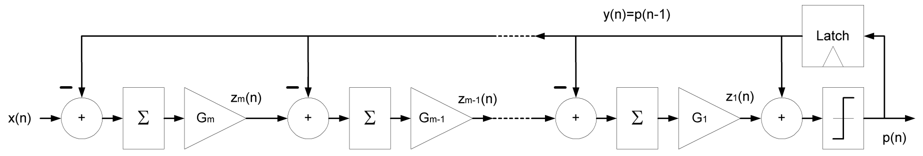

Figure 2.11: General dAIM structure. From [Kje03]

hybrid modulators do however have many common properties as they both contain $\Delta\Sigma$ elements to allow for "lossless" quantization. Furthermore it is less complex than many hybrid modulators, e.g. WPWM. All the properties of dAIM are not explored fully, yet, however a great deal of research is currently done at Bang & Olufsen ICEpower A/S. The dAIM modulator is described in detail in [And03, Kje03].

To illustrate the behavior of dAIM two FFT plots are shown in Figure 2.12. The noise shaping properties of dAIM are easily seen with a very low noise floor at low frequencies, with the level increasing with frequency. The G-factors used are: $G_1 = 2^{-6}$, $G_2 = 2^{-7}$ and $G_3 = 2^{-8}$. If the system is plotted with a logarithmic frequency axis, the noise floor wil have a linear progress, which slope will be determined by the order of the modulator. For the 1$^{\text{st}}$ order it will be 20 dB per decade, 40 db per decade for the 2$^{\text{nd}}$ order and so forth. The performance for the simulation shown is a THD+N of 88 dB (0.04 %). According to [Kje03] this yields a dynamic range of 112 dB within the audio band.

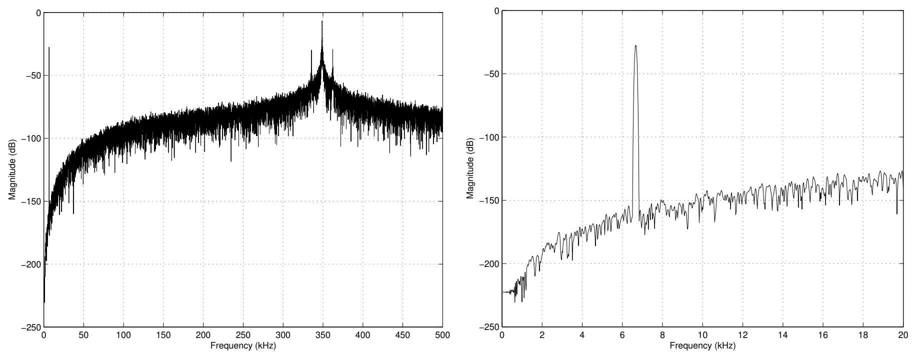

Figure 2.12: Spectrum of dAIM output, input 6.67 kHz, M=0.1, f_s=384 kHz. Left: Wide band plot, Right: Narrow band plot

2.5 Interpolation

Typically a signal is sampled at a frequency slightly higher than two times the maximum frequency. This is required to reconstruct the data fully without having redundant data. The frequency is slightly higher than the Nyquist frequency, given by two times the maximum frequency, to allow for a filter with a finite slope to remove the aliasing from the sampling frequency. The audio CD's sampling frequency is derived from these requirements, with a sampling frequency of 44.1 kHz, which is slightly higher than two times the bandwidth (20 kHz).

The low frequency overhead requires ideally a brick wall filter with infinite slope, however this is not possible. Instead the choice is a filter which within half the sampling frequency attenuates the signal to the noise level of the converter.

A major problem with this approach is that a steep analog filter is expensive to implement. With the progress obtained in Very LArge Scale Integration (chip technology) (VLSI) it is often attractive to solve the problem in the digital domain instead. This is done by oversampling the signal. This increases the range between the maximum audible frequency and $f_s/2$, and thus allows for a shallower filter. When considering 1-bit D/A converters oversampling ratios of $256 \cdot f_s$ are not uncommon.

Another property of the over sampling is an increase in resolution. The noise level of the quantizer is given by:

$$Q_n = \int_{-q/2}^{q/2} e^2 \, de = \frac{1}{3q} e^3 |_{-1/2}^{q/2} = \frac{q^2}{12} \tag{2.28}$$

In this equation q represents the quantizer's step size, and e is the quantization error which is assumed as having a uniform distribution.

If the noise is assumed to be white it will be equally spread out in the frequency spectrum, and the noise in the baseband is given by:

$$Q_b = \frac{q^2 \left(f_s/2\right)}{12 \left(f_{\mathrm{ovs}}/2\right)} \tag{2.29}$$

If for instance an oversampling ratio of 4 is chosen the following noise level will be achieved:

$$Q_{\mathrm{ovs}} = \frac{q^2 \left(f_s/2\right)}{12 \left(4 f_s/2\right)} = \frac{\left(q/2\right)^2}{12} = \frac{Q_N}{4} \tag{2.30}$$

And the resolution has thus been improved by one bit.

Even though the example shown here is based on, as we will see later, unrealistic assumptions regarding the noise, it illustrates the basic properties of oversampling.

Oversampling is further advantageous when used in combination with the hybrid scheme shown earlier. First of all oversampling is required to perform noise shaping as the noise is moved into the excess bandwidth. Furthermore the linearity of the conversion is increased as the carrier frequency to bandwidth ratio is increased. The main disadvantage in digital amplifiers is that the efficiency reduces with the switch frequency, and a switch frequency of above 500 kHz is not recommendable [Nie98]. The ratio typically used at Bang & Olufsen ICEpower A/S is 4 or 8 according to the input, to obtain a 384 kHz sampling frequency for the WPWM. A further limitation on the oversampling ratio used is the system clock frequency as it increases proportional to the oversampling ratio.

2.6 The analog approach to digital amplification

To ensure correct reproduction of the modulated signal, through the power switches, error correction is needed. The typical approach used by many manufacturers is a feed forward system where the parameters of the power stage are determined and used to design a digital precompensation system, which corrects the errors caused by the power stage. This approach is unsuitable, as it either requires well specified, and thus expensive components, or alternatively a calibration of the precompensation system in each amplifier. An additional disadvantage is that the specifications of components tend to drift when the amplifier ages, and the error compensation thus gets ineffective, or even worse, add additional distortion.

At Bang & Olufsen ICEpower A/S a different strategy for error correction of the power stage has been chosen. A control system called Pulse Edge Detection and Error Correction (PEDEC) is used to form a local closed loop around the power stage itself while the digital modulator is not included in the loop. The basic operation of PEDEC can be seen from Figure 2.13.

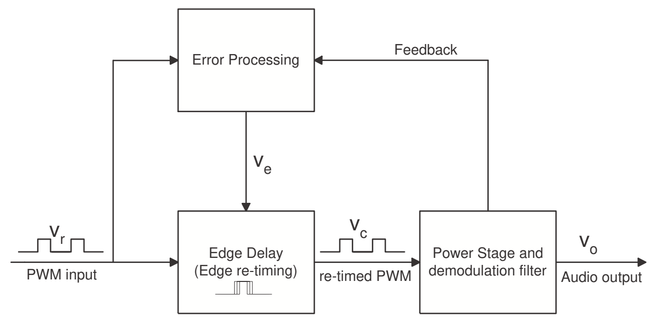

Figure 2.13: Block diagram of PEDEC control system, from [MA03].

The PEDEC system works by re-timing the pulses to compensate any error occurring. This is done by the ED unit, which is fed by the v_e signal. The v_e signal is created by comparing the output and the input of the power stage, which is both pulse trains. From these two signals the error can be determined, and should ideally be zero when no error occurs.

$$K_{PEDEC} = 2\frac{t_0}{t_p}\frac{V_C}{V_I}, \text{ for } -V_I \leq v_e \leq V_I \tag{2.31}$$

The gain in the edge delay unit is given by Equation 2.31, where t_p is the period time of the pulse train, and t_o is the rise and fall times of the edges in the edge delay signal. V_I is the maximum amplitude of the edge delay signal, and V_C is the maximum amplitude of the output of the edge delay unit.

Three PEDEC topologies currently exist, VFC1, 2 and 3, where VFC3 is the most relevant as it includes the demodulation filter in the control loop. The operation of VFC3 can be seen in Figure 2.14.

The compensator block is given by Equation 2.32. In this expression the zeros and poles are determined by the requirements of the system. Two zeros are used to cancel the effect of the demodulation/reference filter. Two poles are used to limit the bandwidth within the loop. The exact placement of these poles may vary depending on whether a two or a three level modulator is used, as more attenuation of the switch frequency is recommended for two level. The final pair of pole / zero is used as a lag compensator.

$$C(s) = K_c\frac{(\tau_{z1}s+1)\cdot(\tau_{z2}s+1)\cdot(\tau_{z3}s+1)}{(\tau_{p1}s+1)\cdot(\tau_{p2}s+1)\cdot(\tau_{p3}s+1)} \tag{2.32}$$

The A block is given by Equation 2.33, and is used to scale the feedback down to a size similar to the reference signal.

$$A(s) = 1/K \tag{2.33}$$

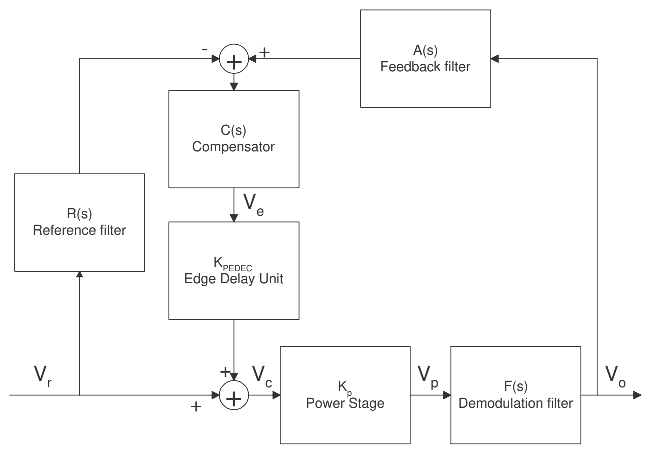

Figure 2.14: Block diagram of PDEC, VFC3. From [MA03]

The transfer function of power stage and edge delay unit is given by Equation 2.34, which is just a multiplication of the Edge delay unit given by Equation 2.31, and the gain in the power stage.

$$B(s) = K_{PEDEC} K_p \tag{2.34}$$

The transfer function for both demodulation and reference filter is given by Equation 2.35 and 2.36. Those filters are standard 2$^{\text{nd}}$ order filters.

$$R(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.35}$$

$$F(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.36}$$

All these transfer functions lead to the open loop function given by Equation 2.37.

$$L(s) = C(s)A(s)B(s)F(s) \tag{2.37}$$

If the system is modified so that $K = K_p$ (the attenuation in the A block equals the gain in the power stage), and $F(s) = R(s)$ (the reference filter and the demodulation filters are equal), the transfer function shown in Equation 2.38.

$$H(s) = F(s)K_p \tag{2.38}$$

This transfer function is ideal as it only consists of a power gain K_p and a lowpass filter, $F(s)$.

To avoid high frequency noise the PEDEC control system is often modified to accept two inputs; a pulse signal and a delayed pulse signal. The delayed pulse signal is typically digitally delayed, where the delay is adjusted to resemble the delay in the power stage. This principle is shown in Figure 2.15.

Further details on the system can be found in [Nie98, MA03].

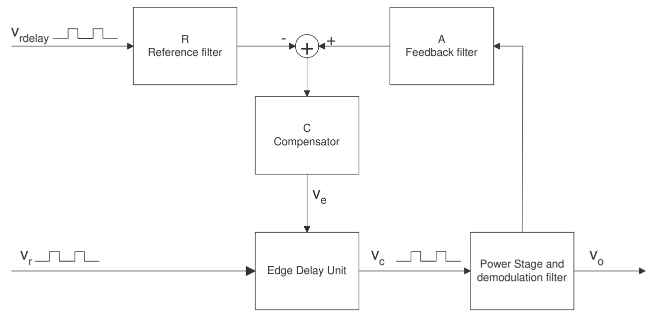

Figure 2.15: Block diagram of PEDEC with delayed delayed input. From [MA03]

2.6.1 Performance

The effect of the PEDEC control system is easily illustrated by a few measurements. The measurements shown here are all taken from [And02]. As stated above, the main function of PEDEC is to reduce the THD, so let us take a look at some THD measurements.

When comparing the THD+N measurements from the amplifier with, and without control, shown in Figure B.1 and B.2, it is obvious that the PEDEC system is required for a satisfying performance. With the PEDEC system the THD+n stays well below 0.05 % within moderate levels while it peaks at 1 % without control.

Similarly, the frequency response is affected by the control system. When comparing the frequency responses shown in Figure B.3 and B.4 the PEDEC has far better performance than the uncontrolled system, where the PEDEC controlled amplifier offers far better linearity. A point should be made to the y-axis of the Figure B.3 and B.4 which are scaled differently.

There are many other audio measures which are not shown here, as PEDEC only has limited influence on these parameters.

2.7 $\Delta\Sigma$-modulation

$\Delta\Sigma$-converters has won a strong place in conversion between digital and analog domains. This is due to the nature of $\Delta\Sigma$ modulators which trades precision in levels of signal amplitude for timing precision. This trade is highly desirable as it is far easier to obtain precise timing in the VLSI technologies used today.

The possibility for a 1 bit output of the $\Delta\Sigma$ modulator makes it very interesting for controlling the power switches in a class D amplifier as well, and thus create a power D/A converter. $\Delta\Sigma$ derived technologies are used in most digital input class D amplifiers, besides the noise shaper and dAIM they are used for similar purposes in products from other companies. The Equibit modulator from Texas Instruments is for instance based on a noise shaper.

An important measure when designing an amplifier is the noise. The noise caused by a $\Delta\Sigma$ modulator origins from the quantizer. The common assumption for quantization noise has been to consider it white, however this is not valid for ΔΣ modulators for a number of reasons.

This section presents a short introduction to ΔΣ-conversion, which highlights the main aspects. Furthermore a summary of the leading strategies for assessing noise is presented. As the difference between A/D and D/A conversion is subtle, papers describing both are used as sources for this report.

As shown in Section 2.5, the baseband noise can be reduced considerable by the use of oversampling, and the signal could ideally be quantized to one bit if sufficient oversampling is applied. When quantizing a signal it is shown in [Gra90] that adding noise to the input signal, through dithering it, can improve the perceived audio quality. This noise source should be an i.i.d., independent source.

The ΔΣ modulator can be explained through the dithering idea. The basic idea is to use the quantization noise as noise source for dithering the input. This replaces the i.i.d. source with a source, deterministic dependent on the input. This is shown in Figure 2.16. This basic structure can be rewritten

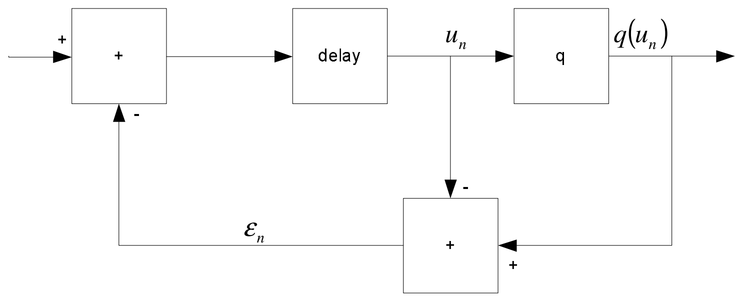

Figure 2.16: Deterministic dithering.

into the well known ΔΣ modulator, which is shown in Figure 2.17. This basic

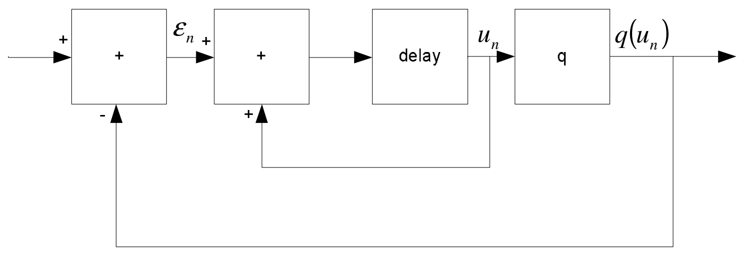

Figure 2.17: First order ΔΣ modulator.

modulator has the property that the input signal passes right through while the added noise signal is high pass filtered. This filtering suppresses the noise in the baseband, and adds 1.5 bit resolution in the first order case and 2.5 in the second order modulator [SP98]. As mentioned before the assumption of white noise is not valid, but it offers the possibility of a simple estimate of the enhancement obtained when applying ΔΣ-modulation.

2.8 Noise modeling in $\Delta\Sigma$-modulators

The basic white noise model used above is excellent for understanding the basic properties of $\Delta\Sigma$ modulation, however the assumption of white noise usually does not hold true. In [Gra90] it is argued that this assumption is a fairly good approximation if

1. The quantizer does not overload.
2. The quantizer has a large number of levels.
3. The distance between the levels is short.
4. The probability density of pairs of input samples is given by a smooth density function.

It is further argued that these demands are violated for oversampling $\Delta\Sigma$ modulators because

1. It's often unknown if the quantizer will overload, with an input within a defined range.
2. The quantizer typically has few levels.
3. The bin width is typically large.
4. The feedback applied prevents the quantizer input from having smooth density functions.

These rules limit the use for the white noise model. It might be suitable for multi-bit converters like the noise shaper applied in WPWM, but for single bit converters it is definitely of very limited use.

The quantization noise can be divided into two parts; granular noise which occurs when the quantizer is operating within its boundaries, and overload noise which occurs whenever the input exceeds the boundaries of the quantizer. As the overload noise is very hard to estimate the $\Delta\Sigma$ modulators are usually limited to the non-overloading region. Thus most scientific publications on $\Delta\Sigma$-modulation are concerned with granular noise.

To avoid the shortcomings of the basic noise model applied above, other methods of noise estimation are examined. These methods are:

- Models based on a specific input signal.
- Models based on an input signal combined with noise.

The first type is typically developed for DC [Gra89, Gra90] and sinusoidal [RMGW89, Gra90] inputs. The models are handled by either difference equations [Gra89, RMGW89, WCG89, NL94] or fourier series [Gra90, RL94]. These input options are somewhat limited but corresponds well to the input signals used when evaluating audio circuits by measurement.

The second types are based on an arbitrary signal with some additional i.i.d. noise at the input [Gal93, Gal94].

2.8.1 Input signal determined noise models

Determining noise models from deterministic input signals are well treated in [Gra90, Gra89, RMGW89], where models are created for the single loop ΔΣ modulators. The main shortcoming of these papers are the lack of theory for modulators of a higher order than one. A general expression for 2^{nd} order modulators are created in [Gra90], but the developed expression is only valid for quantizers with at least 2 or more bits, and thus not usable for one bit converters. Models for higher order modulators are developed in [WCG89].

The following text is a summary of these papers which treats the main aspect of the developed models, for more information please refer to the papers. All of the theory assume that the quantizer is operating within its boundaries, and is thus not overloaded.

The work in [Gra90] is based on a comparison of the uniform quantizer and ΔΣ modulators. The moments of the error sequences from both functions are compared. To do this comparison the fourier series are developed in order to determine the 1^{st} and 2^{nd} order moments. If these two moments match the moments of a uniform quantizer, the quantizer noise is considered to be white as the uniform quantizer operates well within the boundaries where it can be considered white. The basic error function for the quantizer can be written as Equation 2.39. In this function u represents the input, Δ the distance between two output levels and ϵ is the error function.

$$e = \frac{\epsilon}{\Delta} = \frac{1}{2} - \left\langle \frac{u}{\Delta} \right\rangle \tag{2.39}$$

The $\langle x \rangle$ is a fraction operator commonly used in quantization theory, it returns the fractional part of x. As can be seen from the equation, the quantization error is only dependent on the step size and input signal.

Gray proceed to develop the noise models for deterministic inputs. The first input treated is the DC case. In these calculations the quantizer input, u_n has been replaced with $s_n = n\beta$, where β is given by Equation 2.40.

$$\beta = \frac{1}{2} + \frac{x}{\Delta} \tag{2.40}$$

At first the DC signal may seem like a poor choice for a test signal. The argument for using a DC is that at high interpolation factors a DC signal resembles a slowly varying signal. Thus the DC signal can be used for noise estimation on a wide range of signals as long as they are oversampled sufficiently.

For the DC input the moments of the noise are determined in [Gra90], the result is shown in Equation 2.41 and 2.42:

$$\overline{E}\{e_n\} = \quad 0 \tag{2.41}$$
$$\overline{E}\{e_n^2\} = \quad \tfrac{1}{12} \tag{2.42}$$

The moments agree with the uniform assumption, however when regarding the 2^{nd} order properties in Equation 2.43 it is according to [Gra90] obvious that the noise is non-white as the exponential component indicates that the spectrum is discrete rather than continuous.

$$\begin{aligned} R_e\left(k\right) &= \sum_{l\neq 0}\left(\frac{1}{2\pi l}\right)e^{j2\pi lk\beta} \\ &= \frac{1}{2}\frac{1}{\pi^2}\sum_{l=1}^{\infty}\frac{\cos\left(2\pi lk\beta\right)}{l^2} \\ &= \frac{1}{12}-\frac{\langle k\beta\rangle}{2}\left(-\langle k\beta\rangle\right) \end{aligned} \tag{2.43}$$

Through investigation of Equation 2.43 it can be found that the noise spectra has the amplitude S_n seen in Equation 2.44, at the frequencies $\langle n\beta\rangle$ given by Equation 2.45.

$$S_n = \begin{cases} 0; & \text{if } n = 0 \\ \frac{1}{(2\pi n)^2}; & \text{if } n \neq 0 \end{cases} \tag{2.44}$$

$$\langle n\beta\rangle = \left\langle n\left(1\frac{1}{2}+\frac{x}{\Delta}\right)\right\rangle \tag{2.45}$$

For sinusoidal inputs an input of the form $A\cos n\omega_0$ is considered, where its A is considered to be less than the maximum input, b. Corresponding expressions are made for s_n

$$s_n = \sum_{i=0}^{n-1}\left(\frac{1}{2}+\frac{x_i}{\Delta}\right) = \frac{n}{2}+\frac{A}{2\Delta}+\alpha\sin\left(n\omega_0-\frac{\omega_0}{2}\right) \tag{2.46}$$

This expression leads to

$$S_{(m,1)} = \left(-1\right)^m c_e\left(m\right)^2 \tag{2.47}$$

$$S_{(m,2)} = \left(-1\right)^m c_0\left(m\right)^2 \tag{2.48}$$

$$\lambda_{(m,1)} = \left\langle m\tfrac{\omega_0}{2\pi}\right\rangle \tag{2.49}$$

$$\lambda_{(m,2)} = \left\langle m\tfrac{\omega_0}{2\pi}-\tfrac{1}{2}\right\rangle \tag{2.50}$$

c_e and c_0 are both given by quite complex functions, which can be found in [Gra90]. The main purpose of 2.47 and 2.48 in this report, is to show the origin of the simplified expression. Equation 2.47 and 2.48 can be simplified by setting the amplitude of the sine to the maximum allowable input, $A = b$. The result of this simplification is seen in Equation 2.51 and 2.52. Where the first gives the amplitude, and the second, the frequency.

$$S_m = \begin{cases} \frac{1}{2} & \text{when } m = 0 \\ \left(\frac{1}{\pi}\sum_{l=1}^{\infty}\frac{J_m(2\pi\alpha(2l-1))}{2l-1}\left(-1\right)^1\right)^2 & \text{when } m \text{ is even} \\ \left(\frac{1}{\pi}\sum_{l=1}^{\infty}\frac{J_m(4\pi\alpha l)}{2l}\left(-1\right)^l\right)^2 & \text{when } m \text{ is odd} \end{cases} \tag{2.51}$$

$$\lambda_m = \begin{cases} \left\langle m\frac{\omega_0}{2\pi}-\frac{1}{2}\right\rangle & \text{when } m \text{ is even} \\ \left\langle m\frac{\omega_0}{2\pi}\right\rangle & \text{when } m \text{ is odd} \end{cases} \tag{2.52}$$

In these equations J_m denotes the mth order bessel function. The expressions for the sinusoidal case unfortunately contain infinite sums. However they do converge and plots of spectra for different inputs are shown in [Gra90].

2.8.2 i.i.d. based noise modeling

The i.i.d. (indefinite independent distribution) noise modelling is based on a study of not only the ΔΣ modulator but also the subsequent filter. This fact limits the use for evaluating the modulator only, in a class D amplifier. Instead it considers the entire system from input to demodulation filter. In a class D amplifier this is further complicated by the presence of the power converter between the modulator and the demodulation filter. This consideration somewhat limits the use however some interesting results are offered in [Gal93] which offer a closed form expression for the noise in a first order modulator when applying a sinusoidal input.

2.8.3 Noise in multistage modulators

Most ΔΣ modulators are of higher order than one, and it is thus required to expand the models further to get a reliable noise estimate. Work on this is done in the deterministic case by Chou [WCG89], and by Galton in the i.i.d. case [Gal94].

For multistage modulators the best solution is offered by Galton. The solution presented in [Gal94] offers a general solution applicable to most generic ΔΣ modulators. The expression for the entire output spectrum is shown in Equation 2.53 where $S_{xx}\left(e^{j\omega}\right)$ is the spectrum of the modulators input and $S_{ee}\left(e^{j\omega}\right)$ is the spectrum of the output, given by Equation 2.54. In this expression Δ is a matrix of the step sizes for each quantizer in the modulator, and N is a matrix of transfer functions connecting each stage of the modulator. N is given by Equation 2.55. K is the order of the modulator.

$$S_{yy}\left(e^{j\omega}\right) = S_{xx}\left(e^{j\omega}\right)\left|S\left(e^{j\omega}\right)\right|^2 + S_{ee}\left(e^{j\omega}\right) \tag{2.53}$$

$$S_{ee}\left(e^{j\omega}\right) = \sum_{k=0}^{K}\frac{\Delta_k^2}{12}\left|N_k\left(e^{j\omega}\right)\right|^2 \tag{2.54}$$

$$N(z) = U(z)\left(I - G(z)\right)^{-1} \tag{2.55}$$

In this expression G and U are matrices which can be found in the genric ΔΣ modulator which is show in Figure 2.18. This figure is derived from another

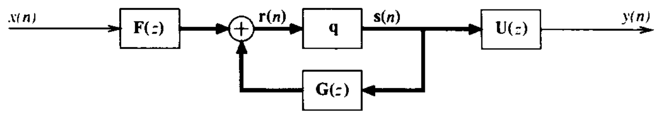

Figure 2.18: Generic ΔΣ modulator of arbitrary order, and configuration. From [Gal94].

generic ΔΣ modulator, shown in Figure 2.19. The relation between these two modified ΔΣ modulators is quite simple, the U matrix is the same, and the relation between F, G and T is given by $T(z) = [F(z)\,|G(z)]$.

The advantage of these generic modulators is that many configurations can be described using them. The author has an example where a cascade modulator consisting of a double loop and a single loop is described using these topologies.

2.8.4 Digital limitations

Another source for noise is the limited resolution used for arithmetics in hardware. Typically the resolution used is 24-bit fixed point, which is considered enough for digital audio. These sources are discussed in [Won90, JdlRRV99, ASVL99]. During the project finite resolution will not be treated, as the simulator are already designed to handle this. Furthermore it has proven successful to use 24 bit fixed point resolution for audio applications.

Finally, jitter offers another source which adds noise to the system. This noise is typically seen as errors in the exact placement for the pulse transitions. Jitter in DPMAs is described in detail in [Hio94]. It is however not possible to design jitter resistant digital audio circuitry, thus the system clocks used in this project will be assumed jitter free.

2.9 Audio measures

To determine the "quality" of the audio reproduced by an amplifier some measures have to be introduced. These measures origin from both audio and telecommunications industry, where they have been used for a long time with no changes. It can be argued that these measurements does not relate very well to the perceived quality. To alter this different algorithms have been developed, which estimate the perceived quality by using psycho acoustical models. These algorithms are not treated further here as these measurements are not available for the amplifiers used for comparison. Furthermore they are not publicly available but requires licensing. More information on this subject can be found in [Kje03]. The measures treated here are all classic measures used whenever measuring the specifications for audio equipment. For more information on measuring audio specifications please refer to [Boh00].

Fast Fourier Transform

The Fast Fourier Transform is well known in signal processing. It transforms a time domain signal to frequency domain. The FFT is usually used to obtain the spectrum from a given signal; eg. the output of a amplifier. The FFTs presented in this report are obtained by averaging 4 times. This gives a smoother surface where tonal components are easier to identify.

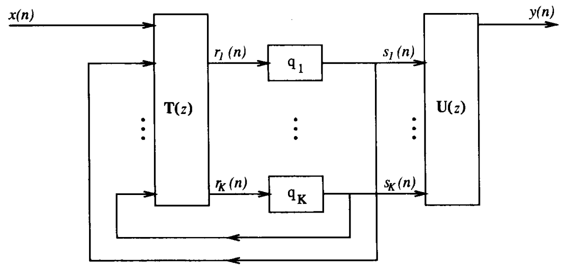

Figure 2.19: Generic $\Delta\Sigma$ modulator. From [Gal94].

Another important property of the FFT is the frequency resolution, which the leads to lower noise floors as the resolution increasesthe bin width decreases, and less energy is contained in each bin. The resolution is unfortunately not similar for all FFTs in this report.

Frequency response

The frequency response is also known as the bandwidth. It is measured by applying a frequency sweep to the input, and the output amplitude is measured in dB referred to the amplitude at 1 kHz, and the bandwidth is specified as well as the amplitude margins used.

Dynamic range

The dynamic range is calculated by measuring the maximum output voltage and the amplitude of the noise within the audio band. A ratio between these measurements are then calculated, and the result is expressed in dB. The dynamic range is usually measured at 1 kHz.

In digital audio the system is often supplied with a signal at -60 dB as digital audio systems often closes down at no input, and thus gives a false impression of the noise output.

Total Harmonic Distortion

The Total Harmonic Distortion (THD) is given by the total amplitude of all harmonic distortion within a certain bandwidth. The THD is interesting as it is related to the nonlinearity of the amplifier. The THD is often calculated from a spectrum, e.g. obtained by FFT.

THD+Noise

Instead of THD, THD+Noise (THD+N) is often measured. The THD+N is determined by summing all signal components excluding the fundamental tone. The THD+N measure is often used as it includes all contributions from the amplifier, and not just harmonic distortion.

Intermodulation (CCIF)

The intermodulation measure (IMD) is used to determine nonharmonic nonlinearities. There are several methods for determining intermodulation. The method described here is the one recommended by International Telephonic Consultative Committee (CCIF). It is measured by applying two tones spaced with 1 kHz, and with equal amplitude. Then intermodulation can be measured by summing the contributions from the occurring intermodulation components. The ratio between the intermodulation components and the fundamental is finally calculated, and expressed as a percentage.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is a measure that indicates the influence of a badly regulated supply on the amplifiers output. It is measured by measuring the signal perturbing the supply, and the resulting signal on the amplifier output. The ratio is then determined and expressed in dB.

2.10 Object of this thesis

The basic goal of this project is to eliminate the use of analog control of the power stage by moving the required control system into the digital domain. Similarly the use for WPWM in hybrid modulators should be obsolete if proper regulation is applied. The main reason for this is to minimize implementation costs by integrating the modulator and the control system in the same IC (Integrated Circuit), whereas the modulator and the control system are located in two different ICs in the current hardware generation. The simplification of the system furthermore allows the use of DPMA (Digital Pulse Modulating Amplifier) in applications where it has not been possible due to both cost and size.

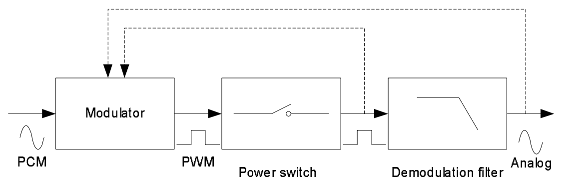

Figure 2.20: Basic layout for feedback system.

The feedback system designed during this project should be sufficient to minimize any distortion to a reasonable level, without being unnecessary complex. In practice the amplifier should thus yield performance comparable to the current amplifier based on PEDEC.

To evaluate different schemes the simulator developed by Kjeldsen [Kje03] should be used. This simulator is easy configurable and able to simulate most aspects of a digital amplifier, however two important aspects are left out. The simulator lacks the ability to estimate the noise caused by modulation, and it lacks the ability to simulate the unlinarities in a power stage. These two blocks should be implemented to allow for simulation on the entire system.

The main aspect when creating the power stage simulation block is to identify the main contributors to the distortion. Here the blanking delay and the power supply perturbations are obvious contributors. But other contributors like parasitic capacitance and resistance in the circuit should be evaluated as well to obtain a simulation sufficiently close to reality.

When the simulator is complete the development of feedback topologies can commence. The first task should be to decide what and how much information should be fed back into the digital domain. This could be restricted to timing information on the pulse edges or it could be more complex data like the demodulated output sampled at high resolution. Or combinations of the two mentioned here. The basic possibilities are shown in Figure 2.20 where the feedbacks are shown with dotted lines. A more detailed strategy is shown in Figure 2.21. This figure illustrates two types of feed back, a simple where the

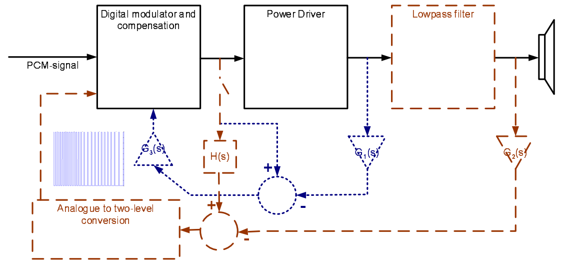

Figure 2.21: Basic layout for feedback system.

signals taken after the power stage, and a more advanced, where the demodulated signal is used in the feedback.The simple feedback's main advantage is that the signal is in "pulse domain". The disadvantage is that the signal taken here can only be used for correction of pulse timing errors. The advanced feedback benefits from the ability to correct both pulse timing and amplitude errors, and can thus correct all types of errors in a pulse modulated amplifier.

The feedback systems should be evaluated during the development on the classic measures used in audio. These are among others dynamic range, THD + noise and intermodulation. This evaluation should be used to determine whether a specific feedback topology is suitable.

Chapter 3

Power stage modeling

To evaluate the impact of an error compensating algorithm a model of the system is required. This model should be sufficiently precise but at the same time not too precise. This trade off is made to obtain usable simulations in respect to both the time spend making the simulation, and the precision of the result in respect to the object that is being modelled. Another part of this model design is to choose a simulation tool suited for the task at hand.

This chapter is both an evaluation of simulation tools and power stage models. The main goal is to determine a simulation method sufficiently advanced to support the development of feedback control systems.

3.1 Simulation Tools

The simulation methods considered are MATLAB^{TM} simulation using both the Simulink toolbox, and MATLAB scripts. The Simulink toolbox benefits from an easy perceivable environment where the transitions between continuous and discrete time are handled easily, and whole systems can be implemented as block diagrams. The main disadvantage for Simulink is another aspect of the user friendliness; it is difficult to master the calculations performed "behind the scenes", and thus control the accuracy of simulation versus simulation time trade off. This usually results in quite good simulation results which are, unfortunately, painfully slow to obtain.

MATLAB simulations using scripts are opposite of Simulink. The user is in total control of the simulations, and thus the calculations performed, however the user has to determine the exact equations for the system. This can be tedious, especially when considering dual-domain systems with transitions from digital to analog. The extra amount required by the scripts pays off in improved simulation times.

PSpice is a program designed for simulation of analog circuitry. It's basic function is to determine the differential equations of an electronic system, and solving them numerically taking sufficiently small steps to obtain usable result, in the same manner as Simulink solves differential equations. PSpice is ideal for simulating the power stage as it can easily model an electronic system in a way which is very close to the reality. This means that not just a few error sources can be included. Instead all can be included, even the more insignificant, just by applying sufficiently complex models. The main disadvantage is that it is hard to model discrete time components in PSpice.

An ideal solution to the simulation problems would be to make a model part MATLAB, part PSpice, allowing for the best of two worlds. This integration is unfortunately impossible.

3.2 Modeling the modulator

The ideal way to implement the modulator would be to directly apply the source files developed in [Kje03] directly into Simulink. Preferably into a plug-in structure which allows the modulator to be replaced easily. This is unfortunately not possible. Simulink allows the user to implement custom blocks through the “S-functions” (System function) which allows for implementation of Matlab code. The structure of these S-functions is unfortunately quite different from the structure of standard Matlab functions. Another and more serious disadvantage is that the use of S-functions based on Matlab code slows the simulation. This is due to the fact that Simulink calls a Matlab code interpreter in each simulation step. There are two methods to avoid this problem. The first is to create the S-function for the modulator using c-code. The second is to implement the modulator using standard Simulink blocks. These blocks can then be combined into a subsystem which has the same function as the S-function. Unfortunately neither of these options allow for direct implementation of the source code from the simulator made in [Kje03].

For the initial simulations a 3$^{\text{rd}}$ order dAIM modulator implemented using standard Simulink blocks was used. A further advantage was that this model was readily available from Bang & Olufsen ICEpower A/S.

3.3 Simple simulation using Simulink

The first simulation attempted is based on Simulink. It features the two main error contributors, blanking delay and power supply perturbations.

The blanking delay has been implemented by replicating the incoming pulse signal. The replica is then delayed according to the required blanking delay. The original and the delayed replica is finally added. This generates a three level signal where the zero-level represents the blanking delay where *all* switching elements are off. The principle is shown in Figure 3.1. The original pulse train as well as the one with added blanking delay is shown in Figure 3.2. The

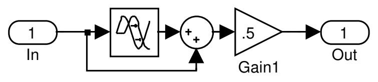

Figure 3.1: Generation of blanking delay using Simulink

numbers used for this simulation is taken from the current WPWM based power amplifier. This yields a switch frequency of 384 kHz, and a blanking delay of 50 ns. The duty cycle is 50/50.

Simulations of power supply perturbations are somewhat more complicated. The simplest configuration with the power supply perturbed by a sine is treated here. The distortion is obtained in Simulink by multiplying the signal with a source equalling the power supply. Here this source is chosen as a biased sine. The Basic principle is shown in Figure 3.3, where the signal is multiplied by a 0.1 amplitude sine biased by one. The “Dead time” block contains the system for blanking delay, shown in Figure 3.1. The resulting waveform is shown in Figure 3.4, where the perturbations is easily seen on top of the pulse train. The perturbations shown here are not entirely realistic, as the power supply perturbations usually are correlated with the power drawn from the supply, and thus the amplifier’s input signal. The perturbation shown here could be used for simulating *cross talk* which occurs when the same power supply supplies multiple amplifiers.

3.3.1 Evaluation of simulation

To determine the influence of the distorting blocks added, the Power Spectrum Density (PSD) was determined. When considering a PSD of the pulse train with added blanking delay, there is no visible change when comparing the spectrum

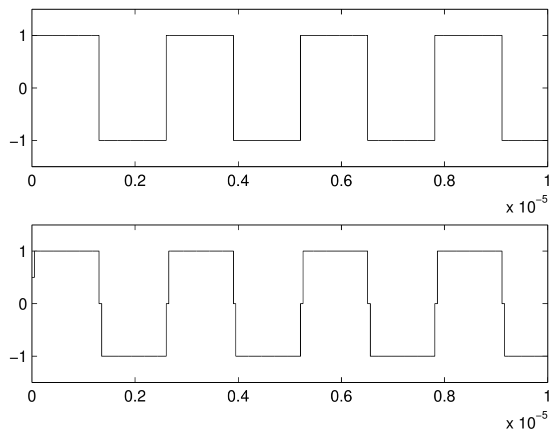

Figure 3.2: Original pulse train (top) and resulting pulse train with blanking delay (bottom)

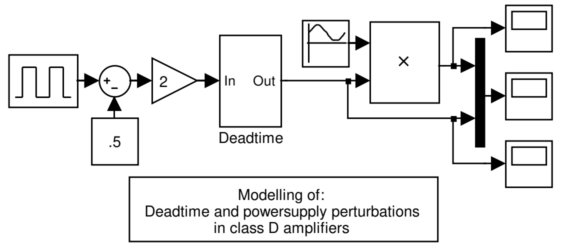

Figure 3.3: Generation of power supply perturbations using Simulink

for a 384kHz pulse with a 384kHz pulse with blanking delay. The impact of the blanking delay cannot be seen from the figure. According to Section 2.2.1 the blanking delay should add additional harmonic distortion but this cannot be seen as the harmonics of the carrier is above the bandwidth of the plot.

To determine the impact of the blanking delay, the Fourier series for a pulse train with blanking delay was determined in Appendix A. The spectrum for a standard pulse train with 50/50 duty cycle and f_c = 384khz, and a similar pulse with 50ns blanking delay was determined. The result is shown in Figure 3.6. When considering this figure it can be seen that the spectras only differ marginally. This Spectra only approximates the real spectra as it is based on a fixed switching frequency, where modulators as e.g. dAIM will have a varying

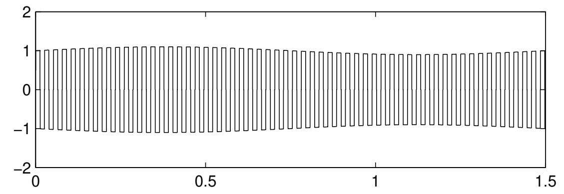

Figure 3.4: Resulting pulse train with blanking delay and perturbations on the power supply

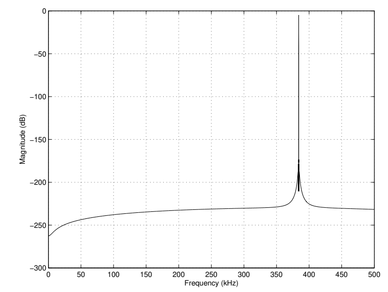

Figure 3.5: Idle spectrum after addition of 50 ns blanking delay, $f_c = 384kHz$.

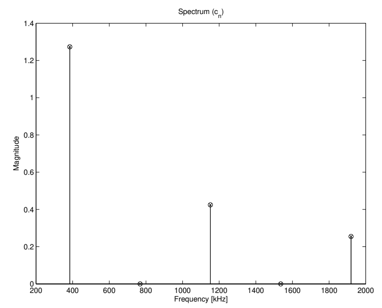

Figure 3.6: Spectrum for pulse without blanking delay (×) and with 50 ns blanking delay (○).

switching frequency.

Similarly a PSD of the pulse train with added distortion from the power supply perturbations was generated. This PSD looked as expected with heavy intermodulation between the carrier and the perturbations on the power supply. In simulations where the carrier is modulated with an input signal, similar

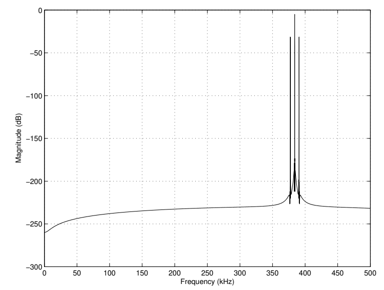

Figure 3.7: Idle spectrum after addition of blanking delay and power supply perturbations, $f_c = 384kHz$, supply perturbations 10% of supply voltage, $f_{\text{perturbation}} = 6.67\text{kHz}$.

sidebands will be seen around the frequency of the modulating signal. The level of perturbation applied is large to illustrate the properties, while in reality it will be much smaller, depending on the stiffness of the power supply.

The simple model shown here effectively models some of the basic properties of a class D amplifier, while it neglects many less significant. The neglected properties are primarily related to the physical behavior of the power stage where both transistors and the demodulation filter as well as the amplifier's load are neglected completely. These components play a large part in the behavior of a class D amplifier and thus a more complex model is required.

3.4 Improved model

To obtain more realistic results a more precise model of the power stage components is required. To implement this more realistic model the MATLAB Simulink toolbox SimPowerSystems was applied. This toolbox allows for simulation of switch mode power systems within Simulink.

The parts to be implemented using SimPowerSystems are the switching elements (MOS-FETs) and the demodulation filter. The values chosen for the components origin from the ICEpower 40 volts amplifier platform, where Eskil Jørgensen has been most helpful to provide data. The ICEpower 40 volts platform was chosen as it represents a midrange power output, delivering 210 watt into 4 Ω.

3.4.1 Building a model

The power stage model is implemented as a half bridge to simplify the model and thus improve simulation speed, and not as the H-bridge shown previously. This half-bridge is succeeded by a demodulation filter and finally a load.

Power stage

The model of the power stage is based on the MOS-FET found in SimPowerSystem. This model has 4 ports, gate drain and source as a normal FET and a measurement port where the diode current and voltage can be accessed. The FET is modelled as a current source, which implies a limitation on which loads can be driven. The FET model is a macro model which is either on or off, the transition is not modelled. The FET is controlled by the gate signal which is a numerical signal that turn the FET on when above zero and off otherwise. The FET has a measurement output; m. This signals is not used, and to avoid warnings it is connected to a termination block.

To control the two FETs with a signal similar to the one seen in Figure 3.2 some control are needed to split these signals into two separate signals controlling each FET.

The power supply for the transistors was modeled as controlled voltage sources in the initial model. These sources were then controlled by a sine with very high bias. In the final model, the power supplies were modeled as voltage sources with a series resistor which causes voltage drops related to the power consumed. It might be beneficial to incorporate both possibilities to be able to measure voltage drops related to the amplifier as well as uncorrelated voltage fluctuations related to outside disturbances.

Output filter

The output filter is modeled over the output filter currently used in the ICE-power 250A amplifier. The diagram is shown in Figure 3.8. This diagram only deviates from the original amplifier with the resistor $R_{L_{\mathrm{sim}}}$ which is added to solve simulation issues within Simulink, due to the fact that Simulink models transistors as current sources.

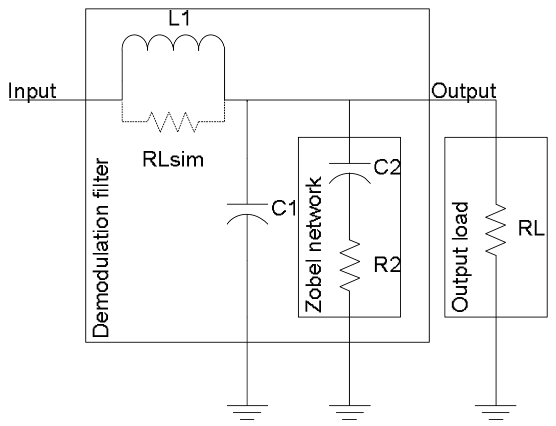

Figure 3.8: Demodulation filter for class D amplifier.

The output inductor is modeled as a ideal inductor which is far from a correct model. The properties of the inductor are dependent on the magnetic properties of the inductor which are never ideal, especially for power compo-

R_{on}	On resistance	36	mΩ
L_{on}	On inductance	$3 \cdot 7$	μH
R_{d}	Diode resistance	16	mΩ
R_{s}	Snubber resistance	∞	Ω
C_{s}	Snubber Capacitance	0	F

Table 3.1: Values for SimPowerSystem simulation of MOSFET switching element, approximating 40V ICEpower amplifier.

nents. The main problems with a power inductor are typically hysteresis and saturation. These properties have been left out of the model to keep it simple, while the contributions are among the main contributors to the distortion, when not considering blanking delay and supply perturbations.

The diagram suggests that the speaker connected to the output should be simulated with a resistive load. This might not be completely in touch with the reality, as a typical speaker is a quite complicated electro acoustical system. The resistive load is however quite good as measurements on real amplifiers are typically performed with a purely resistive load, thus the simulation will be comparable to real measurements.

3.4.2 Setting the parameters

The data used for the MOS-FETs are shown in Table 3.1. The snubber values are initially left at zero as recommended by Christian Lund from Bang & Olufsen ICEpower A/S. The snubber circuit is used to removed high voltage spikes at the transitions. A snubber circuit can be employed in the model, If the simulations have trouble with converging, however this reduces the accuracy, as no snubber is present in the modeled amplifier; however it improves simulation speed. The values for the output filter is shown in Table 3.2.

A disadvantage by not employing the FET's snubber circuit is that it is modeled as a current source, and thus not capable of driving a series load containing an inductor. This problem can be solved either by using the snubber circuit, or by parallel coupling the output inductor with a resistor, $\mathrm{R}_{\mathrm{L}_{\mathrm{sim}}}$, sufficiently large to be negligible. A value of 1 MΩ is chosen, and this value is indeed big in comparison with the other component values in the filter.

The output load resistor, R_L is chosen to 4 Ω. Loudspeakers usually have a nominal impedance of either 4 or 8 Ω, where 4 Ω are chosen as it induces larger output currents from the amplifier, and thus stresses it more.

Within the output filter are further two more blocks, one in series with the output load, and one in parallel with the output load. The series block measures the output current, and the parallel measures the output voltage.

The complete model is shown in Figure 3.9. In this figure oscilloscopes are connected to display output current and voltage.

3.5 A note on simulation within Simulink

When applying Simulink to solve problems in s-domain, a "solver" has to be chosen. This solver solves the differential equation involved in the diagrams

L_1	Output inductor	20	μH
$R_{L_{\mathrm{sim}}}$	Inductor resistance	1	MΩ
C_1	Output capacitor	330	nF
C_2	Zobel capacity	330	nF
R_2	Zobel resistance	10	Ω
R_{L}	Load Resistance	4	Ω

Table 3.2: Values for SimPowerSystem simulation of output filter and load, approximating 40V ICEpower amplifier.

created in Simulink. When applying the SimPowerSystem toolbox Simulink requires the use of a "stiff" solver. The solvers recommended by MATLAB for this task are `ode15s` and `ode23tb` where `ode` means "Ordinary Differential Equation". These solvers differ in that `ode23tb` has the classification "low"[1] precision while it converges fast where, `ode15s` has "low to medium" precision while converging somewhat slower. Other "stiff" solvers exist however they are for special problems, and are not considered here.

The term "stiff" is defined as follows:

> "A problem is stiff if the solution being sought is varying slowly, but there are nearby solutions that vary rapidly, so the numerical method must take small steps to obtain satisfactory results."

in [Mol04]. This means that the stiff solvers perform more work in each step but are able to solve stiff problems in less steps than non-stiff solvers. Excellent examples are given on this in [Mol04].

The precision can be further adjusted within Simulink by adjusting relative and absolute tolerances. By decreasing the values for the tolerances the precision as well as the simulation time increases. Finally the minimum, maximum and initial step size can be adjusted. Initially all these settings are left to their

[1] According to MATLAB online help.

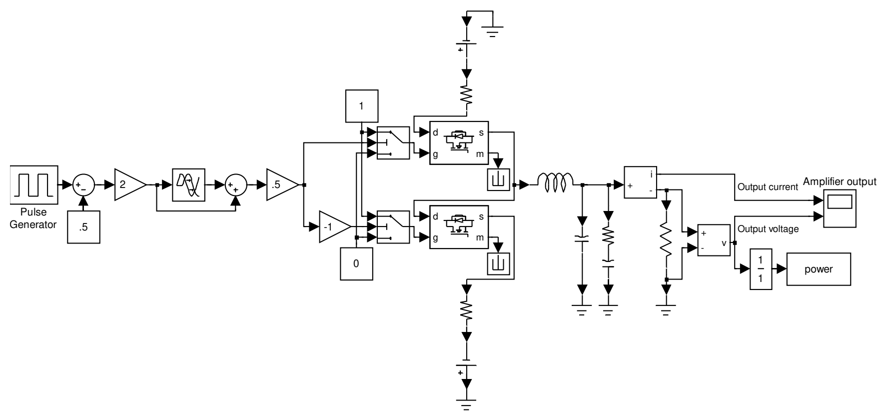

Figure 3.9: Complete Simulink model of the power stage, including blanking delay, power supply perturbations, transistors and demodulation filter.

default setting which is variable step size, the relative tolerance is set to $1 \cdot 10^{-3}$, and the remaining settings left to `auto`.

The choice of solvers as well as the parameters for them does not influence the discrete part of the system.

3.6 Tuning the model

To verify the function of the power stage model a 6^{th} order lowpass filter was attached to the output voltage and current measurements. The filter has a cutoff frequency of 20 kHz. The initial simulations revealed some rather strange behavior. The output was rather distorted. This distortion is easily visible

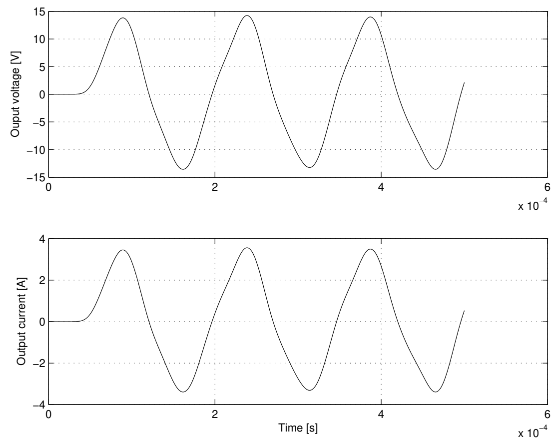

Figure 3.10: Simulation of power system as shown in Figure 3.9 with 7 kHz, M=0.7 input.

from Figure 3.10, where the slope of the sines changes significantly at the zero crossings.

To avoid these problems a larger value for $\mathrm{R}_{\mathrm{L}_{sim}}$ was tried, 1 GΩ was inserted. This solved the problem, however it did not prove as a solution, as it caused the simulation to run *very* slowly. There was no major speed increases to gain by changing the solver or the parameters for the simulation precision.

As mentioned in Section 3.4.2 the transistor model's snubber circuit could be employed if the simulation has trouble converging. The snubber values were set to the SimPowerSystems default for the first trial; $\mathrm{R_s} = 10\Omega$, and $\mathrm{C_s} = 0.01\mu\mathrm{F}$. The result is shown in Figure 3.11. The result obtained with snubber circuit seems more reasonable as the output resembles the input sine much better than the previous simulation. Furthermore the simulation converges much faster. After consulting with Eskil Jørgensen from Bang & Olufsen ICEpower A/S again, the snubber capacitance, C_{s}, was changed to 470 pF as 10 nF is far too much for an audio amplifier. When simulating with this new value, results somewhat similar to the default snubber values are obtained. The result is shown in Figure 3.12. This result converges a bit slower than the previous snubber simulation. This is expectable as the smaller capacitor causes sharper transitions and thus more ringing at each transition, which leads to a reduced step size around the transitions. The simulation speed is however still far better than the simulation without snubber circuit.

To further verify the model the blanking delay can be set to zero, to force the model into a state where "shoot through" occurs. When performing a simulation with the blanking delay set to zero the simulations run at a slower speed. This might be an indication that something changing fast has occurred in the system after removing the blanking delay. This corresponds well to the expected results. When dealing with blanking delay in real life, the effect is usually determined by measuring the power consumed by the amplifier in idle. Ideally no power should be consumed. Whenever "shoot through" occurs the

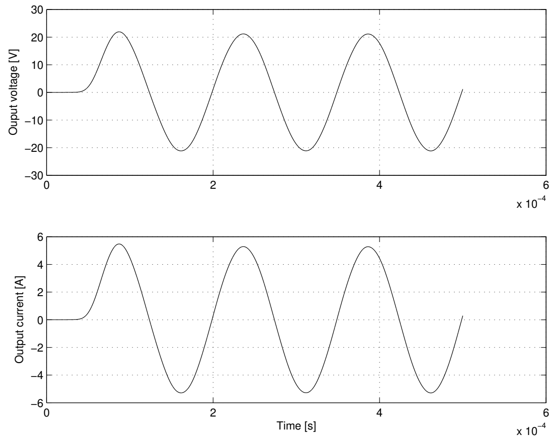

Figure 3.11: Simulation of power systems as shown in Figure 3.9 with 7 kHz, M=0.7 input. $R_{L_{sim}}$ is changed to ∞ and The MOSFET models snubber circuits are enabled, C_s=10 nF.

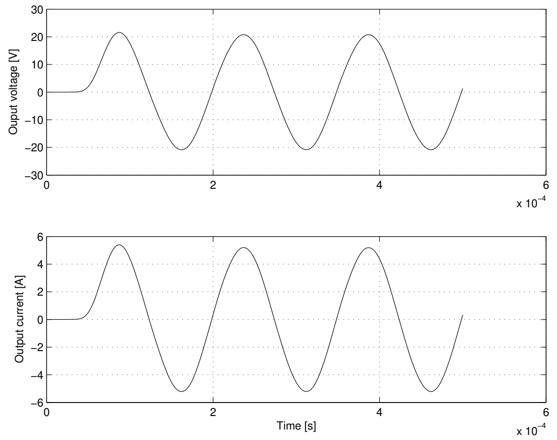

Figure 3.12: Simulation of power systems as shown in Figure 3.9 with 7 kHz, M=0.7 input. $R_{L_{sim}}$ is changed to ∞ and The MOSFET models snubber circuits are enabled, C_s=470 pF.

R_{on}	On resistance	36	mΩ
L_{on}	On inductance	$3 \cdot 7$	μH
R_{d}	Diode resistance	16	mΩ
R_{s}	Snubber resistance	10	Ω
C_{s}	Snubber Capacitance	470	pF

Table 3.3: Values for SimPowerSystem simulation of MOSFET switching element, approximating 40V ICEpower amplifier, after fine tuning for simulation.

power dissipated will rise significantly. An ampere meter is connected in series with both the positive and the negative supply. The amplifier input is connected to a 384 kHz 50/50 duty cycle pulse train, and the current is measured with and without blanking delay. The result of this test is shown in Figure 3.13. In

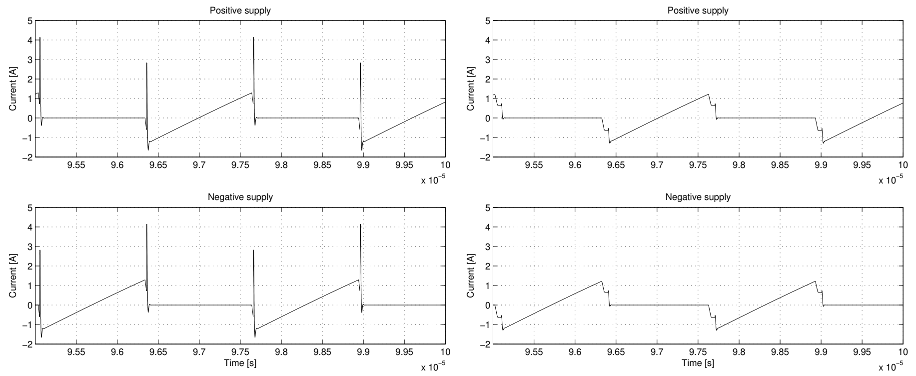

Figure 3.13: Simulation of power systems with no blanking delay (left) and 50 ns blanking delay (right).

the case with no blanking large spikes are seen at the transitions, while there are no spikes with 50 ns blanking delay. Thus the transistor model behaves as expected.

In the final model the voltage source supplying the amplifier is changed to fixed voltage source in series with a resistance, modelling the output impedance of the source. The two sources are both set to 40 V. The output impedance of power supplies is usually frequency dependent, but to simplify the model a pure resistance was chosen. After consulting with Lars Michael Fenger from Bang & Olufsen ICEpower A/S, the value was set to 1 mΩ which was said to be a suitable value. The output resistance is, besides being frequency dependent, also dependent of the type of supply. Using a good switch mode supply with a high bandwidth in the control loop of course offer better performance than a simple transformer with a rectifier bridge and a capacitor.

To ease the model overview these changes have been incorporated into the previous tables, and are shown in Table 3.3 and 3.4.

L_1	Output inductor	20	μH
$R_{L_{\text{sim}}}$	Inductor resistance	∞	Ω
C_1	Output capacitor	330	nF
C_2	Zobel capacity	330	nF
R_2	Zobel resistance	10	Ω
R_{L}	Load Resistance	4	Ω

Table 3.4: Values for SimPowerSystem simulation of output filter and load, approximating 40V ICEpower amplifier, after fine tuning for simulation.

3.7 Evaluating the model

The simulation was carried out to verify the dAIM implementation as well as the power stage model. To provide the simplest verification the dAIM results should be comparable to the simulation results obtained in [Kje03]. This was done by using the simulator blocks developed in [Kje03] for all post processing of the signal. Furthermore the signal lengths and sampling frequencies was, to the widest extent possible, the same as used in [Kje03].

To provide simple verification of the power stage model the results found were compared to measurements on a *real* unregulated power stage. These real measurements were taken from [And02]. When comparing the measurements found in [And02] with the results from the simulations, it should be remarked that different PCM→PWM conversions are used. In [And02] WPWM is used while dAIM is used in the Simulink model. This is of course problematic, however these two modulators have similar performance especially when both are driven by an input signal with high sampling frequency (384 kHz) in both cases.

To evaluate the model let us first take a look at a waveform from the amplifier output when idle. To obtain this simulation the dAIM modulator was replaced with a 384 kHz 50/50 duty cycle pulse generator. The waveform is shown in Figure 3.14. The primary observation to be made here is that the only signal present is the 384kHz signal controlling the switches. This signal is heavily attenuated by the output filter, and the remaining ripple voltage seems to be sinusoidal. Secondly, let us take a look at the spectrum that is shown in Figure 3.15. In comparison with the spectra shown for blanking delay on Figure 3.5 there is considerable more noise. The exact origin of this noise is not known however it could be the calculation of the PSD or the Simulink simulation tolerances that induce it. From the PSD it can be seen that the signal is indeed sinusoidal.

Next, let us take a look at the amplifier when excited. A common frequency used for test is 6.67 kHz. This signal is chosen as it is the highest frequency where the 3^{rd} harmonic is within the audio band. The signal is shown in Figure 3.16. The input signal as well as the carrier are easily seen. It shows that the carrier is attenuated by the demodulation filter while the signal passes unaltered through the amplifier. When regarding the spectrum shown in Figure 3.17 some interesting things begin to emerge. First of all uneven harmonic distortion occurs. And, secondly, intermodulation between the input signal and the carrier is seen around the peak at the carrier frequency.

When comparing the figure with the similar plot for dAIM alone, shown in

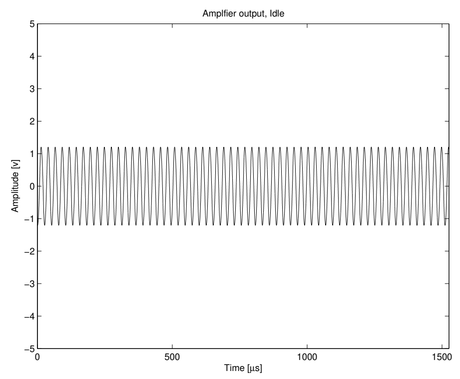

Figure 3.14: Amplifier output when idle, input 384kHz 50/50 duty cycle pulse train.

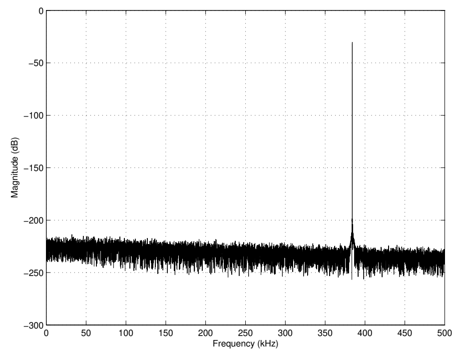

Figure 3.15: Spectrum of amplifier output when idle, input 384kHz 50/50 duty cycle pulse train.

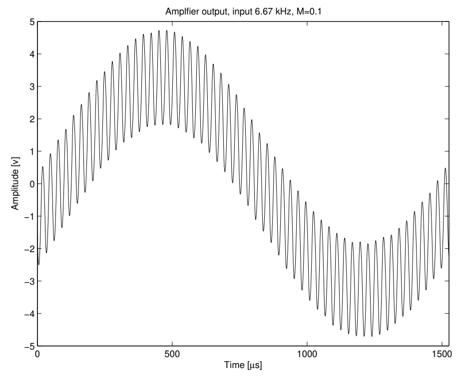

Figure 3.16: Amplifier output, input 6.67 kHz, M=0.1.

Figure 2.12, page 18, the main observation to be made is that the noise floor is much higher. Within the audio band, the noise floor is almost constant when the power stage is connected, while the noise floor from the modulator itself is very low at low frequencies and increases towards higher frequencies. This is visible from both narrow and wide band FFTs. Furthermore the dAIM modulator itself has no harmonic distortion while the THD+N from output of the power stage is -51 dB (0.3 %). This is somewhat lower than the real measurements from an unregulated power stage. The expected result can be seen by Figure B.2, page B-2, where the THD+N is 0.7 % under similar conditions. The results are unfortunately not directly comparable as the THD+N measurements of the unregulated power stage are made using the WPWM modulator and not the dAIM however the difference in perforamnce is very small. The main source for the deviation is the output inductor which is modeled by an ideal inductor while the real inductor's parameters are dependent on many parameters related to its magnetic properties.

The simulator developed by [Kje03] can estimate the dynamic range when excited by a sinusoidal input with an amplitude of -60 dB. The FFTs with

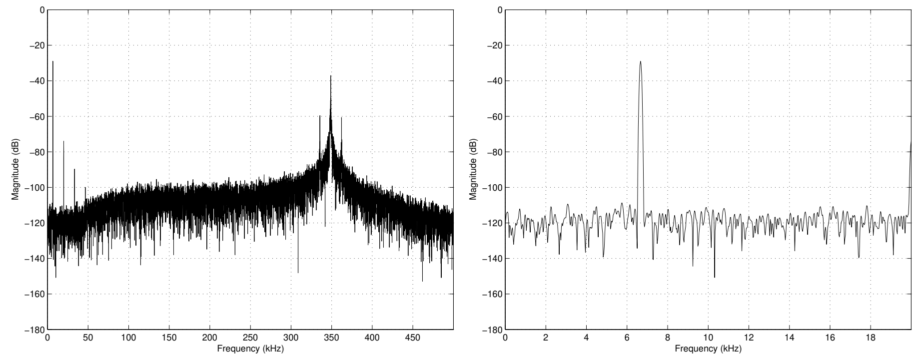

Figure 3.17: Spectrum of amplifier output, input 6.67 kHz, M=0.1 (-20 dB). Left: Wide band plot, Right: Narrow band plot.

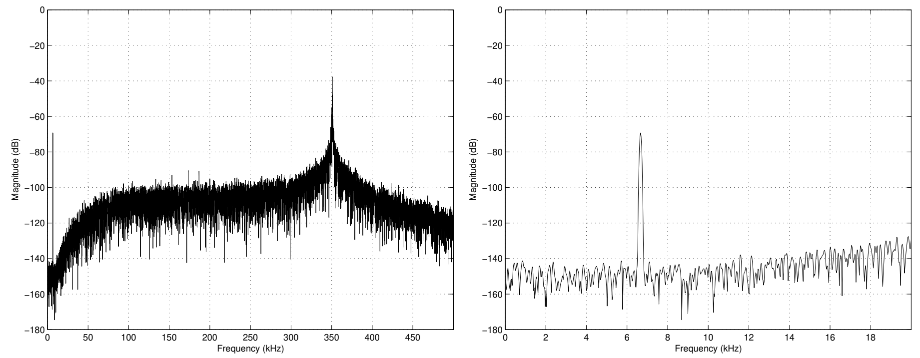

Figure 3.18: Spectrum of amplifier output, input 6.67 kHz, M=0.001 (-60 dB). Left: Wide band plot, Right: Narrow band plot.

-60 dB are shown in Figure 3.18. From these FFTs the dynamic range can be determined to be 107 dB. The result is slightly better than the result for a similar modulator in [Kje03] (105 dB) but the sampling frequency, f_s are doubled from 192 kHz to 384 kHz, so this result is not surprising. The THD+N is 0.4 % which is worse than the simulation at -20 dB. This is expected as the lower amplitude of the signal brings the signal closer to the noise floor.

Ideally many more simulations should be made to verify the models behavior over a wide range of input situations, however the simulations are rather slow, and it would thus require a tremendous amount of time to make THD+N plot similar to the ones shown for the PEDEC and the unregulated power stage.

3.8 Measurements on, and comparison with, an unregulated power stage

To verify the model, additional measurements were made to complement the measurements in [And02]. These measurements were made by sampling a relatively long signal, which subsequently can be processed in MATLAB.

3.8.1 Modifying power stage for measurement

The measurements made are based on an analog amplifier modified to receive the pulse train from a digital modulator instead of an analog signal. The amplifier used for the measurements was the ICEpower 500A module, which is capable of delivering 500 watt into a 4 Ω load. It might seem unreasonable to choose a 500 watt amplifier for the measurements when all simulations are based on a 210 watt amplifier. The reason for this is that the ICEpower 250A module has an unlinearity in the blanking delay which causes the upper MOS-FETs to have unequal blanking delay (approximately 60 ns difference, the one FET has 30 ns while the other has 90 ns, while the lower FETs both have 60 ns). This nonlinearity would cause additional distortion beyond what is typically seen, and what is modelled in the Simulink model. The 500A module is without this nonlinearity and was thus chosen. By supplying the 500A module with a lower supply voltage, 50 V instead of 70 V, it models a 250 watt amplifier quite well. The choice of the 500A induced some further problems due to it's more complex

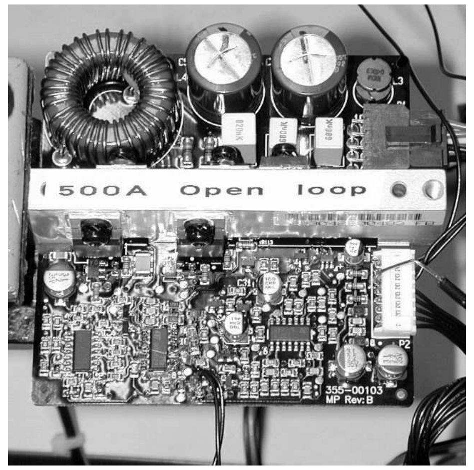

Figure 3.19: The modified ICE500A module used for the measurements.

design. If the 250A module had been used the signal could have been inserted directly on to the drivers for the MOS-FETs. This is not possible on the 500A where the blanking delay is not created by the drivers but by a feedback around a comparator earlier in the signal path. Thus the signal had to be routed through this comparator. The changes made are described in the following, however the full diagram is not included as it is confidential. A simplified diagram is shown in Figure 3.20.

The input was applied to the comparator by removing a resistor in the signal path from the analog modulator, and connecting the pulsed output from the digital modulator. To enable the power stage to run, the reference to the comparator had to be set to the middle of the output voltage from the modulator which is either 0 or 3.3 V. This was done by a voltage divider which was used to create 1.65 V. The resistors for this voltage divider were chosen as a tradeoff between power consumption and voltage stability. The values are 7.5 kΩ for the upper resistor, and 1.2 kΩ for the lower resistor. Unfortunately the comparator is quite fragile, and it had to be changed more than once during the modifications due to overload of the input.

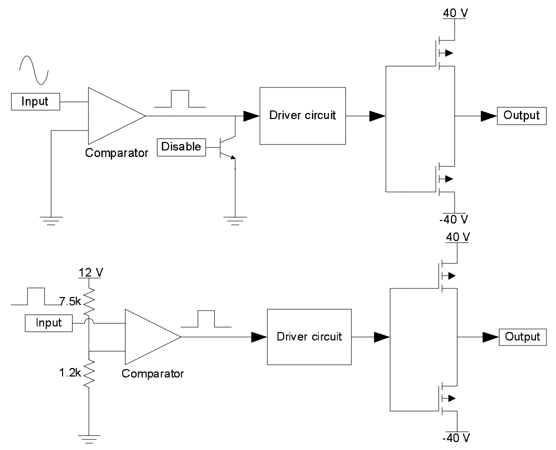

Figure 3.20: Simplified amplifier diagram. Top: Before changes, Bottom: After changes.

To enable the power stage to run at 50 V the voltage check had to be disabled. The amplifier is disabled by two transistors which pull the PWM output of the comparator down to ground if the amplifier is disabled, and thus causes the switching to cease. This disable circuit was disabled by lifting the transistor leg connected to the PWM paths.

Finally the resistors connecting the output to the feedback path were removed to avoid the analog control systems operating, and thus reduce any noise caused by unwanted operation of the control system.

3.8.2 Measurement setup

The digital modulator used was a dAIM modulator implemented into Bang & Olufsen ICEpower A/S' most recent digital hardware; the DHW40. This hardware version is created from a slightly modified version of the Virtex-II MB evaluation board from Memec Design. The board contains a Xilinx Virtex II FPGA which excels in both speed and complexity, with a possibility of implementing designs which equivalents 1 million gates. This evaluation board is combined with an interface board, developed by the author of this thesis, which contains an interface for SP/DIF, in optical and electrical medias, as well as AES/EBU interface. Furthermore the interface is equipped with a sample rate

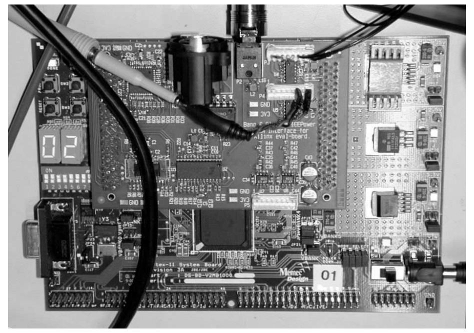

Figure 3.21: ICEpower DHW40 development platform for digital modulators. Large print is the Virtex-II MB board, with the smaller interface board connected on top.

converter and a digital filter used for oversampling. This enables the interface to supply the modulator implemented in the FPGA with high quality audio signals with a wide range of sampling frequencies, spanning from 32 kHz to 768 kHz. Finally the interface board is equipped with drivers capable of supplying the PWM signals generated to a power stage. For pure evaluation of algorithms, without power stage, the interface board is equipped with a 3$^{\mathrm{rd}}$ order low pass filter for demodulation.

The dAIM modulator implemented had the same coefficients as used in the simulations ($G_1 = 2^{-6}$, $G_2 = 2^{-7}$ and $G_3 = 2^{-8}$), and the volume control implemented was set to 0 dB to avoid distortion caused by the volume control.

The input for the dAIM was created using a PC-based measurement device made by Audio Precision. This device is basically a tone generator (with analog and digital output), and an analyzing section capable of a wide range of measurements. The AP is the reference in the audio industry and is used for evaluating most types of audio equipment.

As time series were needed, the AP was not used for analysis. Instead a WaveRunner 6030 sampling oscilloscope from LeCroy was used. This oscilloscope's main features are a very high bandwidth (350 MHz) and a very deep memory, which allows for fast sampling of long time sequences. Another useful feature is the capability to save the time series directly in Matlabs file format.

The AP was connected to the digital interface board with a TOSlink cable which is fiber optics. This was chosen to avoid ground loops, and thus 50 Hz hum in the system. The output from the power stage was connected to the oscilloscope by a LeCroy ADP305 differential probe which has 100 MHz bandwidth. The use of a differential probe is necessary as the output of the ICE500A module is balanced, and thus not referred to ground. A diagram of the complete system can be seen in Figure 3.23.

At both sessions the frequencies measured were 100 Hz, 1 kHz and 6.67 kHz. At the first session the measured amplitudes were -60 dB, -20 dB, and at the second they were -60 dB, -20 dB and -2 dB. All these measurements are not intended for evaluation use in the first place, but are made as the additional time used to make them are far less than the time required if they were to be made later.

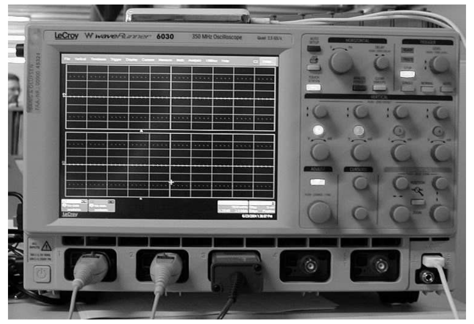

Figure 3.22: LeCroy WaveRunner 6030 with an Apple iPod on top for storage.

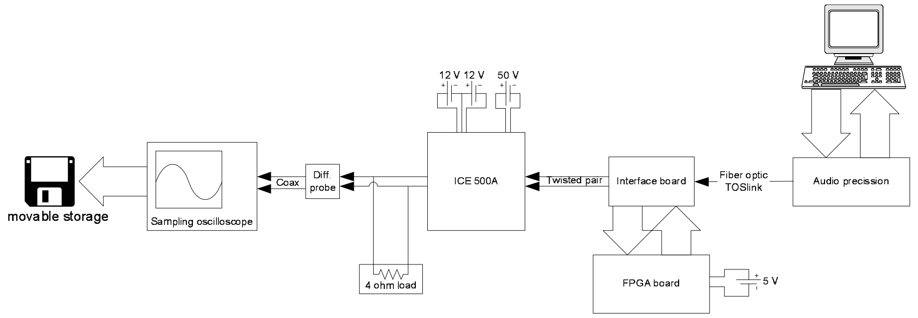

Figure 3.23: Complete system for measurements.

3.9 Results

The wave forms obtained are rather similar to the ones obtained from the simulator. When comparing Figure 3.16 and 3.24 the two waveforms are quite

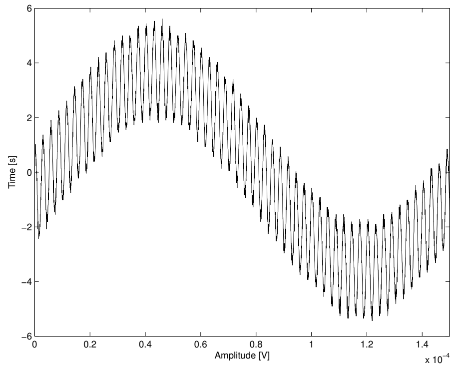

Figure 3.24: Amplifier output, input 6.67 kHz, M=0.1 (-20 dB).

similar. The amplitude of the latter are a bit higher, but this is as expected, as the amplifier measured operates on a voltage a bit higher than the one used in the model. There is additional noise on the amplifier measured, it is especially noticeable around the peaks of the carrier sinusoidal.

To do a comparison between the model and the real amplifier simply comparing the waveforms by eye will not do; numbers are needed. The THD+N and dynamic range are obtained using the exact same functions as for the Simulink models. The FFTs used are calculated using what what corresponds to 2^{14} input samples at the given output frequency, and can be determined by Equation 3.1.

$$n_{\mathrm{FFT}} = n_{\text{input samples}} \cdot \frac{f_{\text{sampling, oscilloscope}}}{f_{\text{sampling, input}}} \tag{3.1}$$

For the first measurement session $2{\cdot}10^6$ data points were collected at 25 MHz, in total 80 ms, and for the second session $1 \cdot 10^6$ data points were collected at 10 MHz, in total 100 ms.

To have a wider range of data a second session was done, which included -2 dB input. The measurements done during session 1 were repeated to ensure data consistency. The -2 dB measurements at 100 Hz are left out as they caused the 50 V power supply to clip and thus were unusable.

The FFTs calculated can be found in Appendix D.1 for the first session, and in Appendix D.2 for the second session.

The results in terms of THD+N are shown for both sessions in Table 3.5 and 3.6. The dynamic range included is a readout given by the simulator implemented in [Kje03].

Frequency	100 Hz		1 kHz		6.67 kHz	
Input level	THD+N	Dyn.	THD+N	Dyn.	THD+N	Dyn.
-60 dB	-22	82	-16	76	-14	74
-20 dB	-42	N/A	-23	N/A	-26	N/A

Table 3.5: Measurement results from first measurement session. All measurements are in dB.

Frequency	100 Hz		1 kHz		6.67 kHz	
Input level	THD+N	Dyn.	THD+N	Dyn.	THD+N	Dyn.
-60 dB	-25	85	-40	100	-12	72
-20 dB	-33	N/A	-8	N/A	-22	N/A
-2 dB	N/A	N/A	-24	N/A	-28	N/A

Table 3.6: Measurement results from second measurement session. All measurements are in dB.

To get a better understanding of the measurements they were compared. The measurement data for the two sessions, the difference between them, the simulation results from the Simulink and the difference between the measurement results and the Simulink results in terms of dB and magnitude. These data are shown in Table 3.7.

The two measurement sessions differ a lot. The origin of these differences are not known for certain, however they could be related to:

Frequency	100 Hz		1 kHz		6.67 kHz	
Measurement	-20 dB	-60 dB	-20 dB	-60 dB	-20 dB	-60 dB
Session 1	-26	-14	-23	-16	-42	-22
Session 2	-33	-25	-8	-40	-22	-12
Difference	7	11	-15	24	-20	-10
Simulink (from Section 3.7)	-50	-49	-45	-48	-51	-47
Difference	17-24	24-35	22-37	8-32	9-29	25-35
Difference in magnitude	7.1-15	15-56	13-71	2.5-40	2.8-28	18-56

Table 3.7: Comparison of THD+N, all numbers are given in dB.

- Ambient environment, especially electromagnetic interference.
- Changed operations of the oscilloscope.

The ambient environment at Bang & Olufsen ICEpower A/S can vary a lot as many class D amplifiers can be operating with high output currents, and no shielding. The noise floor has been seen to jump about 20 dB due to amplifiers operating nearby. Furthermore the oscilloscope operation was changed from first session to second. In the first session the data was sampled at 25 MHz while it was only sampled at 10 MHz in the second session. After consulting with LeCroys home page another problem occurred; the data is sampled with 8 bit resolution, which is insufficient for proper audio reproduction. The effect of quantization is somewhat dampened by the high oversampling, as discussed in Section 2.5. The oversampling gains approximately 4.5 bits at 25 MHz, while only 3.9 bits are gained by 10 MHz.

This sums up the main possibilities for the mismatch between first and second session. As it varies whether first or second session is best, the gain of resolution by oversampling can be left out, and the remaining error source is the ambient environment.

When comparing the measured results with the results obtained in Simulink, a mismatch can be seen again. The problem is generally better THD+N in the simulation than in the measurements. This is especially noticeable at low signal levels (-60 dB) where the signal is very faint and even small increases in the noise will have significant influence. The difference at -20 dB is probably related to the quantization in the oscilloscope.

3.10 3rd Measurement Session.

As no clear relationship between the two measurements themselves and the simulations results could be shown in terms of THD+Noise, of the reasons explained above, a third measurement was made. This measurement was done as shown in Figure 3.23, though the sampling oscilloscope was removed, and the analog analyzer section of the AP was connected instead. The AP was set to measure THD+Noise, and sweep the input amplitude, to produce a plot of THD+Noise plotted versus input amplitude. These plots can be seen in Section D.3.1. On these plots the points (-60 dB, -20 dB and -2 dB), whose values can be found in Table 3.8, are marked with ◦. To ensure consistency these measurements were carried out two times as well, and they produced similar results within .1 dB. The results shown in the table are the mean value.

	100 Hz		1 kHz		6.67 kHz	
Input level	Meas.	Sim.	Meas.	Sim.	Meas.	Sim.
-60 dB	-28.2	**-49**	-40.9	**-48**	-31.0	**-49**
-20 dB	-28.6	**-50**	-40.9	**-45**	-33.8	**-55**
-2 dB	-29.2	**-37**	**-41.5**	-33	-31.5	**-44**

Table 3.8: THD+Noise on unregulated power stage, measured with AP and simulation results from similar model. Best performance in each case is marked with **bold.**

The results for -20 and -60 dB were compared with the simulation results and the deviance was comparable for both excitation levels, indicating a higher noise floor than the simulations. The deviance was approx. 17 dB (equal to 7 times higher THD+N on the measurements). These results are more believable than the ones shown in Table 3.7. The THD+N measurements shown in Section D.3.1 can each be divided into two parts, on each side of the minima, at left side (low amplitude inputs) the noise is the dominant contributor, while the harmonic distortion is the main contributor on the right side (high input amplitudes), where the noise is neglectable. This general property is only of limited use for the measurements as we only have three points. They can however be used to tell a little about the faults of the model.

At low amplitudes there is a large deviance, 17 dB, which indicates that the noise level in the simulator is too low. This lack of noise is caused by the ideal components used for the simulation. These components lack the thermal noise originating from real components, especially larger resistors. At higher amplitudes it can be seen that the harmonic distortion in most cases are too low. As with the low amplitudes the lower noise levels are caused by use of ideal components. As explained earlier the output filter which is a major contributor is modeled as ideal, and thus causes a lower level of distortion.

3.11 Comparison of FFTs.

As explained in Section 3.9 FFTs where calculated from the time series measured during session 1 and 2. Similarly FFTs where measured using the AP, during session 3. The FFTs measured were using 2^{14} input samples, 4 times averaging and a Blackman-Harris window. These settings correspond to the ones used in the simulator. Unfortunately the APs sampling frequency is 65 kHz and not 384 kHz as used in the simulation. This causes an increased frequency resolution, which leads to a lowered noise floor as the energy contained in each bin becomes smaller as the frequency increases. The increased noise level found in the FFTs obtained from the time series, measured using the LeCroy oscilloscope, is due to the low resolution.

The measured FFTs used were the FFTs obtained from the AP, as they have the lowest noise floor, and thus reveals any frequency components hidden below the noise floor better. These measured FFTs can be found in Appendix D.3, and the simulations can be found in Appendix C.

The FFTs measured have similar properties at -60 dB. These are, besides the first harmonic, dominated by frequency components spaced at 1 kHz, and not directly related to the first harmonic. These additional frequency components are identical for 100 Hz and 6.67 kHz. They do not appear in the simulation results.

Another general property of the measure results is the presence of equal harmonics. These can be found in all measurements at higher amplitudes, where harmonic distortion occurs. They are typically caused by some unevenness in the amplifier, and could for instance be caused by poorly matched transistors in the amplifier. These even harmonics are not seen in the simulation, however they can easily be created if wished so. As the amplifier used is based on a full-bridge they do not origin from the power supply. They likely originate from the transistors are the driving circuit for the transistors. Another sources could be the output inductor which, for this particular amplifier, is created of two inductors, one for each half-bridge, wound on the same core, to provide coupling between them. This construction could add additional even harmonics if the two windings are not entirely identical.

3.12 Conclusion on Amplifier Modeling

During this chapter a simple amplifier model was developed. To obtain a more realistic model this model was expanded into a more advanced model which models the MOSFETs employed as switching elements as well as the demodulation filter. Furthermore a more realistic supply was added, by adding the output impedance of the power supply to the model.

The model however has some shortcomings, first of all the components used to model the demodulation filter were ideal, where real components designed to handle the required power are definitely not, as they have some parasitic components as well. The modeling of the power supply's output impedance is also an approximation. Power supplies typically have frequency dependent impedance, which increases with frequency. Finally the amplifier's load is modeled by a resistor. This is a rough approximation as a real amplifier would be loaded with a loudspeaker. A loudspeaker's impedance varies from a lot depending on the drivers used and the acoustical as well as the electric design, thus a average model cannot be created. Instead a resistive load has been chosen as this typically is the load chosen for lab measurements.

The simulation results obtained basically agree with what should be expected however there are some differences from the measurement shown on an unregulated power stage in Section 2.6, page 19. These differences are as explained related to the trade-offs made during the model design, and are in no way critical.

Chapter 4

Feedback

As mentioned in the introduction a lot of feedback options exists. The two main classifications are:

- Feedback of timing information. The feedback signal is taken between the MOSFETs and the demodulation filter, and consists of a pulse train.
- Feedback of amplitude modulation. The feedback signal is taken from the output of the demodulation filter.

The first option benefits from a simple implementation. Only a very simple A/D conversion is required in the feedback path, the signal should just be scaled down to the digital levels. This modulator could for instance be implemented by closing the loop in the dAIM modulator around the power stage. Alternatively the error could be calculated by subtraction, and feed into an error correction unit before the modulator.

4.1 Performance requirements

Before starting the evaluation of different feedback schemes, a target has to be defined. To justify the implementation of a digital feedback system the system has to be better. But this causes a new question to rise: "What does *better* mean?" The obvious answer is that better means better audio specifications. However there is another answer, better also means smaller and cheaper. If the technology developed here can allow the use of a digital class D amplifier in an application where it previously has been unavailable due to cost or size, the technology can be justified, even if it doesn't offer better audio specifications than available today. The parameters relevant for evaluation are:

- **Audio specifications:** The costumers want good sounding amplifiers.
- **Flexibility:** The digital approach can ease the implementation of control system as it can easily be changed by reprogramming the software, while an analog solution would require changing components.
- **Price:** Reduced manufacturing costs allow for a larger profit margin (more $) or reduced price which yields larger sales (and again more $).

- **Size:** Reduced size of the complete amplifier allows for implementation of high efficiency amplifiers where previously impossible. An application could be polyphonic ring tones for cellular phones.

The first parameter is quite easy to estimate as the audio measures introduced in Section 2.9 can be used directly. As argued there are some new algorithms which claim to evaluate sound the way humans perceive it and thus provide a better measure, but these algorithms are not widely used, and thus unusable for comparison between different amplifiers.

The second and third parameters are somewhat harder to estimate as they are not related directly to the developed algorithm. They are dependent on many other parameters, eg. semiconductor technology, availability of raw materials, not to mention the large scale economics involved. Estimating these parameters is far beyond the scope of this report.

These parameters can be estimated by comparison of parameters related to implementation. The parameters are gate count and speed requirement of the digital circuit which sets the demands for the chip technology, and secondly the silicon area required, which controls the cost. These parameters are also available for the IC implementation of the WPWM algorithm which is implemented by Sanyo Semiconductors. The comparison is however complicated by the involvement of analog ICs which are not directly comparable to digital ICs. However we are far away from these parameters as well. The parameters available are the number and type of arithmetic operations used to process a sample. These numbers can be compared to those available for other digital modulators.

4.2 Initial approaches to timing feedback

When considering the analog amplifier from Section 2.1, page 6, the inner control loop providing timing feedback has a high bandwidth. The bandwidth requirements are set by the nature of the amplifier which requires a phase of $-180°$ to oscillate. If the loop is not used to make the amplifier oscillate, a lower bandwidth is sufficient. A lower bandwidth requirement would furthermore be attractive as it is extremely difficult to obtain high resolution, high sampling frequency converters.

The digital control system basically consists of two parts, an A/D conversion and a control system. Each is unavoidable and highly dependent on the other. Thus they cannot be designed independently and joined later on. In the following both are treated simultaneously, but with a bit more weight on the A/D converter initially as it is easier to apply changes to the control system than the A/D converter itself.

Far the easiest approach to designing the feedback system is downscaling the power output from the FETs to TTL level. As this signal is a pulse train it can (ideally) be sampled as a 1 bit signal. Sampling this way is not without problems. To obtain sufficient performance the sampling resolution should be high enough to cause no major unlinearities in the feedback path. When considering a switch frequency of 384 kHz and a system frequency of 98.304 MHz this gives 256 clock cycles and thus corresponds to 8 bit precision. This is clearly not enough for reproduction of quality audio. If the information contained in each input sample should be effectively recovered by 1 bit sampling after pulse modulation a sampling frequency of $2^{n_{\text{bit}}} \cdot f_{cycle}$ would be required. For the

384 kHz system that would give approximately 25 GHz if a resolution of 16 bit is required. While this speed might be obtainable for very high end scientific applications with low complexity, it is definitely not available to consumers.

A solution which might sound reasonable would be to incorporate some sort of noise shaping $\Delta\Sigma$ modulator circuit. This would, as shown previously in Section 2.7, page 22, effectively reduce the quantization noise in the audio band. Simulations done by Bang & Olufsen ICEpower A/S's semiconductor partner Sanyo, when implementing the WPWM modulator, has however shown it ineffective to implement several cascading $\Delta\Sigma$ modulators.

Another solution could be to close the dAIM loop around the power stage. This could easily be achieved by properdown scaling of the power output from the FETs. This implementation is beneficial as the whole system would be contained inside a single noise shaping circuit. The complete system is shown in Figure 4.1.

Unfortunately the unlinearity inside the loop would consist of a power stage, a gain and two quantizers. This is in it self not a problem, however the output being fed back would be the output inside the control loop, and the power output would be uncorrected.

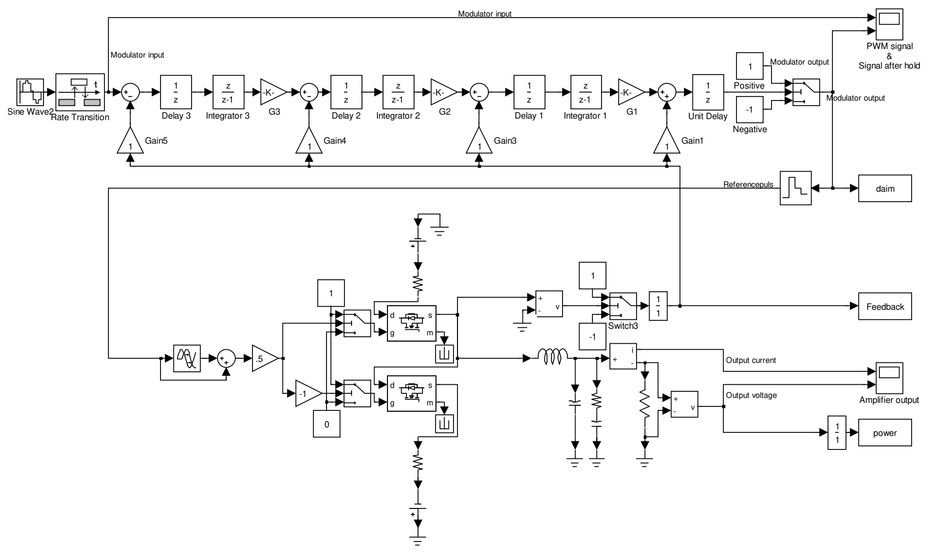

Figure 4.1: 3$^{\text{rd}}$ order dAIM modulator with the power stage inserted into the feedback path.

The results of a simulation are shown in Figure E.1, E.2 and E.3 which show the spectrum of the amplifier output, the amplifier input and the feedback signal. It can easily be seen that both amplifier output and input suffer from an increased noise floor. The PSDs are similar in both cases within the audio band while they differ at higher frequencies. The THD+N is 37 dB for the amplifier input, while it is 35 dB for the output.

The PSD plot of the signal (shown in Figure E.3) in the feedback path is remarkable. In this signal the noise floor is very well suppressed, and the obtained THD+N is 75 dB, corresponding to the result for the dAIM itself, which can be seen in Figure 2.12, page 18.

These simulation illustrates the properties of dAIM quite well, in principle the dAIM algorithm should be sufficient to correct the errors occurring in the power stage if a feedback without unlinearities can be obtained. The feedback used for these simulation does however contain a transition from analog to digital domain which causes a quantization of the pulse edge's placement in continuous time.

The error occurring when sampling the pulse edges is illustrated in Figure 4.2. The error on the leading edge is in the range [-1 0] cycles, while the error on the trailing edge is [0 1] cycles. This error is considered to be uncorrelated to the signal, and thus uniformly distributed. This gives a total error in the pulse

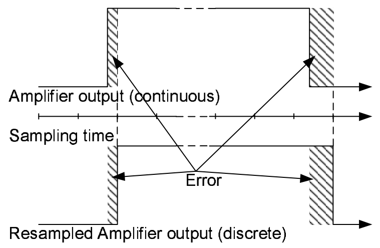

Figure 4.2: Error on pulse placement due to sampling with finite frequency.

width in the range [-1 1] cycles. The error is given by a difference between two uniform distributions. This error has a triangular distribution with mean zero if the two uniform distributions are assumed to be uncorrelated. However this last assumption is not valid. The noise level can easily be calculated from this, if the assumptions are valid, however this is not necessary to realize that the noise level is beyond the tolerable.

The main message above is that the 98.304 MHz sampling frequency is too slow. Either the sampling frequency has to be increased or some error correction has to be inserted into the sampling process.

4.3 Analog→Digital conversion for feedback

The insertion of error correction brings us to the A/D converter. In A/D converters designed to sample signals with high accuracy the system is often based on a system feeding the sampled signal back into the analog domain. In analog domain the original and sampled pulse are then compared to determine the error, and compensation is performed.

The classical example to this is the $\Delta\Sigma$ modulator A/D converter, which is similar to the $\Delta\Sigma$ modulator D/A converter in that the calculations are performed in analog electronics, and the quantizer is changed to operate in discrete time, and thus sample the signal.

To allow for two noise shaping circuits in cascade the signal could be demodulated and then converted into a 1 bit signal again. This would remove the high frequency noise while recreating the signal resolution within the audio band. This method increases the complexity of the feedback dramatically as a filter and a A/D converter is required in the feedback path. Furthermore a demodulation filter is redundant as a demodulation filter is already employed for the power path.

When the high frequency quantization noise is removed the use of a second noise shaping circuit is not without problems. When using this implementation special care should be taken as the noise shaping circuit will inherently introduce some delay.

When the signal is sampled again, it can be downsampled to a sampling rate corresponding to the rate of the input. With the power output safely brought in to the digital domain a suitable control system can be employed.

Another system suggested by Kennet Andersen from Bang & Olufsen ICE-power A/S was to employ the PEDEC control system as a correction unit. This suggestion is a logical suggestion as the PEDEC unit is designed to correct misplacement of pulses in time. The basic principle is shown in Figure 4.3. When

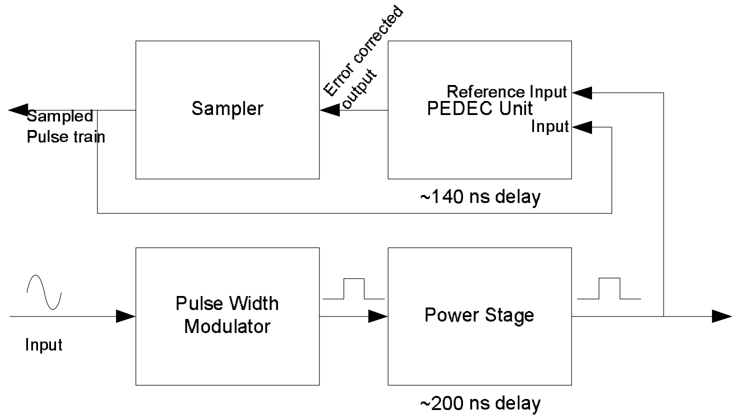

Figure 4.3: Correction of timing errors on sampling using PEDEC.

considering this scheme, it is evident that it will have some noise shaping properties, as the combination of sampling and pulse width correction will cause the high frequency noise to rise. Whether this will work is not sure, PEDEC has never been evaluated for this purpose, and to determine if it will work some basic properties like noise transfer function has to be determined. A major advantage over the $\Delta\Sigma$ modulator is that the PEDEC in its nature is always synchronized with the incoming pulse train, while the $\Delta\Sigma$ modulator is not. The PEDEC unit is furthermore beneficial as it provides correction, both in terms of pulse edges, but also amplitude. When implementing a PEDEC feedback the main contributor will be the demodulation filter which is outside the loop.

A major paradox of this idea is that one of the main reasons in designing a digital feedback system would be to eliminate analog control, eg. the use of the PEDEC system. If it is required by the sampling process nothing is gained except increased complexity, unless the amplifier performance can be increased significantly. This is true for the $\Delta\Sigma$ modulator as well as some analog circuitry is required.

The PEDEC solution described above is the only reasonable solution if a feedback of timing information is wanted. The $\Delta\Sigma$ modulator is not applicable for timing information as it requires demodulation whereas PEDEC works directly on the pulse edges.

4.4 Feedback of amplitude information

As the basic feedback of timing information was not satisfying, the use of A/D converters was discussed. When using a D/A converter, there is no reason to exclude the demodulation filter from the feedback, and the entire amplifier can thus be included in the control loop. An advantage by including the whole amplifier within the control loop is that the bandwidth within the loop can be reduced to audio frequency, and a far lower sampling frequency can be allowed. Furthermore, a far greater delay is allowable with respect to the phase margin, and commercial converters can thus be allowed.

The main problem when using commercially available A/D converters are their sampling frequency versus resolution. It is a trade-off, where the choice basically has to be made between one or the other. Analog devices offer a converter which can deliver a frequency of 105 MSps (Mega samples per second) at a resolution of 14 bit. This speed is not fast enough to sample the pulse edges themselves while it is sufficiently fast to sample the audio bandwidth.

The high resolution A/D converters are all based on a multi bit $\Delta\Sigma$ modulator. This design allows for higher resolution, but this resolution comes at a cost; a digital filter is required prior to downsampling the signal. This filter adds a significant group delay to the system. The delay is problematic as the total delay allowed within the control loop is limited by the required phase margin, and thus the bandwidth. Though, if commercially available A/D converters are used in the control loop they should be used on the demodulated audio output, and within audio bandwidth only. This limitation suits two purposes as it both reduces the bandwidth to a level allowed by commercial converters, and as a larger group delay can be allowed due to the lower bandwidth.

In Table 4.1 a number of A/D converters primarily from Analog Devices is listed. One of the main aspects is the price which range from \$5.60 to \$582.10(!) depending on the required specifications. This cost should be seen in comparison with the cost of a PEDEC control chip which is about \$2.

The choice of the A/D conversion strategy is dependent on the properties of the control system , and only small general guidelines can be given, however the resolution should be higher than in the system controlled to minimize distortion. This means that 20-24 bit will be required as the current WPWM and dAIM modulators are designed to a performance equivalent to CD performance; 16. bit.

4.5 Control Loop Design

The allowable bandwidth is directly influenced by the delay found in the open loop system. Thus the delay found in the system directly limits the possibilities for a control system.

The main property influenced by the delay is the phase margin. The phase margin is given by the angular distance from 180° (2π) to the point where the amplitude crosses 0 dB. This measure is related to the gain margin which is

Converter	Sampling rate	Resolution	SNR [dB]	THD[dB]	Group delay	Conversion time	Price [$]
AD6645	105 MSps	14 bit	75	-	-	9.5 ns	88.00
AD10678	80 MSps	16 bit	80.5	-	-	12.5 ns	582.10
AD677	100 kSps	16 bit	-	99	-	10 μs	32.45
AD7457	100 kSps	12 bit	71	84	-	1.6 μs	-
AD7651	100 kSps	16 bit	86	98	-	10 μs	8.24
AD7661	100 kSps	16 bit	89.3	107	-	10 μs	9.90
AD7680	100 kSps	16 bit	86	97	-	10 μs	5.81
AD1871	96 kSps	24 bit	105	95	460 μs @ 96 kHz	N/A	5.60
AD1877	48 kSps	16 bit	-	90	$\frac{36}{f_s}$= 750 μs @ 48 kHz	N/A	8.40
CS5340	192 kSps	24 bit	-	94	$\frac{12}{f_s}$=62.5 μs @192 kHz		-

Table 4.1: Specifications for a high end A/D converters used for audio, and high speed converters.

given by the distance from the crossing of 180° to 0 dB. For more information refer to [jan].

Most high end A/D converters rely on a multi bit $\Delta\Sigma$ modulator converter which is followed by a digital filter used for anti aliasing before downsampling the signal. The filter applied for demodulation causes a significant group delay. The converters furthermore have a conversion delay, which is insignificant in comparison to the group delay caused by the filter. These delays can be found in Table 4.1 for a range of converters. The delays in the feed forward system are

- Modulator
- Power stage

All these contributors are in the nano second range.

The preferable control design would be a design closing around the entire system, both modulator, amplifier and demodulation filter. This could be realized both using serial and parallel compensation, however the serial approach is preferable as a minimum of feedbacks are preferable due to the complexity of bringing the analog signal into digital domain.

According to [jan] a gain margin of 6 to 8 dB and a phase margin of 30 to 60° is recommendable. These numbers are given as a trade off between fast control, and low overshoot, and should be individually chosen for a given application. These boundaries can be used to estimate some limits for our control system. If the gain is considered to have a flat response within the audio band and roll off outside the audio band it can be assumed to have a bandwidth of the -3 dB frequency.

The equations below can be used to form a connection between the system delays and the bandwidth in the control system. In these equations γ_M represents the phase margin, f_{bw} the bandwidth, and the $t_{\text{delay, ...}}$ represents the delays. In Equation 4.1 the time corresponding to a given phase delay is determined by calculating the wavelength at the cut off frequency and multiplying it with the phase margin given as a fractional number. The maximum allowable delay in the control loop is then calculated in Equation 4.2 where the phase delay required for marginal stability is calculated by halving the wavelength (equivalent to 180° phase lag). The required delay for the wished phase margin, and the delay in the amplifier is then subtracted to obtain the allowed delay in the control system.

These equations are based on a coarse assumption where the dynamic phase lags within the system are replaced by constant time delays. This is however not incorrect for the power stage itself, as it can be considered a pure gain (with a delay). For the modulator the assumption might be worse, as no frequency analysis has been made of dAIM or WPWM. The 2$^{\text{nd}}$ order demodulation filter is not included in these equations as it has a cut off frequency well above the audio band (50 - 100 kHz), and thus causes almost no phase delay within the audio band.

A bandwidth of *at least* 20 kHz is required to obtain good performance within the audio band.

$$t_{\text{delay, phase margin}} = \frac{1}{f_{\mathrm{bw}}} \cdot \frac{\gamma_M}{360°} \tag{4.1}$$

$$t_{\text{delay, control}} = \frac{1}{2 \cdot f_{\mathrm{bw}}} - t_{\text{delay, amplifier}} - t_{\text{delay, phase margin}} \tag{4.2}$$

To apply these equations some information about the system is required. The delay in the amplifier has been determined during the design of the PEDEC system, and is approximately 200 ns. The delay in the modulator is determined by the number of latches within the design, and is given by the order: $\frac{n_{\text{order}}+1}{f_{\text{system}}}$. This is 40.7 ns for the current dAIM modulator running at 98.304 MHz. The delay has not been determined for the WPWM, but it is magnitudes larger due to the increased complexity. The bandwidth within the control system should be above 20 kHz to ensure proper audio reproduction, while not being too high to avoid noise, for this example 30 kHz is suggested. As explained earlier the demodulation filter is neglected.

$$t_{\text{delay, phase margin}} = \frac{1}{30\text{ kHz}} \cdot \frac{30^\circ}{360^\circ} = 4.17\ \mu\text{s} \tag{4.3}$$

$$\begin{aligned} t_{\text{delay, control}} &= \frac{1}{2 \cdot 30\text{kHz}} - (200\text{ ns} + 40.7\text{ ns}) - 4.17\ \mu\text{s} \\ &= 12.3\ \mu\text{s} \end{aligned} \tag{4.4}$$

This very simple analysis shows that there will at best be an allowable delay of 12.3 μs. When comparing this number to the group delays for A/D converters given in Table 4.1 it is evident that the most converters, especially the high resolution, are far too slow to provide a feasible solution for the closed loop system. The choice is thus dependent on whether a 16 bit converter or less is suitable. The system bandwidth can hardly be reduced further, and an increase will only make the problems worse. Similarly a larger phase margin will reduce the allowable delay as well.

If, instead, going back to the feedback of timing information the advanced A/D converter is unnecessary. If the PEDEC solution considered is in fact viable, a far lower delay can be obtained in the converter, however a far higher band width is required as well.

4.6 Discrete PEDEC

An obvious starting point for the implementation of a closed loop control system is the PEDEC system. The theory behind this system is well known, and thus the system just has to be discretized in order to have a starting point for a digital implementation.

The basic connection between the s-plane in analog domain, and the z-plane used in digital domain is given by Equation 4.5. In this equation T_s denotes the sampling period.

$$z = e^{s \cdot T_s} \tag{4.5}$$

Unfortunately expressions converted using this expression cannot be converted into a difference equation, and thus is not realizable in digital hardware.

Instead the bilinear transform can be used. This transform is done by substituting s with the expression given in Equation 4.6.

$$s = \frac{1 - z^{-1}}{1 + z^{-1}} \tag{4.6}$$

Due to the nature of the bilinear transform, the frequencies of an analog filter, and its responding digital filter is related by the relationship given by Equation 4.7.

$$\omega = 2f_s \tan \frac{\omega'}{2f_s} \tag{4.7}$$

The bilinear transformation is easily calculated for simple systems, the transformation for the reference filter, $R(s)$, given by Equation 2.35, is calculated in Equation 4.8 to 4.16.

$$
\begin{aligned}
R(s) &= \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} && (4.8)\\
\downarrow s &= 2f_s \frac{1 - z^{-1}}{1 + z^{-1}} && (4.9)\\
R(z) &= \frac{\omega_0^2}{\left(2f_s \frac{1-z^{-1}}{1+z^{-1}}\right)^2 + \frac{\omega_0}{Q}\left(2f_s \frac{1-z^{-1}}{1+z^{-1}}\right) + \omega_0^2} && (4.10)\\
&= \frac{\omega_0^2}{2^2 f_s^2 \frac{(1-z^{-1})^2}{(1+z^{-1})^2} + \frac{\omega_0}{Q} 2f_s \frac{1-z^{-1}}{1+z^{-1}} + \omega_0^2} && (4.11)\\
&= \frac{\omega_0^2 (1 + z^{-1})^2}{2^2 f_s^2 (1 - z^{-1})^2 + \frac{\omega_0}{Q} 2f_s (1 - z^{-1})(1 + z^{-1}) + \omega_0^2 (1 + z^{-1})} && (4.12)\\
&= \frac{\omega_0^2 (1 + 2z^{-1} + z^{-2})}{2^2 f_s^2 (1 - z^{-1})^2 + \frac{\omega_0}{Q} 2f_s (1 - z^{-2}) + \omega_0^2 (1 + z^{-1})} && (4.13)\\
&= \frac{\omega_0^2 (1 + 2z^{-1} + z^{-2})}{2^2 f_s^2 (1 - 2z^{-1} + z^{-2}) + \frac{\omega_0^2}{Q} 2f_s (1 - z^{-2}) + \omega_0^2 (1 + z^{-1})} && (4.14)\\
&= \frac{\omega_0^2 + 2\omega_0^2 z^{-1} + \omega_0^2 z^{-2}}{(2^2 f_s^2 \frac{\omega_0}{Q} 2f_s + \omega_0) + (-2 \cdot 2^2 f_s^2 + \omega_0) z^{-1} + (2^2 f_S^2 + \frac{\omega_0}{Q} 2f_s) z^{-2}} && (4.15)\\
&= \frac{\omega_0^2 + 2\omega_0^2 z^{-1} + \omega_0^2 z^{-2}}{(8f_s^3 \frac{\omega_0}{Q} + \omega_0) + (-8f_s^2 + \omega_0) z^{-1} + 2f_S (2f_S + \frac{\omega_0}{Q} 2) z^{-2}} && (4.16)
\end{aligned}
$$

A similar transformation can be made for the compensator $C(s)$ but this is unfortunately quite complex, as the compensator is of much higher order.

$$C(s) = K_c \frac{(\tau_{z1}s+1)\cdot(\tau_{z2}s+1)\cdot(\tau_{z3}s+1)}{(\tau_{p1}s+1)\cdot(\tau_{p2}s+1)\cdot(\tau_{p3}s+1)} \tag{4.17}$$

To avoid these tedious calculations, MATLAB was used to substitute the bilinear transform from Equation 4.6 into the compensator. Secondly the expression was split into nominator and denominator, and the zs were isolated in order to obtain the filter coefficients.

4.6.1 Choice of values for system

To design a PEDEC control system some properties have to be known and others decided in order to obtain a functional control system.

In Equation 4.18 the general transfer function for a 2$^{\text{nd}}$ order lowpass filter like the demodulation filter used is shown. When comparing with Equation 4.8 the Q and ω_0 can easily be determined By insertion of the values from Table 3.4, page 44.

$$T(s) = \frac{\frac{1}{LC}}{s^2 + s\frac{1}{CR} + \frac{1}{LC}} \tag{4.18}$$

The result is shown in Equation 4.19 and 4.20.

$$\omega_0^2 = \frac{1}{LC} \quad \rightarrow \quad f_0 = \sqrt{\frac{1}{LC}} = 389249 \text{ rad/sec } (= 61.951 \text{ kHz}) \tag{4.19}$$

$$\frac{\omega_0}{Q} = \frac{1}{CR} \quad \rightarrow \quad Q = CR\omega_0 = 0.513 \tag{4.20}$$

A note should be made to the Zobel network which is not included in this filter. The derived Q value is furthermore dependent on the load resistance used, which is chosen to 4 Ω in these calculations. Other values given by the amplifier itself are:

$f_{c,\text{idle}}$	251 kHz
t_p	$\frac{1}{351 \text{ kHz}} = 2.849\ \mu\text{s}$
t_0	270 ns
t_{delay}	$244\ \mu\text{s} = 24 \cdot \frac{1}{f_{sys}}$
f_s	98.304 MHz
K	40

Table 4.2: Values for PEDEC controller.

A note should be made to the sampling frequency used. It is *very* high, and this is unnecessary when considering the bandwidth. The choice of this very high sampling frequency is based on the implementation which is very similar to the analog implementation. The high sampling frequency eases the implementation significantly as the edge delay unit can be implemented in a way similar to the analog implementation. This very similar implementation might not be neccessary but was chosen to obtain a functional model quickly.

The values controlling the operation of the control system were chosen in cooperation with Kennet Skov Andersen from Bang & Olufsen ICEpower A/S, who is very experienced with analog PEDEC. These values are:

τ_{p1}	$\frac{1}{83\ \text{kHz}}$
τ_{p2}	$\frac{1}{83\ \text{kHz}}$
τ_{p3}	$\frac{1}{30\ \text{kHz}}$
τ_{z1}	$\frac{1}{5\ \text{kHz}}$
τ_{z2}	$\frac{1}{5\ \text{kHz}}$
τ_{z3}	$\frac{1}{3\ \text{MHz}}$
K_c	1000

Table 4.3: Values determined for control system.

4.6.2 Implementation

The values above are transformed into filter coefficients using MATLAB. The code used can be seen in Appendix F. During this transformation, the effect of frequency warping has been neglected as it is not relevant for frequencies that are low in comparison with the sampling frequency.

This results in the following expressions:

$$R(z) = \frac{7.772708419251300 \cdot 10^{10} + 1.554541683850260 \cdot 10^{11} z^{-1} + 7.772708419251300 \cdot 10^{10} z^{-2}}{1.990647120010819 \cdot 10^{16} - 3.965957255709562 \cdot 10^{16} z^{-1} + 1.975341226532419 \cdot 10^{16} z^{-2}} \tag{4.21}$$

for the reference filter, and a similar expression for the compensator. The compensator expression is not shown here as it includes some very long numbers.

The implementation is quite straight forward, as shown in 2.6. One of the main issues in the model is the A/D converter used in the feedback loop. The A/D converter used here is simply modeled by a transition from continuous to discrete time. The simulation can be made more realistic by adding quantization and delay to this ideal converter. These parameters can easily be selected to match the parameters of a real converter and the model can thus provide realistic results.

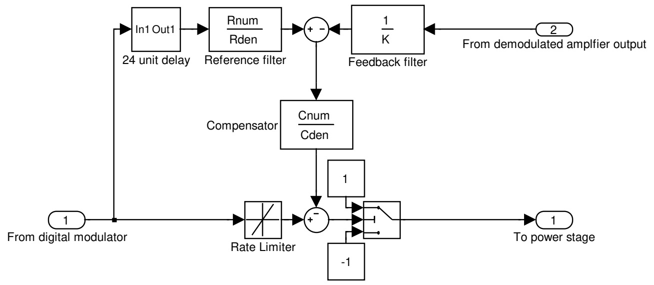

Figure 4.4: Implementation of PEDEC VFC3 control system in the digital domain.

The implementation of the edge delay unit can be seen in Figure 4.4. This implementation, which is very similar to an analog implementation, is implemented in the amplifier model developed earlier. The total system is shown in Figure 4.5.

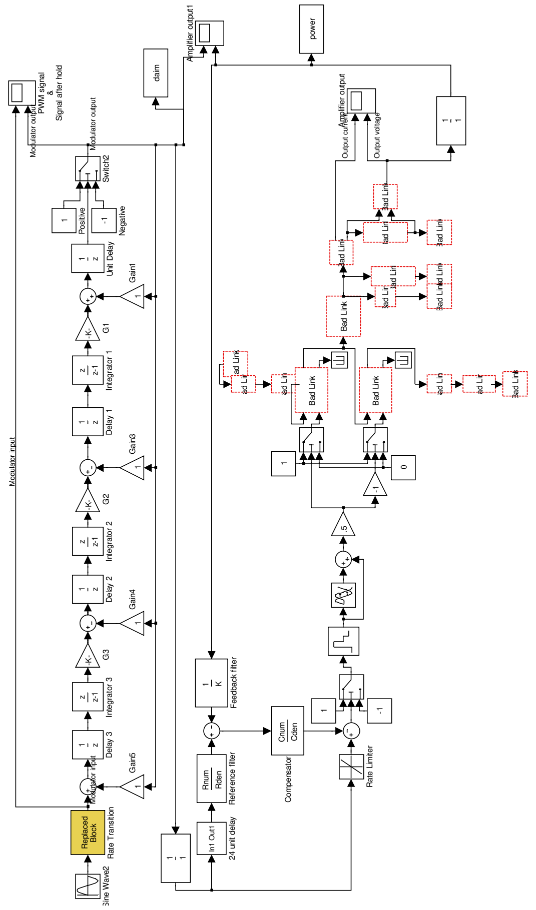

Figure 4.5: Implementation of PEDEC VFC3 control system in the amplifier model. The "missing" blocks are due to an incompatibility between MATLAB 6.5 and 7.0.

4.7 Simulation

The implemented system can be simulated using Simulink. To initialize the variables (gains and filter coefficients) the m-file shown in Appendix F.3 should be used. This file initializes the system with the values previous shown.

The first observation to be made when simulating the systems is that it runs at an incredible low speed. This is not unexpected, as the added signal processing is running at 98.304 MHz. The time required to make an FFT similar to the ones previous shown is 9(!) hours.

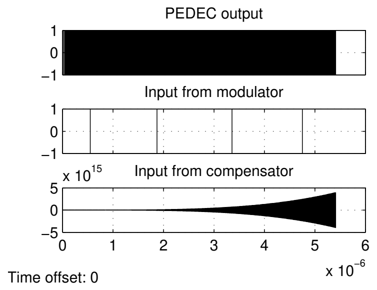

Figure 4.6: In- and output of the PEDEC block after correction of the input type mismatch in the rate limiter.

The simulations made show an output which is dominated by a large DC-output. The spectrums are shown in Appendix G. There are no traces of the 1st harmonic. This indicates a lack of connection somewhere in the model. To locate this error "scopes" were attached to the relevant nets. For the PEDEC implementation this was the in- and outputs of the PEDEC control systems, as the entire system was tested earlier. The reason appeared to be a mismatch of input formats in the "rate limiter" which caused the input to be zero. The in- and outputs after the correction is shown in Figure 4.6. Another quite strange property can be seen by the high frequency oscillations on the PEDEC output.

The correction of the rate limiter input did not solve the problems, and the output after this change was similar to the result before the change.

Another problem with the implementation is the filter lengths. The bilinear transform gives a 7th order filter for the compensator, and a 3rd order filter for the reference filter. These filter lengths are far from sufficient when considering the high sampling frequency used. This is easily seen in the bode plots, where the analog and the digital filters are compared. This comparison is shown for the reference filter, where the cutoff frequency can be seen to differ severely. This is shown in Figure 4.7. Here the frequency mismatch can easily be seen,

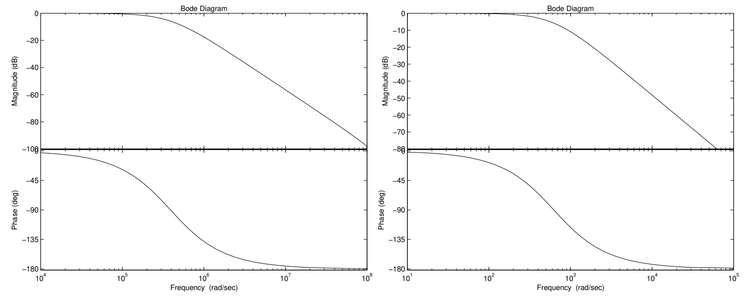

Figure 4.7: Bodeplot for reference filter. Left: Discrete, Right: Analog. Remark that the x-axis is given in rad/sec.

the filters have similar response, but the cut-off frequency differs a factor 100.

The mismatch in the filter responses will in theory cause the control system to saturate. However this should not cause a DC output, due to the design of the edge delay unit, which only allows a minor change of pulse widths.

4.8 Conclusion on Discrete PEDEC

Due to the available time frame it was impossible to make the implemented discrete PEDEC operate. The primary obstacles were the mismatch in filter response. This mismatch causes the control system to saturate, and thus the error correction to stop.

The filter response could be enhanced either by applying longer filters or by applying IIR which allows for a better response without increasing the required processing power.

The main limitation is however neither of the above given error sources. It is the requirement of an A/D converter. This requirement is a practical problem which does not influence the simulation. The problem is, as described in Section 4.4, that converters with low delay are very costly. This limitation has however no impact on the simulation, and can thus be neglected for simulations.

Another problem relevant to the implementation at hand is to reduce the sampling frequency in the control loop, to reduce the simulation time. This is also relevant from a hardware viewpoint, as these fast arithmetic operations are both complex and expensive to implement.

Finally the properties of PEDEC when implemented in discrete time have to be determined. The PEDEC is designed to operate in continuous time, and corrected the pulse train to zero error. When implemented in continuous time the pulse train error can not be corrected to zero but only to the nearest discrete sampling time. This operation will probably cause the PEDEC system to have some noise shaping properties as it will correct the mean to zero, rather than the momentary error. This property has not yet been researched, and needs further attention to determine the impact on the audio band.

Chapter 5

Conclusion

During this project, work has been done on two main types of feedback systems, one based on timing feedback, and one based on amplitude feedback. Currently none is operational. However the road ahead lies open.

The timing feedback control system based on the dAIM is quite promising. The major lack is a good transition from continuous to discrete time when converting the pulses. For this application, a solution based on the control system PEDEC seems promising, but this has yet to be proven.

When considering the systems based on feedback of amplitude information the road ahead looks somewhat more bumpy. First of all, the filters have to be redesigned for use in the digital domain, as the bilinear transformation has shown itself ineffective. Secondly a suitable A/D converter has to be chosen for the application. Given the converters available today, this is impossible for anything besides research, as the price prevents mass production.

For both system the PEDEC system has to be evaluated to prove whether it is usable in discrete time. Or another sampling method should be applied.

The three main topics for the choice of control systems are as earlier outlined cost, flexibility and performance.

The digital control system is clearly a winning idea when considering flexibility. The main advantage is that it will ease the implementation of control systems and thus shorten the time to market. Instead of changing components to obtain best possible performance, it can be done by simply loading new coefficients into a digital circuit.

This flexibility is a major trend in the audio market today, where simple, as well as advanced, functions are embedded in multi-function circuits. An example could be the integrated DSP processor and D/A converter for surround receivers, or the volume control, which now comes embedded into all sorts of devices. In future, a further increase in this trend will be seen and modulators like the dAIM or WPWM will be integrated into a DSP processor.

The digital audio circuits are subjects to Moores law [1] as well as the computer industry. This means that the processing power available in a standard stereo set will rise exponentially, and the allocation of processing power to the control system will be insignificant.

[1] The number of transistors on a piece of silicon will double every 18 month.

Regarding the cost, the implementation of the control systems treated here might seem unreasonable, but if we take a peek at the future it might not be that bad. When considering the future, the processing power required will undoubtedly rise, and the critical component will then be the A/D converter. The development of future A/D converters is harder to estimate as it depends on whether there will be application to drive this market towards better and cheaper converters. The converters available today, are typically targeted towards radio frequency applications, where cost is only of minor concern.

If the feedback of timing information alone is sufficient to obtain the required performance, the prospect is changed as it can be implemented at a cost similar to the cost of the analog control system today. The main properties requiring additional research are whether PEDEC can be used for resampling the pulses at a sufficient resolution, and the dAIM modulator is still researched to determine it's dynamic properties.

The performance of the digital control systems is not finally determined in this report, however there is only little doubt that they will lack performance in comparison with their analog counterparts. Regarding the feedback of timing information, this is mainly related to neglecting the demodulation filter and the perturbations on the power supply.

The PEDEC base amplitude information feedback will likely suffer from some noise originating from the quantizing of the continuous output pulses to the discrete time instances. The impact of this quantization noise still needs to be determined. It also needs to be determined whether or not it has noise shaping properties, and if it has, whether or not they leave the audio band unharmed.

This lack of performance might not be as bad as it seems, for many consumer applications the performance is not the primary concern, and for integrated audio chipsets used in those products the digital control system is still a viable solution when weighting the pros against the cons.

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Appendix A

Determining Fourier series for pulse train with blanking delay

A way to determine the distortion caused by the blanking delay is to develop the Fourier series for a pulse train with blanking delay in the transitions. This Fourier series can then be compared to the Fourier series for a standard pulse train. The general equation for Fourier series is given in Equation A.1.

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n \cos \frac{n\pi x}{L} + b_n \sin \frac{n\pi x}{L} \right) \tag{A.1}$$

The variables a_n and b_n in this equation are given by Equation A.2 and A.3.

$$a_n = \frac{1}{L} \int_c^{c+2L} f(x) \cos \frac{n\pi x}{L} dx \tag{A.2}$$

$$b_n = \frac{1}{L} \int_c^{c+2L} f(x) \sin \frac{n\pi x}{L} dx \tag{A.3}$$

In these equations $f(x)$ is assumed to be a periodic extension, of period $2L$ and c is a random offset in time.

The task is then to determine a sufficient number of a and b coefficients to obtain a sufficient model. For simplicity the pulse is assumed to have unity amplitude.

The solution is obtained by first removing the offset c from the integral limits.

$$a_n = \tfrac{1}{L} \int_0^{2L} f(x) \cos \tfrac{n\pi x}{L} dx \tag{A.4}$$

$$b_n = \tfrac{1}{L} \int_0^{2L} f(x) \sin \tfrac{n\pi x}{L} dx \tag{A.5}$$

As the pulse train has constant output within certain limits the integrals within a period can be split into a positive and a negative part. The new integral

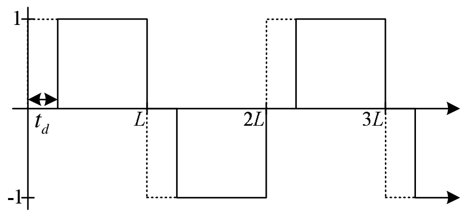

Figure A.1: Pulse train with added blanking delay.

borders are easily seen in Figure A.1.

$$a_n = \frac{1}{L}\left(\int_{t_d}^{L} \cos\frac{n\pi x}{L}dx - \int_{L+t_d}^{2L} \cos\frac{n\pi x}{L}dx\right) \tag{A.6}$$

$$b_n = \frac{1}{L}\left(\int_{t_d}^{L} \sin\frac{n\pi x}{L}dx - \int_{L+t_d}^{2L} \sin\frac{n\pi x}{L}dx\right) \tag{A.7}$$

These integrals can then solved by reference to Schaums Mathematical Handbook.

$$a_n = \frac{1}{L}\left(\left|\frac{L\cdot\sin\frac{n\pi x}{L}}{n\pi}\right|_{t_d}^{L} - \left|\frac{L\cdot\sin\frac{n\pi x}{L}}{n\pi}\right|_{L+t_d}^{2L}\right) \tag{A.8}$$

$$b_n = \frac{1}{L}\left(\left|\frac{L\cdot\cos\frac{n\pi x}{L}}{n\pi}\right|_{L+t_d}^{2L} - \left|\frac{L\cdot\cos\frac{n\pi x}{L}}{n\pi}\right|_{t_d}^{L}\right) \tag{A.9}$$

The equations are then simplified by removing variables eliminating each other.

$$a_n = \frac{1}{n\pi}\left(\left|\sin\frac{n\pi x}{L}\right|_{t_d}^{L} - \left|\sin\frac{n\pi x}{L}\right|_{L+t_d}^{2L}\right) \tag{A.10}$$

$$b_n = \frac{1}{n\pi}\left(\left|\cos\frac{n\pi x}{L}\right|_{L+t_d}^{2L} - \left|\cos\frac{n\pi x}{L}\right|_{t_d}^{L}\right) \tag{A.11}$$

These equations are then expanded.

$$a_n = \frac{1}{n\pi}\left(\sin\frac{n\pi L}{L} - \sin\frac{n\pi t_d}{L} - \left(\sin\frac{n\pi 2L}{L} - \sin\frac{n\pi(L+t_d)}{L}\right)\right) \tag{A.12}$$

$$b_n = \frac{1}{n\pi}\left(\cos\frac{n\pi 2L}{L} - \cos\frac{n\pi(L+t_d)}{L} - \left(\cos\frac{n\pi L}{L} - \cos\frac{n\pi t_d}{L}\right)\right) \tag{A.13}$$

Internal parenthesis are removed.

$$a_n = \frac{1}{n\pi}\left(\sin\frac{n\pi L}{L} - \sin\frac{n\pi t_d}{L} - \sin\frac{n\pi 2L}{L} + \sin\frac{n\pi(L+t_d)}{L}\right) \tag{A.14}$$

$$b_n = \frac{1}{n\pi}\left(\cos\frac{n\pi 2L}{L} - \cos\frac{n\pi(L+t_d)}{L} - \cos\frac{n\pi L}{L} + \cos\frac{n\pi t_d}{L}\right) \tag{A.15}$$

Variables eliminating each other are removed.

$$a_n = \frac{1}{n\pi}\left(\sin n\pi - \sin\frac{n\pi t_d}{L} - \sin n\pi 2 + \sin\frac{n\pi(L+t_d)}{L}\right) \tag{A.16}$$

$$b_n = \frac{1}{n\pi}\left(\cos n\pi 2 - \cos\frac{n\pi(L+t_d)}{L} - \cos n\pi + \cos\frac{n\pi t_d}{L}\right) \tag{A.17}$$

And sinusoidal elements giving constant output are removed.

$$a_n = \frac{1}{n\pi}\left(-\sin\frac{n\pi t_d}{L} + \sin\frac{n\pi(L+t_d)}{L}\right) \tag{A.18}$$

$$b_n = \frac{1}{n\pi}\left(1 - \cos\frac{n\pi(L+t_d)}{L} - \cos n\pi + \cos\frac{n\pi t_d}{L}\right) \tag{A.19}$$

These expression can then be rewritten into:

$$a_n = \begin{cases} \frac{2}{n\pi}\left(-\sin\frac{n\pi t_d}{L}\right) & \text{when odd,} \\ 0 & \text{when even.} \end{cases} \tag{A.20}$$

$$b_n = \begin{cases} \frac{2}{n\pi}\left(1 + \cos\frac{n\pi t_d}{L}\right) & \text{when odd,} \\ 0 & \text{when even.} \end{cases} \tag{A.21}$$

This concludes the derivation of equations for determining the coefficients for the Fourier series.

To verify the obtained result t_d and L was set to respectively 0 and π. When doing this, the correct result for an ordinary pulse signal was obtained.

As the derived expression are somewhat unhandy, a MATLAB implementation has been made. The implementation takes the inputs L, t_d, a signal length, and an approximation order which determines the number of coefficients calculated, and thus the number of iterations made on Equation A.1. The script then plots the spectras given by the coefficients, and the approximated signal. This implementation was used to verify the derived expressions, Figure A.2 shows an estimated pulse train with $L = 1$ and $t_d = 0.5$ approximated with 50 iterations. It is easy to see here that the approximated pulse has a blanking delay similar to the one shown in Figure A.1.

Another property worth looking at is the spectra. To obtain a plot illustrating the properties, the parameter t_d is changed to 0.1 while L and the number of iterations are unchanged. The spectra is shown in Figure A.3. The main observations to be made are that:

- There are no even harmonics.
- The uneven harmonics of the cosine spectra are sinc shaped, although inverted.
- Further investigation shows that reducing the, t_d/L-ratio stretches the frequency response while increasing it compresses the frequency response.

The signal can be translated into a single sine consisting of a phase and a time displacement. The general expression is shown in Equation A.22, which equals Equation A.1.

$$f(x) = \sum_{n=1}^{\infty} c_n \sin\left(n\pi t + d_n\right) \tag{A.22}$$

The amplitude, c_n, is given by Equation A.23 and the time displacement, d_n, by Equation A.24. The time displacement can be transferred into the phase, however this does not serve any purpose in this application.

$$c_n = \sqrt{a_n^2 + b_n^2} \tag{A.23}$$

$$d_n = \sin^{-1} \frac{c_n}{2a_n} \tag{A.24}$$

The spectrum for this series of sines is shown in Figure A.4, together with the time displacement.

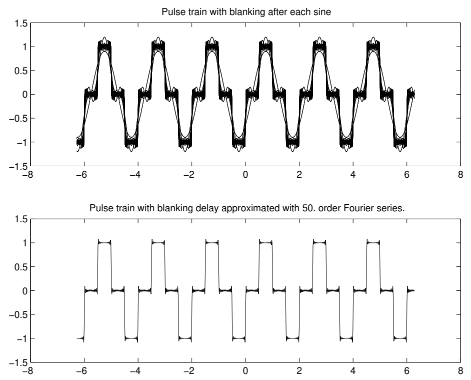

Figure A.2: Plot after each addition of each approximating sine (top) and 50. order approximation (bottom).

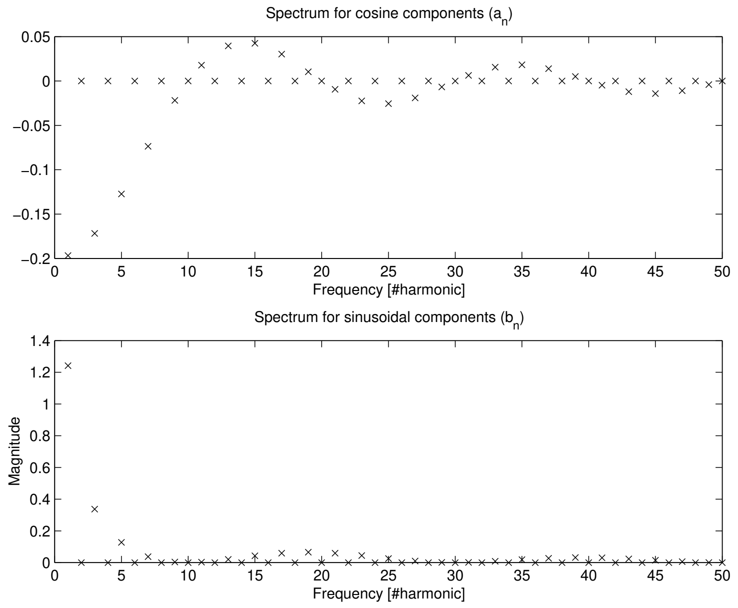

Figure A.3: Coefficients for cosine (top), and sine (bottom) components.

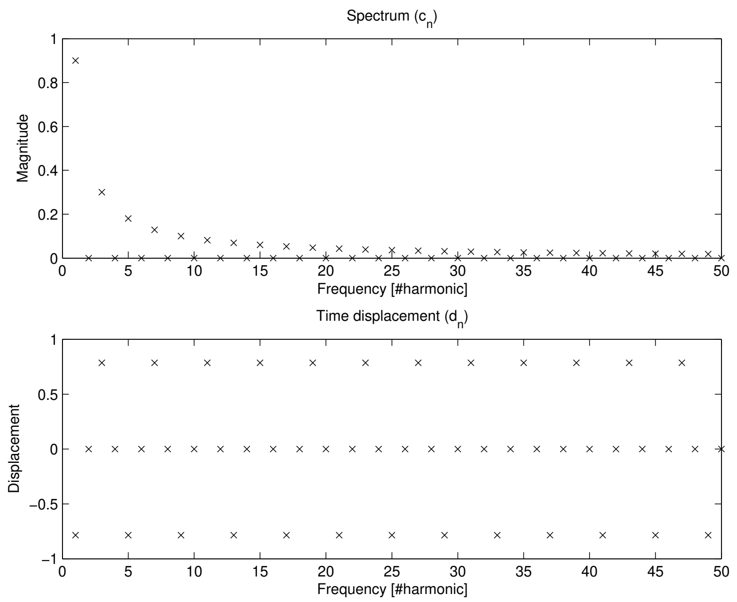

Figure A.4: Spectrum for sines (top), Time displacement (bottom). Parameters used: $L = 1$ and $t_d = 0.5$.

Appendix B

Measurement on power stage with, and without PEDEC

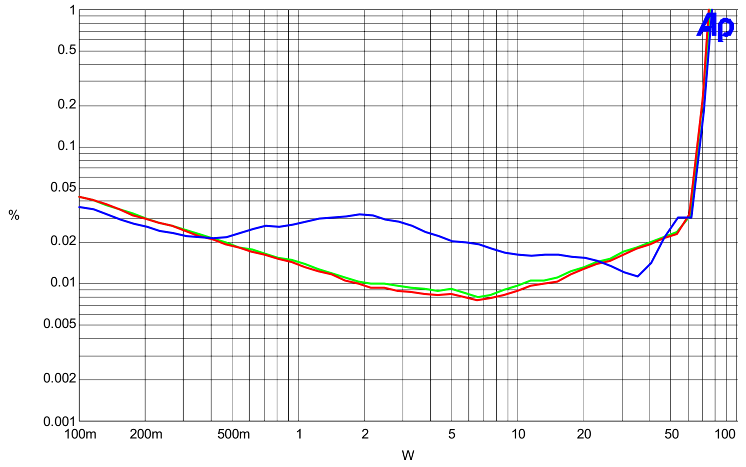

Figure B.1: THD+N vs. power with PEDEC control, green 100 Hz, red 1 kHz and blue 6.67 kHz. Taken from [And02]

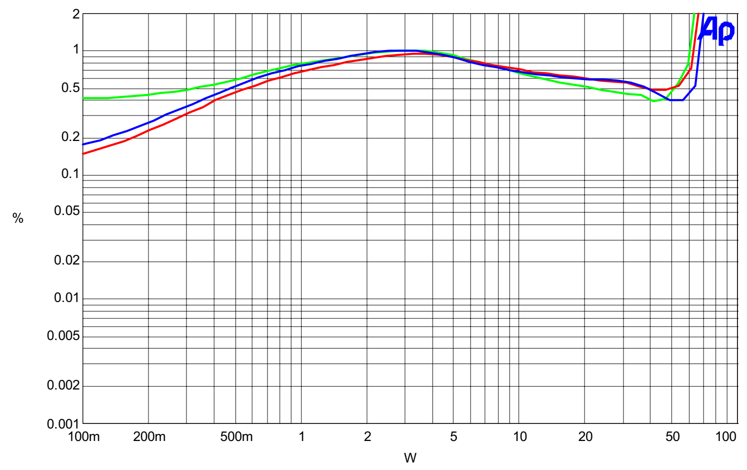

Figure B.2: THD+N vs. power without control, green 100 Hz, red 1 kHz and blue 6.67 kHz. Taken from [And02]

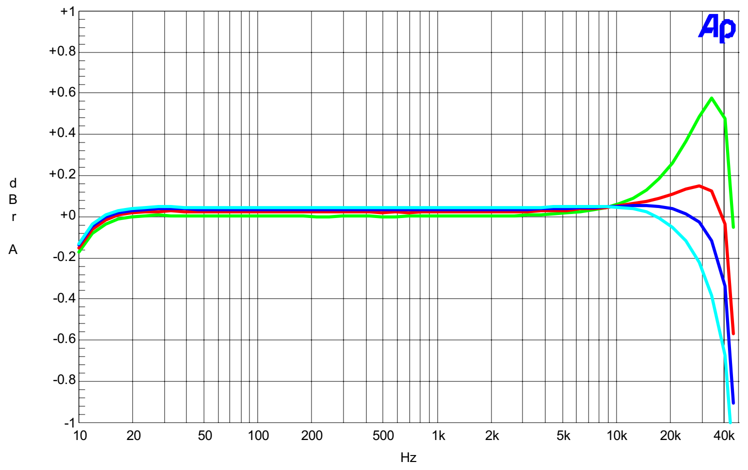

Figure B.3: Frequency response with PEDEC control, -20 dB 10 Hz - 48 kHz, green 4 Ω, red 8 Ω, blue 16 Ω and cyan open load. Taken from [And02]

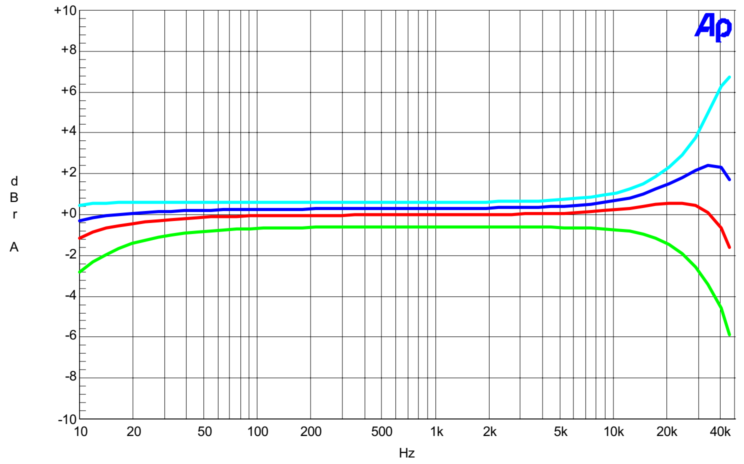

Figure B.4: Frequency response without control, -20 dB 10 Hz - 48 kHz, green 4 Ω, red 8 Ω, blue 16 Ω and cyan open load. Taken from [And02]

Appendix C

Open loop power stage simulations

C.1 100 Hz

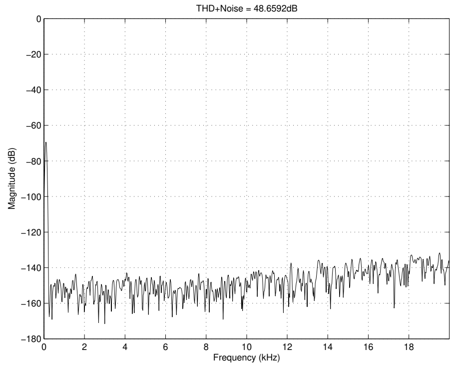

Figure C.1: Spectrum of power stage output, input 100 Hz, M=0.001 (-60 dB).

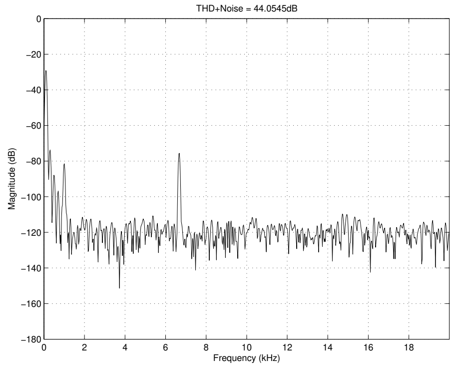

Figure C.2: Spectrum of power stage output, input 100 Hz, M=0.1 (-20 dB).

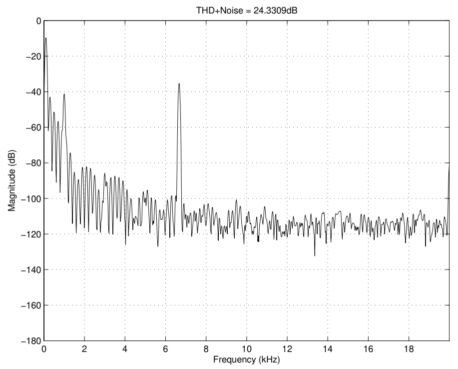

Figure C.3: Spectrum of power stage output, input 100 Hz, M=0.79 (-2 dB).

C.2 1 kHz

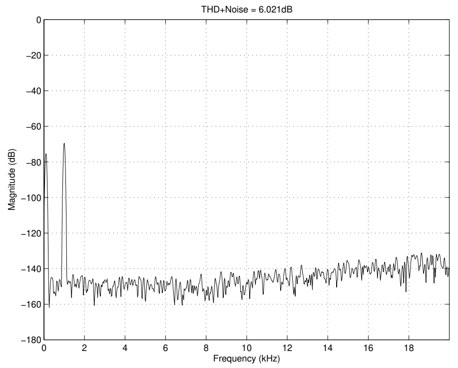

Figure C.4: Spectrum of power stage output, input 1 kHz, M=0.001 (-60 dB).

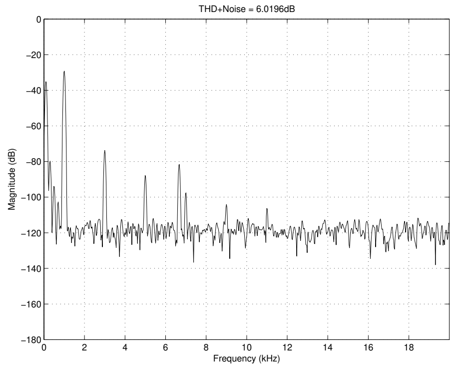

Figure C.5: Spectrum of power stage output, input 1 kHz, M=0.1 (-20 dB).

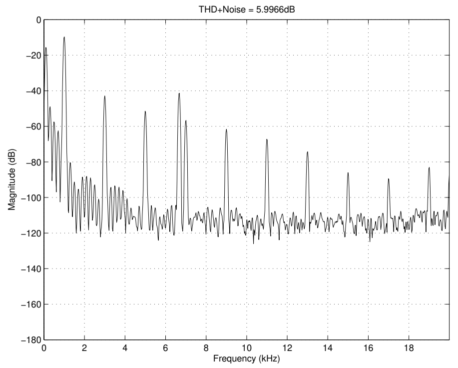

Figure C.6: Spectrum of power stage output, input 1 kHz, M=0.79 (-2 dB).

C.3 6.67 kHz

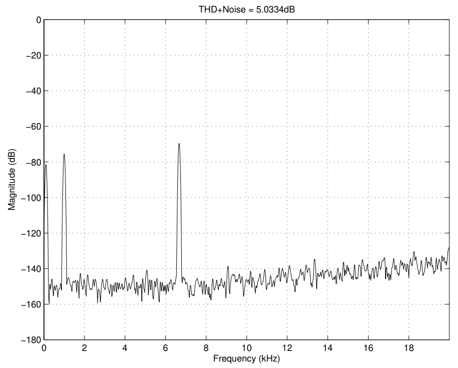

Figure C.7: Spectrum of power stage output, input 6.67 kHz, M=0.001 (-60 dB).

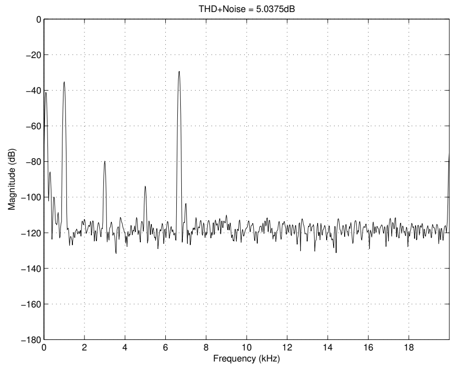

Figure C.8: Spectrum of power stage output, input 6.67 kHz, M=0.1 (-20 dB).

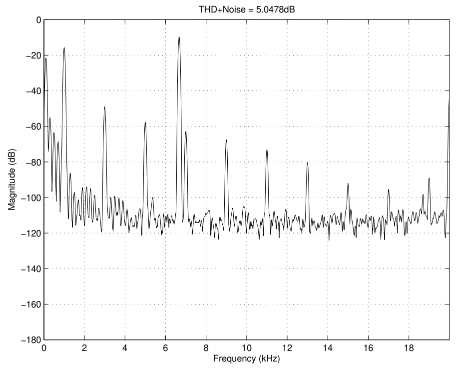

Figure C.9: Spectrum of power stage output, input 6.67 kHz, M=0.79 (-2 dB).

Appendix D

Power stage measurement results

D.1 First session

D.1.1 100 Hz

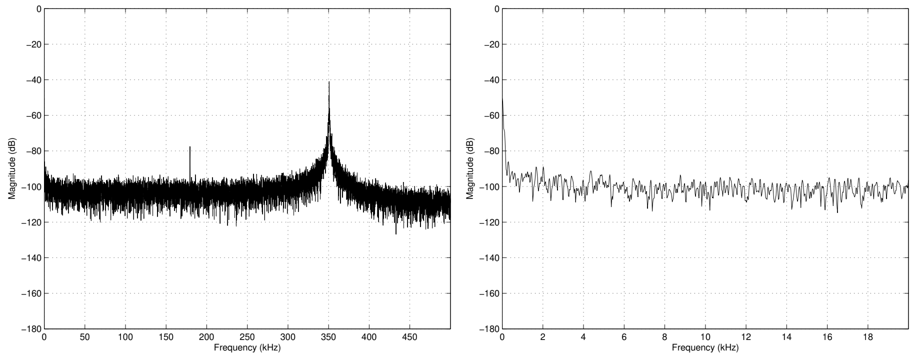

Figure D.1: Spectrum of power stage output, input 100 Hz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

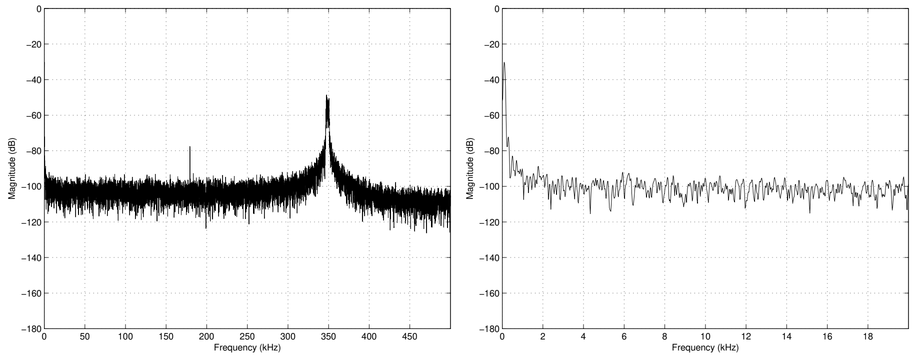

Figure D.2: Spectrum of power stage output, input 100 Hz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

D.1.2 1 kHz

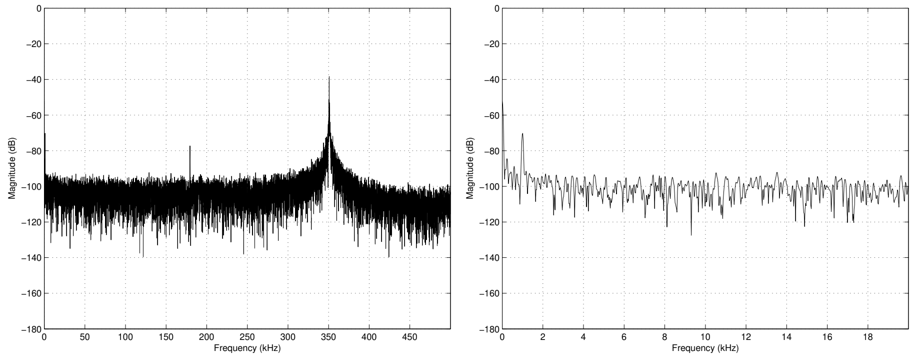

Figure D.3: Spectrum of power stage output, input 1 kHz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

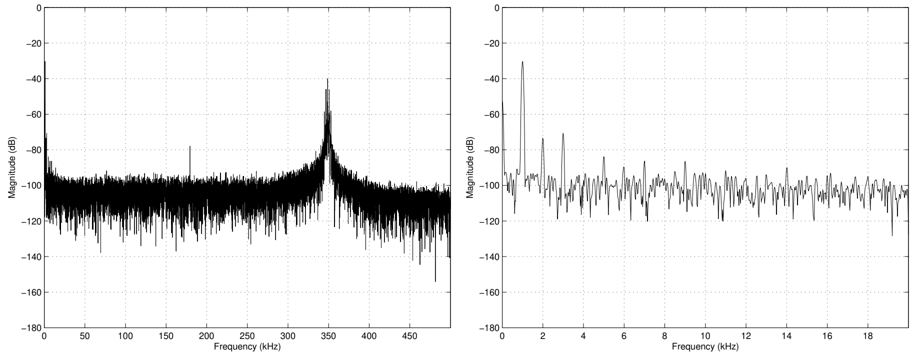

Figure D.4: Spectrum of power stage output, input 1 kHz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

D.1.3 6.67 kHz

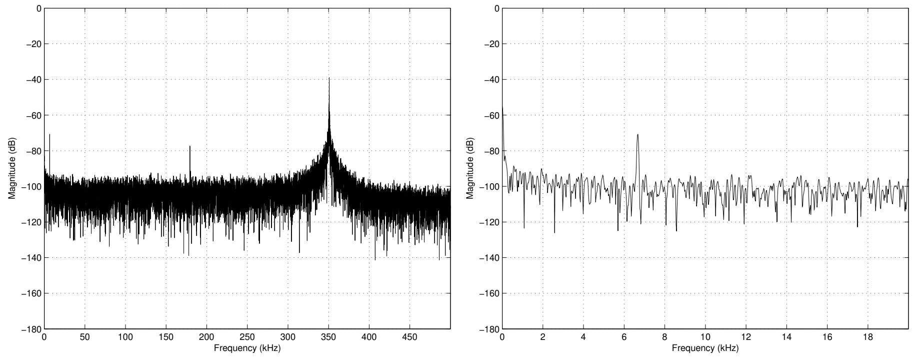

Figure D.5: Spectrum of power stage output, input 6.67 kHz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

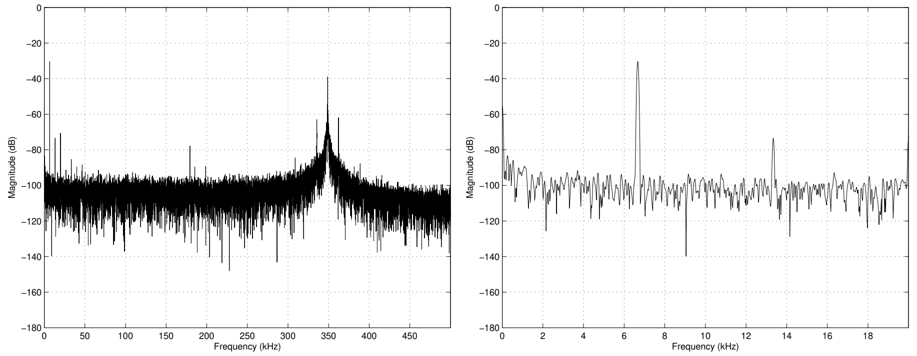

Figure D.6: Spectrum of power stage output, input 6.67 Hz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

D.2 Second session

D.2.1 100 Hz

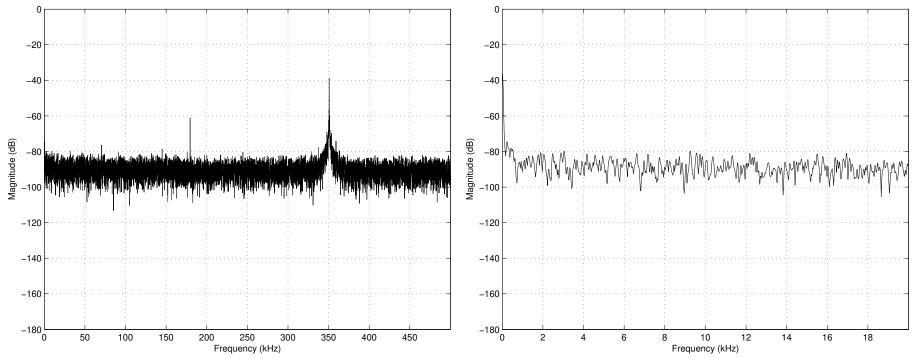

Figure D.7: Spectrum of power stage output, input 100 Hz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

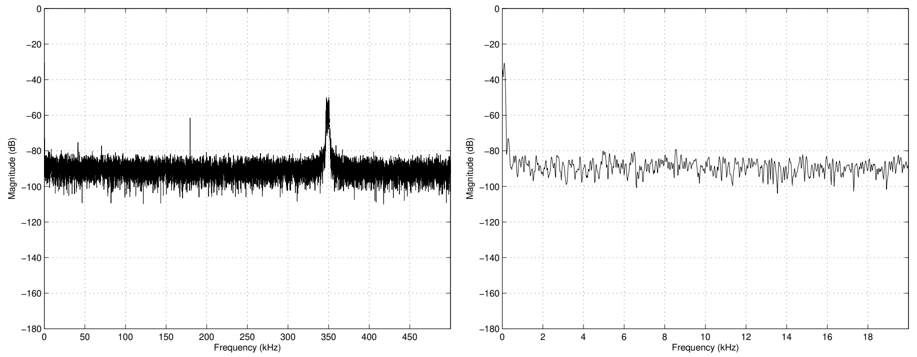

Figure D.8: Spectrum of power stage output, input 100 Hz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

D.2.2 1 kHz

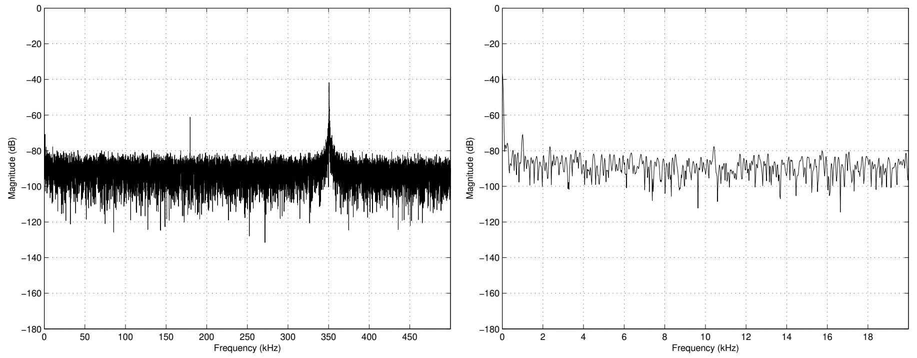

Figure D.9: Spectrum of power stage output, input 1 kHz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

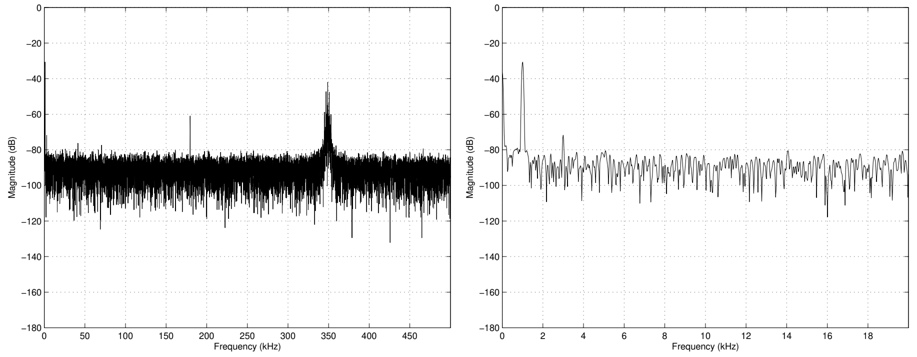

Figure D.10: Spectrum of power stage output, input 1 kHz, M=0.794 (-2 dB). Left: wide band, Right: audio band.

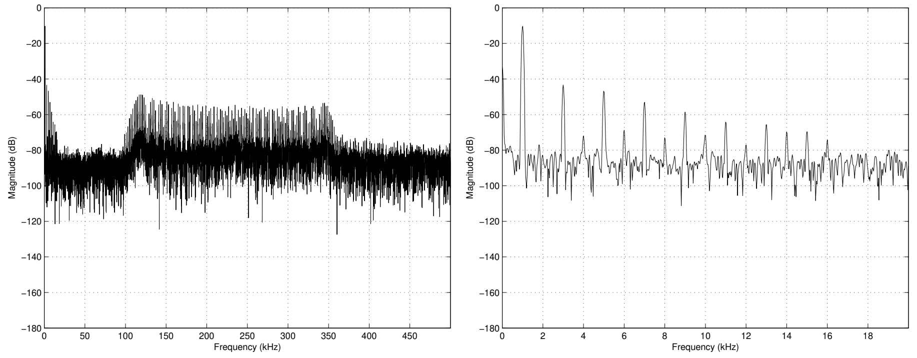

Figure D.11: Spectrum of power stage output, input 1 kHz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

D.2.3 6.67 kHz

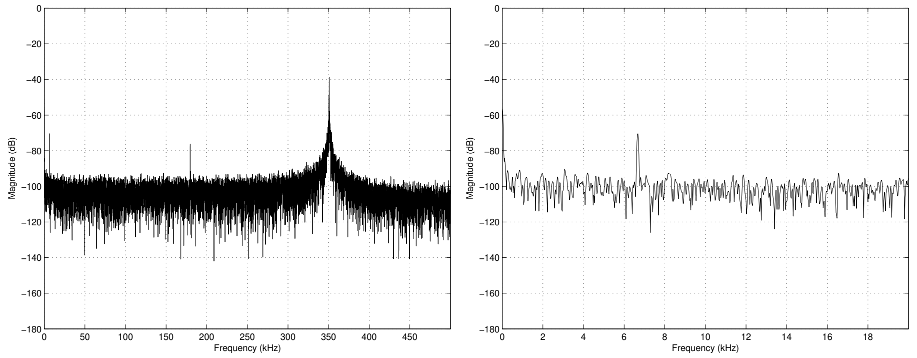

Figure D.12: Spectrum of power stage output, input 6.67 kHz, M=0.001 (-60 dB). Left: wide band, Right: audio band.

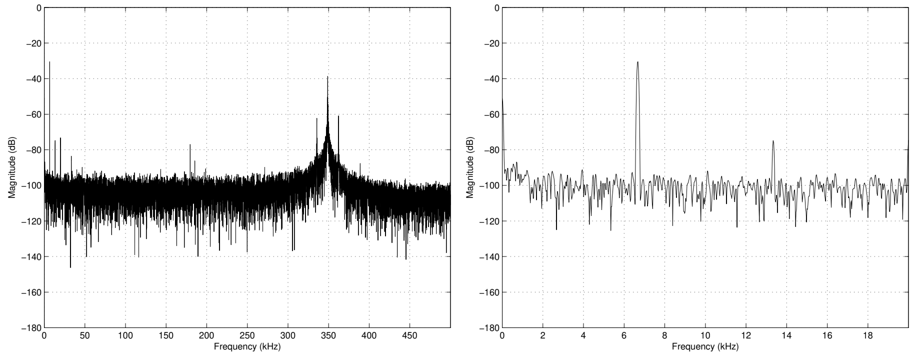

Figure D.13: Spectrum of power stage output, input 6.67 Hz, M=0.1 (-20 dB). Left: wide band, Right: audio band.

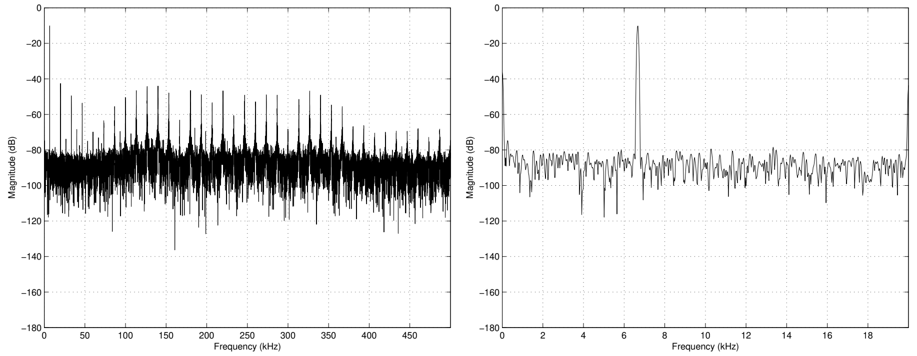

Figure D.14: Spectrum of power stage output, input 6.67 Hz, M=0.794 (-2 dB). Left: wide band, Right: audio band.

D.3 AP Measurements

D.3.1 THD+Noise Measurements

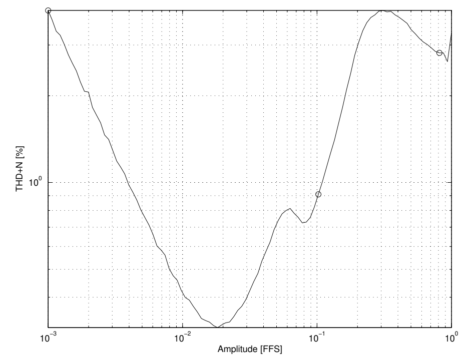

Figure D.15: THD+Noise vs. Amplitude, frequency: 100 Hz. -60, -20 and -2 dB are marked by ∘.

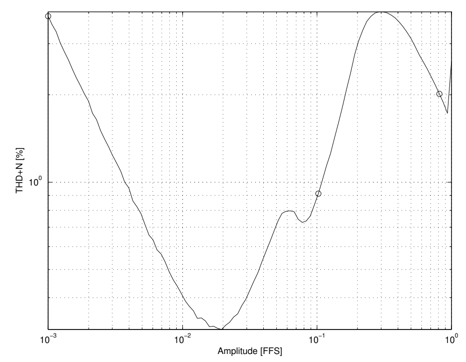

Figure D.16: THD+Noise vs. Amplitude, frequency: 1 kHz. -60, -20 and -2 dB are marked by ∘.

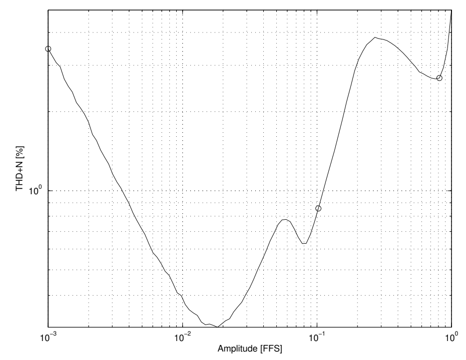

Figure D.17: THD+Noise vs. Amplitude, frequency: 6.67 kHz. -60, -20 and -2 dB are marked by ∘.

D.3.2 FFT Measurements

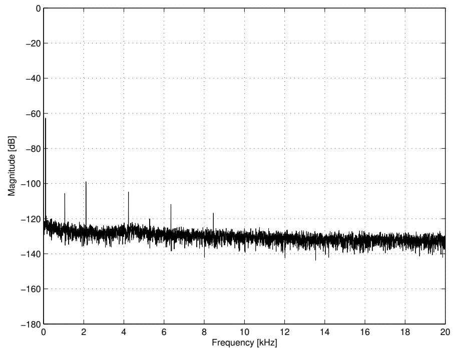

Figure D.18: FFT of amplifier output, frequency 100 Hz, amplitude -60 db.

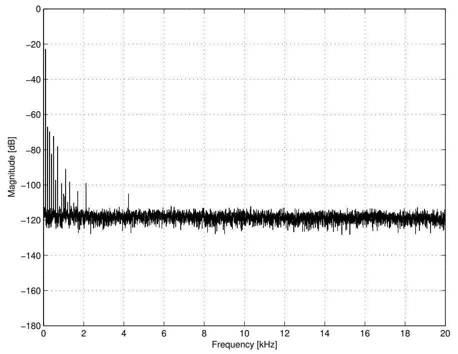

Figure D.19: FFT of amplifier output, frequency 100 Hz, amplitude -20 db.

Figure D.20: FFT of amplifier output, frequency 100 Hz, amplitude -2 db.

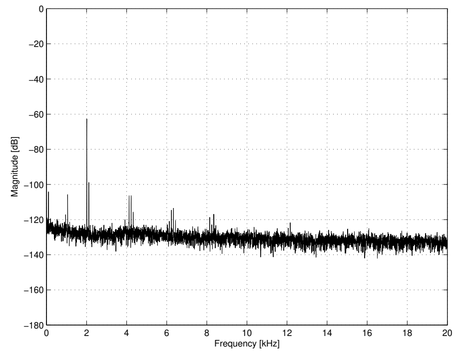

Figure D.21: FFT of amplifier output, frequency 2 kHz, amplitude -60 db.

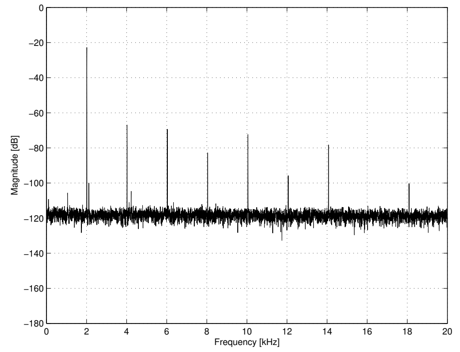

Figure D.22: FFT of amplifier output, frequency 2 kHz, amplitude -20 db.

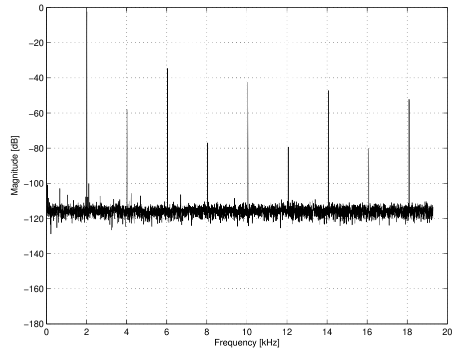

Figure D.23: FFT of amplifier output, frequency 2 kHz, amplitude -2 db.

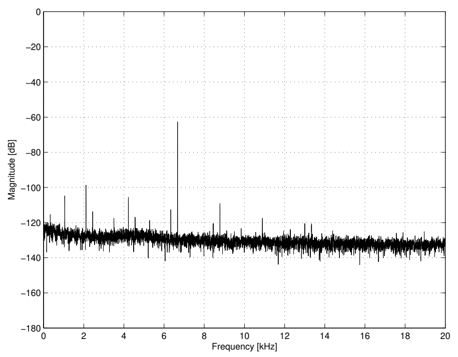

Figure D.24: FFT of amplifier output, frequency 6.67 kHz, amplitude -60 db.

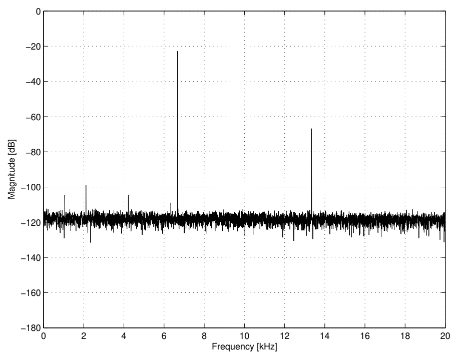

Figure D.25: FFT of amplifier output, frequency 6.67 kHz, amplitude -20 db.

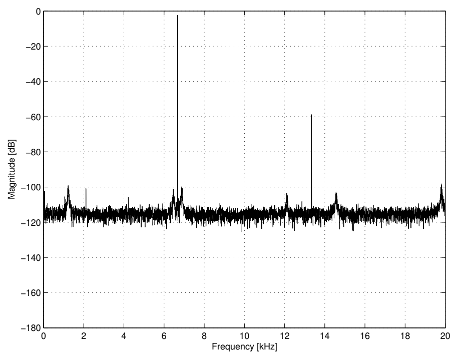

Figure D.26: FFT of amplifier output, frequency 6.67 kHz, amplitude -2 db.

Appendix E

FFT of amplifier based on power stage inserted into dAIM loop

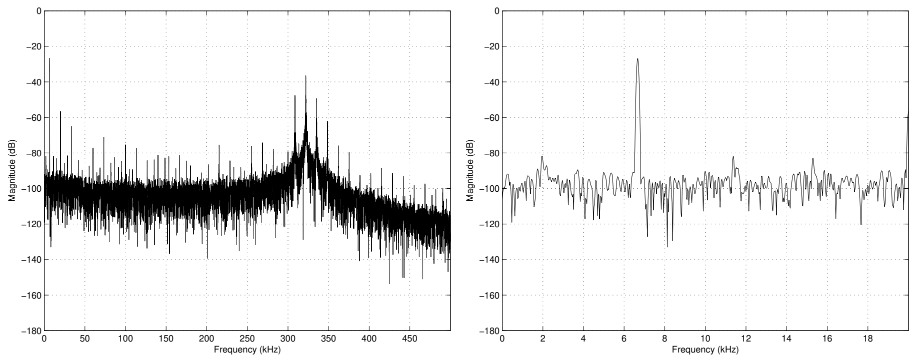

Figure E.1: Spectrum of amplifier output, input 6.67 kHz, M=0.1 (-20 dB). Left: Wide band plot, Right: Narrow band plot. FFT length: 13 k.

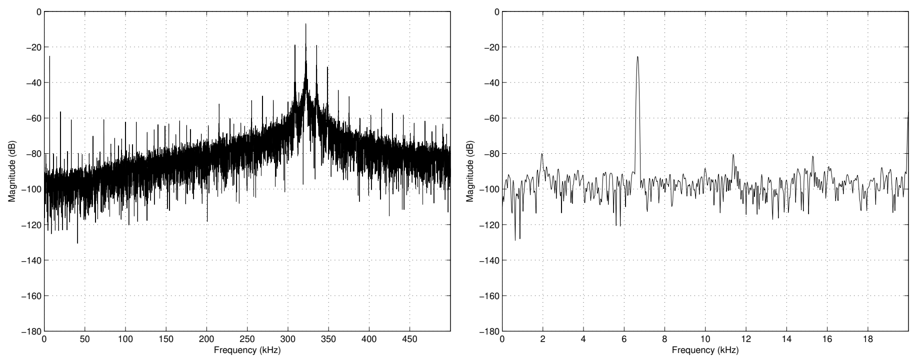

Figure E.2: Spectrum of modulator output, input 6.67 kHz, M=0.1 (-20 dB). Left: Wide band plot, Right: Narrow band plot. FFT length: 13 k.

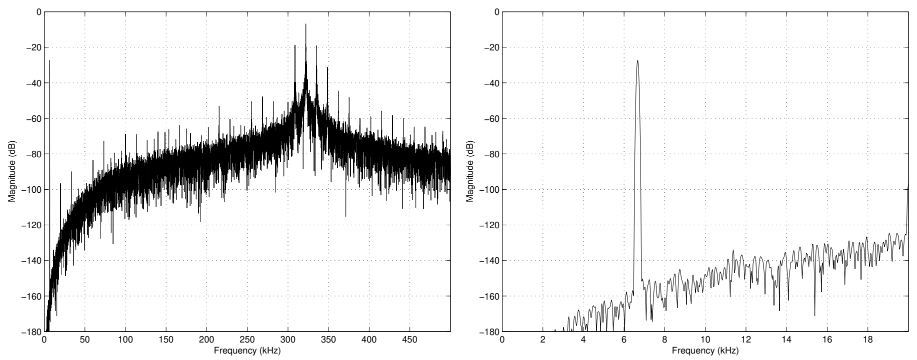

Figure E.3: Spectrum of feedback signal, input 6.67 kHz, M=0.1 (-20 dB). Left: Wide band plot, Right: Narrow band plot. FFT length: 13 k.

Appendix F

Generation of filter coefficients for Discrete PEDEC

F.1 Calculation of discrete reference filter

```
close all
clear all
clc

syms z fs                    %Variables for bilinear transform
s=sym(2*fs*(1-z^-1)/(1+z^-1))
                             %Expression for bilinear transform
syms omega_0 Q
                             %Variables for compensator are created
R=sym(omega_0^2/(s^2+(omega_0/Q)*s+omega_0^2))
                             %Expression for compensator
Rnew=subs(R,s,s);            %Bilinear transform
[cnum cden]=numden(Rnew)     %nominator and denominator are separated
cnum=subs(cnum,omega_0,389249);
cnum=subs(cnum,Q,.513);
cnum=subs(cnum,fs,98.304e6);
cnum=collect(cnum,z)

cden=subs(cden,omega_0,389249);
cden=subs(cden,Q,.513);
cden=subs(cden,fs,98.304e6);
cden=collect(cden,z)
```

F.2 Calculation of discrete PEDEC compensator

```
close all
clear all
clc

syms z fs                    %Variables for bilinear transform
s=sym(2*fs*(1-z^-1)/(1+z^-1))
                             %Expression for bilinear transform
syms tauz1 tauz2 tauz3 taup1 taup2 taup3 kc
                             %Variables for compensator are created
c=sym(kc*(tauz1*s+1)*(tauz2*s+1)*(tauz3*s+1)/...
          (taup1*s+1)*(taup2*s+1)*(taup3*s+1))
                             %Expression for compensator
cnew=subs(c,s,s);            %Bilinear transform
[cnum cden]=numden(cnew)     %Nominator and denominator are separated

cnum=subs(cnum,tauz1,1/(2*pi*83e3));
```

```
cnum=subs(cnum,tauz2,1/(2*pi*83e3));
cnum=subs(cnum,tauz3,1/(2*pi*30e3));
cnum=subs(cnum,taup1,1/(2*pi*5e3));
cnum=subs(cnum,taup2,1/(2*pi*5e3));
cnum=subs(cnum,taup3,1/(2*pi*3e6));
cnum=subs(cnum,kc,1000);
cnum=subs(cnum,fs,98.304e6);
cnum=collect(cnum,z)

cden=subs(cden,tauz1,1/(2*pi*83e3));
cden=subs(cden,tauz2,1/(2*pi*83e3));
cden=subs(cden,tauz3,1/(2*pi*30e3));
cden=subs(cden,taup1,1/(2*pi*5e3));
cden=subs(cden,taup2,1/(2*pi*5e3));
cden=subs(cden,taup3,1/(2*pi*3e6));
cden=subs(cden,kc,1000);
cden=subs(cden,fs,98.304e6);
cden=collect(cden,z)
```

F.3 Generation of nummerical values for Simulink model

```
% Filters wo. frequency warping

% close all;
% clear all;
plotopt=0;

Rnum=[77727084192513/1000 77727084192513/500 77727084192513/1000]

Rden=[19906471200108192513/1000 -19829786278547807487/500 19753412265324192513/1000]

if plotopt==1
    figure(1)
    dbode(Rnum,Rden,1/98.304e6)
end

Cnum=[2471688690782866921798540344053030911430375860563899100267120384189603105726621304153919606375/231584178474632390847141970017375815706539969331281128078915168015826259279872 ...
      -2355649414351244597069330712233218409720719331244373175542918102408724252267167821858295926375/57896044618658097711785492504343953926634992332820282019728792003956564819968 ...
       10971644421808716981559637024436505501406210141377120236282593456974627195459126804482396751875/231584178474632390847141970017375815706539969331281128078915168015826259279872 ...
       1628905744199364074140141872113576123260412484105096931757308061822962195510625/41137613933030151053874229563933762624568396640839496583715 2256 ...
      -11430151984076080289378832944730180737000007502738755452023725114444828786194682777664000591875/231584178474632390847141970017375815706539969331281128078915168015826259279872 2126401311146912379230326806579045260062036738187358377973441506602782414504734681116135542375/57896044618658097711785492504343953926634992332820282019728792003956564819968 ...
      -2013181128508092920268156187252247132796022473099654605507387730620876229614558890675359862375/231584178474632390847141970017375815706539969331281128078915168015826259279872]

Cden=[880907888472955703/140737488355328 ...
       880978257217133367/35184372088832 ...
       4405946817248331795/140737488355328 ...
       20 ...
      -4401724692597671955/140737488355328 ...
      -880556044752067383/35184372088832 ...
      -880626413496245047/140737488355328]

if plotopt==1
    figure(2)
    dbode(Cnum,Cden,1/98.304e6)
end
K=40;
t0=270e-9;
```

Appendix G

Measurements on Discrete PEDEC

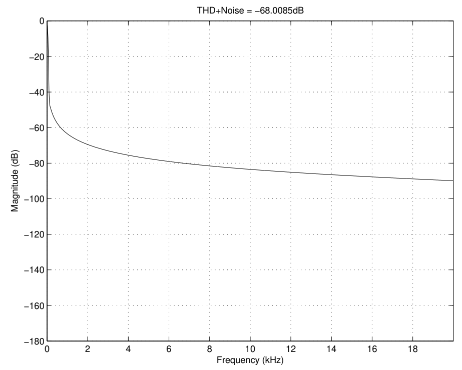

Figure G.1: Spectrum of power stage output, input 100 Hz, M=0.1 (-20 dB).

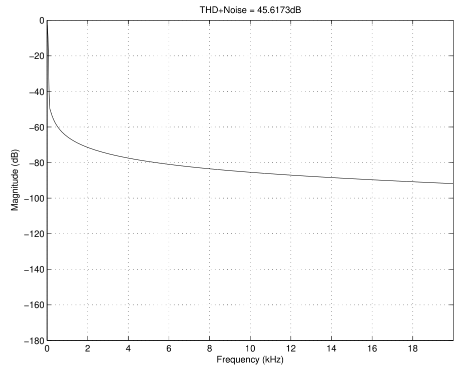

Figure G.2: Spectrum of power stage output, input 100 Hz, M=0.1 (-20 dB).