Low Power / Low Voltage Interface Circuitry for Capacitive Sensors

Design, Optimization and Applications

by

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Preface

This thesis is the result of the research I did on integrated CMOS design for smart sensors, as a part of my Ph.D. program. The work was carried out, at the Electronics Institute at the Technical University of Denmark (from 1. January 1996, Department of information Technology), in the period July 1, 1993 to December 31, 1996. The subject of my Ph.D. study was microelectronic design for smart sensors with emphasis on detailed circuitry aspects.

This thesis consists of 14 chapters grouped into four major parts: Theory, Applications, Appendices and Publications.

The Theory part gives a overview of the future of analog signal processing and establishes the limits of analog signal processing. It is pointed out that one of the interesting areas for analog signal processing in the future is integration with sensors. As an example capacitive micro mechanical sensors seems to have a bright future. It is also pointed out that low voltage and especially power signal processing is becoming more and more important. Limits and design methods of low power / low voltage design are treated thoroughly. Based on these methods new circuit blocks are presented. The theory of $\Sigma\Delta$ modulators are treated briefly and it is showed how electronic circuitry and a capacitive microphone can be combined to form an electromechanical $\Sigma\Delta$ modulator. This principle is an excellent example of a smart sensor. The Applications part gives examples of CMOS circuits that have been implemented in silicon. A low noise / low power amplifier for capacitive microphones is presented. And a Sigma-Delta modulator with extreme low power consumption is presented.

The Appendices part covers topics such as settling of amplifiers, noise in analog signal processing circuitry, matching of amplifiers to capacitive sources and analog signal processing in future CMOS technology. The presentation of these topics is done so they easily fit into the Theory part of this thesis.

The Publications part is an collection of enclosed copies of the papers that I have published during my Ph.D. study.

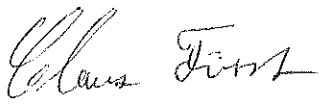
Acknowledgments

First of all I acknowledge the Ph.D. scholarship granted by the Danish Technical Research Council.
I would like to thank every member of the analog group of the Electronics Institute (now Department of information Technology) for many valuable discussions regarding analog circuits.

I would also like to thank Lars Stenberg at Microtronic for doing a thorough proof reading of the manuscript for this thesis.

Also I would like to thank MICROTRONIC and DELTA for their interest in my work.

And last I will thank my family for their support during my Ph.D. study.



Claus Fürst
Søborg, March 31, 1997

Abstract

This thesis focuses mainly on low power / low voltage interface circuits, implemented in CMOS, for capacitive sensors.

A brief discussion on demands and possibilities for analog signal processing in the future is presented.

Techniques for low power design is presented. This is done by analyzing power consumption of different amplifier topologies. Next low power features of different amplifier types are analyzed on transistor level. A brief comparison of SI circuits for low power application vs. SC circuits is presented.

Methodologies for low voltage design is presented. This is followed by a collection of time continuos and time discrete (switched) analog signal processing circuitry. Both the authors own designs and others are presented.

The theory of higher order $\Sigma\Delta$ modulators is presented. Design procedures are given. And it is shown how a $\Sigma\Delta$ modulator can be optimized for a low power consumption.

It is shown that the $\Sigma\Delta$ modulator is advantageous when embedded in a feedback loop with a mechanical sensor. Here a micro mechanical capacitive microphone. Feedback and detection circuitry for a capacitive microphone, is presented.

Practical implementations of low power / low voltage interface circuitry is presented.

It is demonstrated that an amplifier optimized for a capacitive microphone implemented in a standard $0.7\mu m$ CMOS technology compete well with a traditional JFET amplifier.

Furthermore a low power / low voltage $3^{rd} order$ $\Sigma\Delta$ modulator is presented. The $\Sigma\Delta$ modulator is was implemented in a standard $0.7\mu m$ CMOS technology.

The $\Sigma\Delta$ modulator was intended to be used in a feedback loop with a capacitive microphone.

Dansk Resumé

Denne Ph.D. afhandling omhandler interface kredsløb til kapacitive sensorer. Afhandlingen fokuserer hovedsageligt på lav effekt / lav spændings kredsløb implementeret i CMOS.

En introduktion til krav og muligheder for analog signal behandling i fremtiden præsenteres.

Teknikker beregnet for design af lav effekt analoge kredsløb præsenteres. Dette angribes på to niveauer. Først analyseres forskellige forstærker topologier. Dernæst analyseres flere forstærkere detaljeret på transistor niveau.

Endelig sammenlignes SI kredsløb med SC kredsløb ud fra deres lav effekt egenskaber.

Metoder til at designe lav spændings kredsløb præsenteres. Dette følges af en samling af tids-kontinuerte kredsløb, samt af tids-diskrete (switchede) kredsløb. Både forfatterens egne designs samt andres design præsenteres.

Teorien for højere ordens $\Sigma\Delta$ modulatorer præsenteres. Design procedurer for disse gennemgås og det vises, hvordan $\Sigma\Delta$ modulatorer kan optimeres til et lavt effekt forbrug.

Det eftervises at $\Sigma\Delta$ modulatorer med fordel kan benyttes, sammen med en mekanisk sensor, i et modkoblet system. I denne afhandling præsenteres kredsløbs konfigurationer til aftastning og modkobling af en mikromekanisk kapacitiv mikrofon.

Praktiske implementeringer af lav effekt / lav spændings kredsløb præsenteres. Det demonstreres, at en forstærker, optimeret til en kapacitiv mikrofon, kan konkurrere med en traditionel JFET forstærker løsning. Denne er implementeret i en standard $0.7\mu m$ CMOS teknologi.

Derudover præsenteres en tredje ordens $\Sigma\Delta$ modulator optimeret til et lavt effekt forbrug og en lav forsynings spænding. Denne er også implementeret i en standard $0.7\mu m$ CMOS teknologi.

Modulatoren var beregnet til at indgå i et modkoblet system med en mikromekanisk mikrofon.

Contents

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List of Abbreviations

A/D	Analog to Digital.
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor.
CDS	Correlated Double Sampling.
CMOS	Complementary Metal Oxide Semiconductor.
CMRR	Common-mode Rejection Ratio.
D/A	Digital to Analog.
FSM	Finite State Machine.
GBW	Gain Band Width.
JFET	Junction Field Effect Transistor.
MASH	Multistage Noise Shaping.
MOS	Metal Oxide Semiconductor.
MPW	Multi Project Wafer.
OTA	Operational Transconductance Amplifier.
PSRR	Power Supply Rejection Ratio.
SC	Switched - Capacitor.
$\Sigma\Delta$	Sigma-Delta.
SDM	Sigma-Delta Modulator.
SFG	Signal Flow Graph.
SI	Switched - Current.
S/N	Signal to Noise Ratio (power).
SNR	Signal to Noise Ratio in dB.
VLSI	Very Large Scale Integration.
VOA	Voltage Mode Operational Amplifier.

List of Notations

Physical parameters

Oxide thickness.

$$T_{OX}$$

Oxide capacitance per area.

$$C_{OX} = \frac{\epsilon_{S_i}}{T_{OX}}$$

Mobility.

$$\mu$$

Transconductance parameter, p channel transistor.

$$K_P = \mu_P C_{OX}$$

Transconductance parameter, n channel transistor.

$$K_N = \mu_N C_{OX}$$

Thermal voltage at 300^o K.

$$V_t = \frac{kT}{q} = 26mV$$

MOS transistor parameters

Channel width.

$$W$$

Channel length.

$$L$$

Under-diffusion length .

$$L_d$$

Threshold Voltage.

$$V_T$$

Signal analysis

Sequence.

$$x(k)$$

Z transformed of x(k).

$$X(z) = \sum_{k=0}^{N-1} x(k) z^k$$

Analog auto-correlation.

$$R_x(\tau)$$

Analog power spectral density.

$$S_x(f)$$

Sampled analog auto-correlation.

$$r_x(\tau)$$

Sampled analog power spectral density.

$$s_x(f)$$

Digital auto-correlation.

$$r_x(m)$$

Digital power spectrum.

$$s_x(e^{j2\pi f \Delta T})$$

Fourier pair.

$$g(t) \leftrightarrow G(f)$$

Analog Fourier transform.

$$G(f) = \int_{-\infty}^{+\infty} g(t) e^{-j2\pi ft} dt$$

Inverse Analog Fourier transform.

$$g(t) = \int_{-\infty}^{+\infty} G(f) e^{j2\pi ft} df$$

Analog Convolution.

$$g_1(t) \otimes g_2(t) = \int_{-\infty}^{+\infty} g_1(\theta) g_2(t-\theta) d\theta$$

$$g_1(t) g_2(t) \leftrightarrow G_1(f) \otimes G_2(f)$$

$$g_1(t) \otimes g_2(t) \leftrightarrow G_1(f) G_2(f)$$

Discrete Fourier Transform.

$$G[m] = \frac{1}{N} \sum_{k=0}^{N-1} g[k] e^{-jmk\frac{2\pi}{N}}$$

Inverse Discrete Fourier Transform.

$$g(k) = \sum_{m=0}^{N-1} G[m] e^{jmk\frac{2\pi}{N}}$$

ΣΔ Modulators

One-norm, i.e., sum of magnitude.

$$\|\cdot\|_1$$

Two-norm, i.e., square root of sum of squares.

$$\|\cdot\|_2$$

Infinity-norm, i.e., maximum magnitude.

$$\|\cdot\|_\infty$$

Noise Transfer Function, i.e. Z-transformed of ntf(k), see equation 4.2

$$NTF(z)$$

Signal Transfer Function, i.e. Z-transformed of stf(k), see equation 4.1

$$STF(z)$$

Error Transfer Function, i.e. Z-transformed of etf(k), see 4.8.1

$$ETF(z)$$

Noise Amplification factor as a function of quantizer gain, see equation 4.4

$$A(K)$$

Minimum of A(k).

$$A_{min}$$

One-norm of $ntf_K(k)$ versus quantizer gain, see equation 4.9

$$S(K)$$

Minimum of S(k).

$$S_{min}$$

Introduction

In recent years the widespread use of analog signal processing has rapidly decreased. This is due to the emergence of powerful, flexible and cheap digital signal processing replacing a vast amount of analog circuit functions. It is the authors believe that one of the fields remaining for analog signal processing circuitry in the future will be interface circuitry for sensors applications. The close integration of sensor and electronic circuitry is normally denoted a smart sensor.

Furthermore, it is the authors beliefe that low power / low voltage signal processing will be of enormous importance in the near future. This is driven by an wish for portable battery driven electronic systems.

Until now signal processing implemented as analog micro-electronic circuits has not seen the same dramatic improvement as digital circuitry. New micro electronics technologies with very small feature sizes has a potential for pushing the limits of power requirements and obtainable gain bandwidths GBW for analog signal processing. As these new opportunities just have emerged a methodology for low power design must be developed to unleash the advantages. In this thesis an attempt is made to present a design methodology for low power analog microelectronics design.

As future electronic systems will have to operate on battery driven low supply voltages, design techniques for low voltage circuitry has to be developed. This has to some extend already happened but these techniques have not spread among analog designers. In this thesis a collection of low voltage designs and techniques is presented. Both the authors own design and others are presented. It should be emphasized that low voltage does not implies low power consumption for analog signal processing circuitry. For low power analog signal processing a high power supply voltage is optimal. The low voltage power supply is forced upon the designer.

Analog interface circuitry electronics will as stated earlier be of enormous importance in the future. This interface electronics could be: buffers, amplifiers, A/Ds, D/As etc. Among A/D converters the $\Sigma\Delta$ A/D converter is the most interesting at the moment. It has the very desirable features of being inherently linear and relatively insensitive to matching. Furthermore, these types of converters have very useful features when combined with mechanical sensors. This is especially seen when combined with a mechanical sensor in a feedback loop.

Part I

Theory

Chapter 1

Smart Sensors & The Future of Analog Signal Processing

Since the 20's analog signal processing has played a major role in signal processing. Signals were mainly processed in the analog domain. This is now changing. The evolution of VLSI CMOS technologies has had a dramatic impact on signal processing. Cheap and powerful digital chips is at the moment taking over the role as the signal processing unit. Even if the analog technique also has undergone an enormous integration it is a fact that in the future most signal processing will be done in the digital domain. This leaves us with the question. What will be left for analog designers to do ?
In this chapter we will try to point out in which areas analog signal processing is still needed [1]. To see that we will have to discuss what have been the reasons for replacing analog signal processing with digital signal processing. This is summarized in table 1.1. Programmable digital circuitry makes digital signal processing very flexible. On the opposite analog circuitry design is very specific and not flexible. another advantage of digital design is the high degree of automation in the design phase. This is not the case of analog design. Analog design is furthermore more area consuming than digital design. The last point of the table is power consumption for analog and digital design. This actually sets the limits to what kind of analog signal processing that will be advantageous to replace by digital ditto. This will be discussed in the next section. Then we will resume to the areas where analog design still is advantageous. And last we will give a short introduction to one of the few remaining areas where analog signal processing hardly will be replaced signal processing. This is the area of smart sensors.

The last part of this chapter is a discussion of what analog designers can expect from CMOS technologies in the near future.

1.1 Signal Processing and Power

We will first give the reasons why low power signal processing is so interesting and then we will compare power consumption of analog vs. digital signal processing.

Table 1.1: Features of analog vs. digital signal processing.

Features	*Analog*	*Digital*
Flexibility	*low*	*high*
Automation	*low*	*high*
Area	*high*	*low*
Testability	*difficult*	*automated*
Parameter space	*infinite*	*finite*
Power consumption	*?*	*?*

1.1.1 The Need for Low Power Signal Processing

The need for low power signal processing is mainly due to the increasing importance of portable equipment. The main technology drivers for low power electronics in the past years, have been :

The 60's : Biomedical electronics
The 70's : Hand held calculators and watches
The 80's : Portable Computers
The 90's : Portable telecommunication equipment

The question is then what will be the main technology driver beyond year 2000 ? A guess could be body worn equipment. I.e. small personal and multifunctional electronics. As we see from the past it is true that portable equipment has been responsible for the effort to develop low power electronics. It is my postulate that this will continue. But the emphasis on one special product will probably not continue. Instead there will probably be several technology drivers beyond year 2000. All related as portable equipment. The conclusion on that must be that low power electronics will be of enormous importance in the future.

This forces us to face the power crisis.

What is the Power Crisis ?

First we will have to resume some of the major trends in IC technology in the last 3 decades.

Number of components : increases 10 x in 10 years
Clock frequency : increases more than 10 x in 10 years
Power reduction : decreases 10 x in 8 years

From these we se that :

Power per chip area : increases 8 x in 10 years

This means that if now effort is done then the power dissipated per chip area will increase by a factor of 8 every 10 years. Eventually the limit of maximum dissipated power per chip area will be reached. This is not a distant future. For portable equipment the increasing power dissipation of processing units has another impact. Here the power crisis is synonym of less power-on time. The expected battery lifetime is expected to increase 30-40 % in the next 5 years. The projected processing unit power consumption (Source : Intel) is shown in 1.1

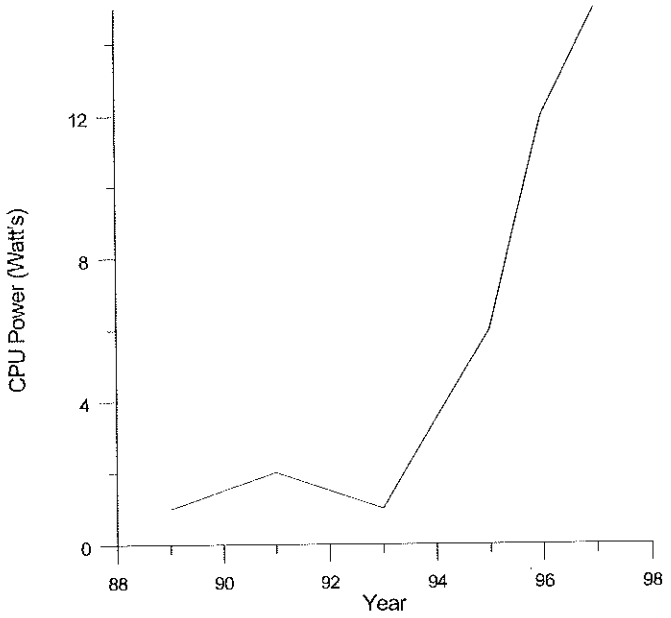

Figure 1.1: Projected processing unit power consumption, source Intel

We have now seen how an important issue low power electronics will be in the near future.

The next question is then, is digital signal processing or analog signal processing favorable in terms of power ?

1.1.2 Power for Analog Signal Processing vs. Power for Digital Signal Processing

It can shown that the theoretical limit of power per pole for analog signal processing is :

$$P_{min} = 8kT \cdot f \cdot S/N \tag{1.1}$$

This equation states that for a signal to noise ratio of S/N and a signal frequency of an analog signal processing system will minimum use P_{min} power. What we see from this is that an analog signal processing system has a very steep dependence of S/N (see Fig. 1.2) i.e. it is very expensive in terms of power consumption to achieve a large S/N. In chapter two the dependence of power consumption of S/N for analog signal processing is developed.

This leads us to the question. How strong is the dependence power consumption and S/N for digital signal processing ?

The power needed to process a signal in the digital domain is (see chapter two):

$$P_{min} = m \cdot f \cdot E_{tr} \tag{1.2}$$

Where :

f = signalbandwith

m : is the number of gate transitions per period 1/f.

E_{tr} : energy per transition.

As we see from equation 1.2 the dependence of the S/N is very weak compared to the analog power requirements.

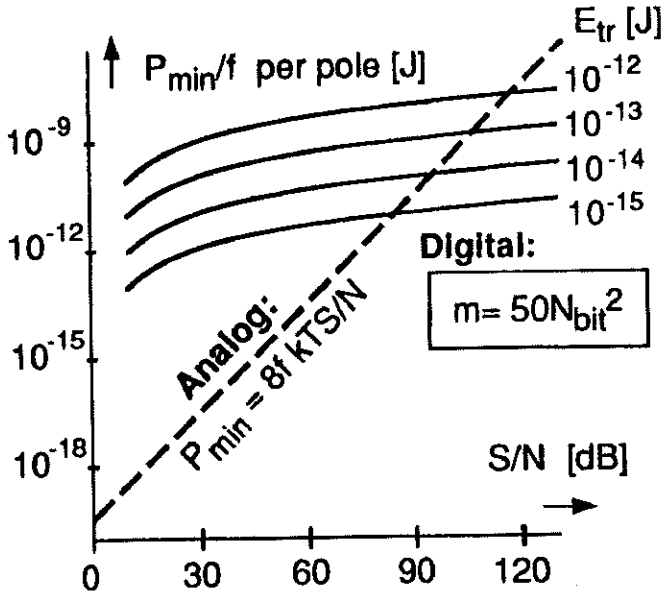

Figure 1.2: Analog vs. digital power consumption

In Fig. 1.2 the two dependencies are plotted against each other. This figure has been taken from [2]. What is very interesting is the value of S/N where it is more effective in term of power consumption. It seems that this limit is approximately around 80dB.

1.2 The future of analog signal processing

The future of analog signal processing will be strongly connected to the microelectronics technology of the future. In this section we will discuss what will be the areas left for analog signal processing and we will give a bid on what will be the microelectronics future technology. Three areas will still be interesting for analog designers.

1.2.1 Low Precision Signal Processing

As seen from Fig. 1.2 below S/N of approximately 80dB it is advantageous, in terms of power dissipation to process signals in the analog domain. Above 80dB it is the digital domain that is most advantageous. This limit will probably move towards a lower S/N

in the years to come. Many people share the opinion that one of the future areas of analog signal processing will be ultra low power signal processing of low precision. One example is neural networks.

1.2.2 High Frequency Signal Processing

The sampling criteria says that the sampling frequency has to be twice the bandwidth of the signal. This and the fact that sampled analog/digital signal processing circuits in fact are processing square waves. A sampled and held sine wave contains a lot of harmonics. This means that a sampled system will have to process frequencies one decade above the frequency of the signal itself. So a time continuos analog signal processing system will always be able to process frequencies one decade above the ones of sampled systems. This is the second area where analog signal processing has it future.

1.2.3 Interface circuitry

As most signal processing in the future will be performed in the digital domain there is a need to interface to the "real world" which in its nature is analog. This interfacing is of primarily A/D and D/A converters. But also impedance converters amplifiers etc. will still be used as conversion circuitry for electrical signals obtained from sensors. Smart sensors is the 3^{rd} area where analog signal processing has its future.

1.3 Smart Sensors

In recent years silicon as a sensor material has been investigated. It seems very promising as it permits the integration of the sensing element and the signal processing circuit on one chip, the so-called 'smart sensor' (see [3]).

1.3.1 Transducers

A transducer is defined a unit that converts a signal from one energy domain to another. Energy domains can be :

Radiant signals
Mechanical signals
Thermal signals
Magnetic signals
Chemical signals
Electrical signals

Normally the primary energy domain is non electrical and a sensor converts the energy into a representation in the electrical domain where it can easily be processed. The conversion from the electrical domain to non electrical is done by an actuator. Sensor and actuator are normally denoted the common name transducers.

1.3.2 Smart sensors

In a traditional sensor system the signal acquisition (the basic signal processing) is normally performed very close (physically) to the sensor. The more sophisticated signal processing is normally not included in the sensor itself. An example could be a capacitive microphone where the signal is being A/D converted. In close proximity of the microphone an impedance converter assure that the signal is not disturbed. The A/D conversion is then performed close to for instance a digital signal processor. The trend is that more of the signal processing moves closer to the sensor. It could for instance be a microphone with direct digital output. This also opens for a lot of other possibilities. Correction of distortion, drift, temperature drift etc. can be directly added to the sensors. In the ultimate merge of sensor and signal processing, the sensor and the electronic circuitry is processed on the same chip. A new term has emerged: Smart sensors.

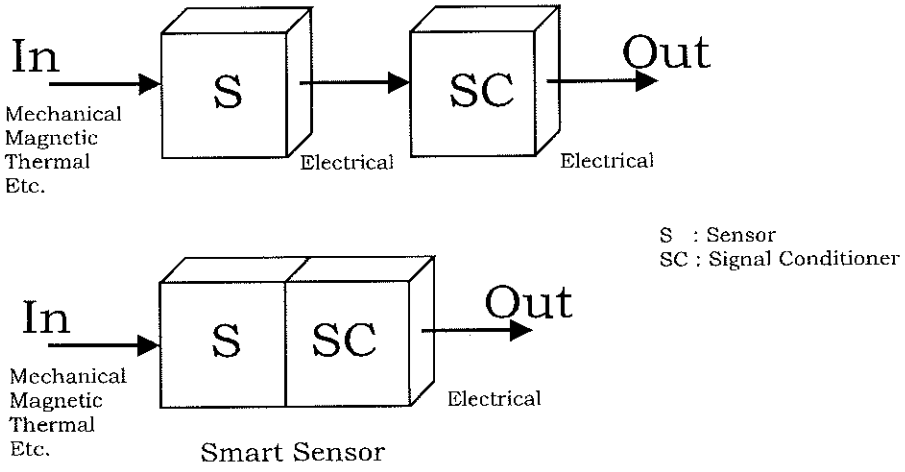

Figure 1.3: From traditional sensor to smart sensor

1.3.3 Capacitive Sensors

During the last 10-15 years capacitive sensors have gained a lot of attention. Why are capacitive sensors so interesting? To answer that question we have to remember the desire to realize true smart sensors, that is to implement both sensors and electronics on the same chip. And we have to remember that a large part of the sensors needed today are of the mechanical type, i.e. measuring pressure, displacement etc. There are basically two effects that have been used to convey signals in the mechanical domain into electric signals. These are piezoresistiv and capacitive sensors. Both can fairly easy be implemented in silicon. Until now the piezoresitive sensor has had a lot of success. So why even bother with capacitive sensors ?

The reason is that capacitive sensors has a number of distinct advantages when compared to their piezoresistive counterpart : high sensitivity, low power consumption, better temperature performance, less sensitive to drift, etc. These are the reasons why capacitive sensors are so interesting. In [4] an overview of capacitive sensors is presented.

The basic idea of capacitive sensors is to measure a displacement by a change in capacitive value. An example of an capacitive displacement sensor (a microphone) is shown in Fig. 1.4

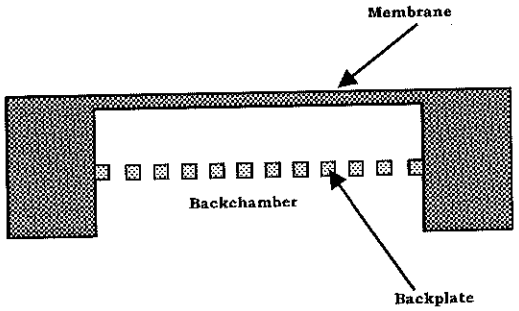

Figure 1.4: A capacitive microphone (not to scale)

The function of the microphone is as follows : An incoming sound pressure will bend the membrane towards the backplate. This will increase the capacitance between the membrane and the backplate. This capacitance change can then be detected.

1.4 CMOS Past Present and Future

In the beginning of the era of integrated circuit design the technology for analog circuit design was bipolar technologies. With the evolution of digital CMOS processes, analog CMOS processes soon became available . The first analog MOS process was very poor. Only NMOS transistors were available and they were not really suited for analog design. This is the reason why bipolar design was dominating in standard analog designs for many years. And to some extent still is. CMOS has still a reputation as a technology not very well suited for analog design.

1.4.1 CMOS, Microelectronic Technology of the Future ?

In recent years the CMOS technologies have undergone enormous improvements. From being a convenient technology it has now the potential to become state of the art for analog designers. In the late 80's it was BiCMOS that was predicted to take this role. But this has never happened. The reasons are that most of the features gained in BiCMOS can also be obtained in modern CMOS proceses. The main argument for using BiCMOS is the bandwidth that can be obtained by utilizing bipolar design. All other features can be obtained by CMOS and for low power design CMOS is more suited than bipolar. In low power design weak inversion operation is of special interest, as this special region of operation of the CMOS transistor gives the best performance for a given power consumption. Transconductance is maximal, GBW is maximal and noise input voltage is minimum. So the current limit of weak inversion operation is of special interest. Furthermore the maximal GBW in weak inversion is of special interest. In appendix E the dependencies of the channel length has been calculated. These are summarized in table 1.2. L is the minimum gate length and Xdrain is the drain area parallel to current flow (see appendix E).

Table 1.2: Analog features dependencies of minimal channel length.

Features	*Dependencies*
Weak inversion current limit	$\sim \frac{1}{L^2}$
Max. GBW in Weak inversion	$\sim \frac{1}{L \cdot Xdrain}$
Charge injection	L^2

A comment on these. Weak inversion operation is today ($0.5\mu m$ technology) with a transistor input-capacitance of 1pF all up to $30\mu A$. This with a GBW of 10-20 MHz and going to sub 0.1μ will give weak inversion operation at $750\mu A$ with a max. GBW in the range of hundred MHz. As seen from the table charge injection will not be a problem in future technologies. Besides from these the most advanced CMOS technologies of today and the future will have low 1/f noise. In chapter six a low noise amplifier with noise corner of 40Hz is described.

In strong inversion the maximal f_T will be comparable to that of bipolar technology. In [5] a short channel CMOS technology exhibits $f_T's$ of 48GHz, at a remarkable low supply voltage of 0.5V. As the threshold voltages of CMOS will go down to 0.5V-0.6V in the future then CMOS will also be very well suited for low voltage design. This comes from the fact that the minimal power consumption of digital circuitry is at a power supply of 1V-1.2V and with a threshold of both P and N channel devices of 0.5V-0.6V (see [6]). So analog circuitry operating on supply voltages from 1V-1.3V (a single battery cell) will be of enormous importance.

So it looks as if CMOS will be able to fully match bipolar technology.

1.5 Conclusion

It is obvious that digital technology will continue to take over signal processing areas from analog signal processing. There will however be some areas where digital signal processing will not be able to compete with analog signal processing. These are :

Low precision signal processing

High frequency signal processing

Sensors and interface circuitry

In order to stay in business the analog designer will have to move his interest to these areas. At the moment sensors and interface circuitry is the most interesting field. Modern CMOS microelectronics technology has become so important that it will be the technology of the next decade(s). Furthermore analog circuit designers will have to design with low power (μ watts) and under low supply voltage (1V-1.2V) constraint.

Chapter 2

Low Power Analog Signal Processing

In this chapter we will treat low power consumption from a theoretical point of view. We will show how the best signal to noise ratio is achieved with the smallest power consumption possible. Besides from section 2.1.1 this has not been presented before.

2.1 Minimal Power for Analog Signal Processing

We will now try to calculate the minimal power for analog signal processing. The following is originally developed by Vittoz [2]

2.1.1 Absolute Minimal Power Consumption for Analog Signal Processing

The simplest analog signal processing circuitry that can be imagined is a single class B amplifier with a purely capacitive load of C_L. The amplifier is operated on a power supply of $V_B = V_{DD} - V_{SS}$.

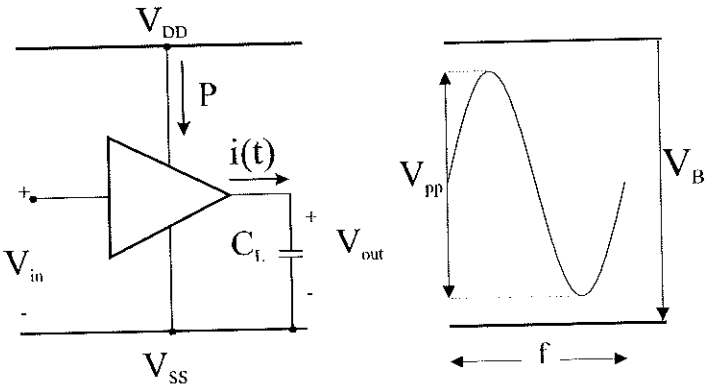

Figure 2.1: minimal analog signal processing circuitry

The power needed to process a sine wave with a peak to peak voltage of V_{pp} and

frequency f is :

$$P = V_B \cdot i_{mean} = V_B \cdot f \cdot V_{pp} \cdot C_L = \frac{V_B}{V_{pp}} \cdot f \cdot V_{pp}^2 \cdot C_L \tag{2.1}$$

As the total integrated noise power at the output is $\frac{kT}{C_L}$ (see appendix C) and the signal power is $V_{pp}^2/8$ then the signal to noise ratio is :

$$S/N = \frac{V_{pp}^2/8}{kT/C_L} \tag{2.2}$$

From equation 2.1 and 2.2 one can see that the minimal power needed for a given S/N is :

$$P_{min} = 8kT \cdot f \cdot S/N \tag{2.3}$$

And this is accomplished for $V_{pp} = V_B$. As one notices, it has a linear dependence of S/N. This is pictured in Fig. 2.2 together with actual implementations of A/D converters. This figure has been taken from [7].

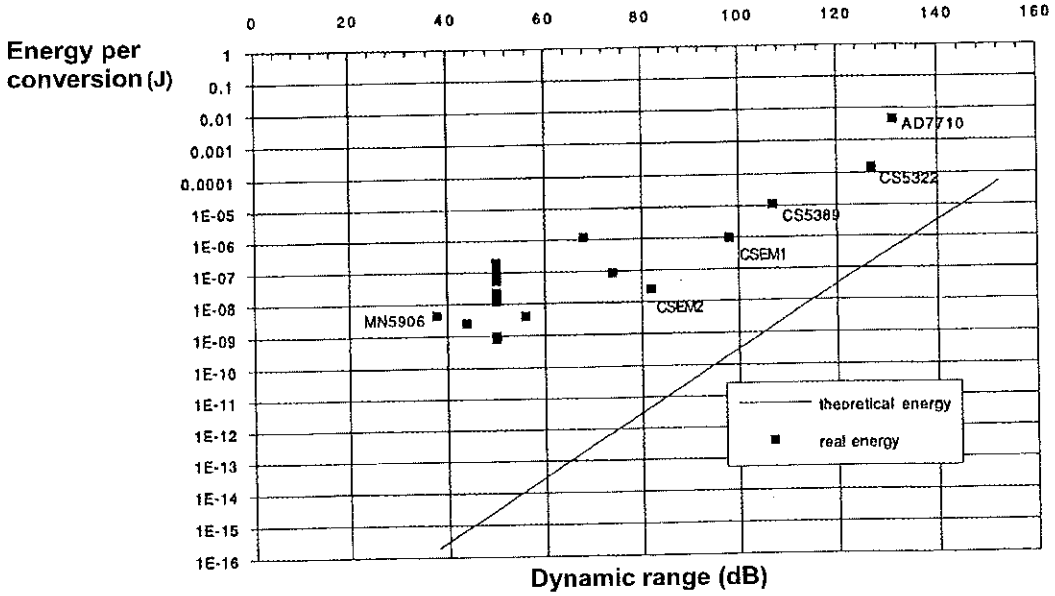

Figure 2.2: minimal power for analog signal processing and power vs. dynamic range for several A/D converters

Fig. 2.2 shows that practical implementations of analog signal processing circuitry uses much more power than predicted by equation 2.3. Why is there this diversion ? There are several reasons :

Non Rail to Rail output swing
Extra noise sources
Not purely class B operation
Quiescent current consumption

Perhaps the last one is the most interesting. In the analysis leading to equation 2.3 the bandwidth of the circuitry was not taken into consideration. i.e. it was assumed that an amplifier with a quiescent current of zero could have a bandwidth sufficiently to process a sine wave with a frequency of f. In real semiconductor circuits there is a directly connection between the quiescent current and the bandwidth of the circuitry. From Fig. 2.3 we see that the bandwidth is :

$$BW = \frac{g_m}{2\pi C_L} \leq \frac{I_{BIAS}}{2\pi n \cdot V_t \cdot C_L} \tag{2.4}$$

The right hand side comes from the fact that g_m of a semiconductor never will be larger than $\frac{I_{BIAS}}{n \cdot V_t}$. Where I_{BIAS} is the quiescent current in the semiconductor. And $n \cdot V_t$ is a slope factor times the 26mV. This could be weak-inversion operation of a MOS transistor or it could be a bipolar transistor.
So bias current is directly proportional to the bandwidth.

2.1.2 Minimal Power Consumption for Analog Signal Processing Circuit with Limited Bandwidth

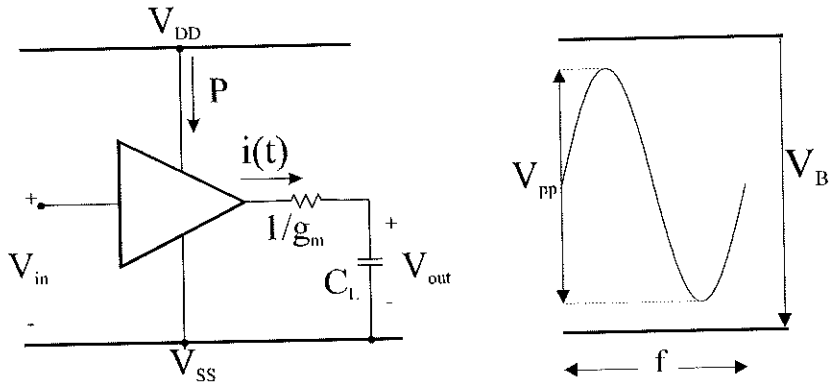

Figure 2.3: minimal analog signal processing circuit with frequency band width limit

We will now again analyze the power consumption of an analog signal processing circuitry but now with the difference that the amplifier has an finite output resistance $1/g_m$. This will in conjunction with C_L set the band limit of the circuitry.

2.1.3 Supply Voltage for Analog Signal Processing

In the analysis we have assumed that the amplifier is 100 % power efficient, meaning that it consumes no static power. This is of course an approximation. One would then like to know when is it valid ? As the S/N is maximum for V_p equal to V_B we see from equation 2.2 that increasing the power supply V_B by a factor of two actually allows us to decrease the load capacitance with a factor of four, still maintaining the same S/N. The static power consumption is equal to :

$$P_{static} = V_B \cdot I_{BIAS} \tag{2.5}$$

Keeping the same bandwidth of the circuit one sees from equation 2.4 ,that the static current consumption I_{BIAS} can be reduced to one quarter. So if we double the supply voltage V_B we can cut the current consumption to one quarter. This reduces the static power consumption to one half. The dynamic power consumption on the other hand is left unaffected. So the conclusion is that for analog signal processing a very large power supply voltage is desirable for low power design. This is of course under the assumption that now slewing occurs.

The next question is then, does the dynamic power dissipation dominate or is it the static power dissipation ?

2.2 Dynamic Power Dissipation vs. Static Power Dissipation

In the following example the power consumption of the popular switched capacitor "autozero circuit" is evaluated. This example is interesting because it is the switched analog signal processing circuitry where dynamic power dissipation maximal. This is due to the charging and discharging of the capacitor.

Example 2.2.1
The major difference between this analysis and the one of Vittoz is that the band-width limit of the amplifier is taken into consideration. At it is seen in the following example, the bandwidth is determined by the quiescent current.

In the analysis we will use the model of a switched capacitor amplifier shown in Fig. 2.4 .

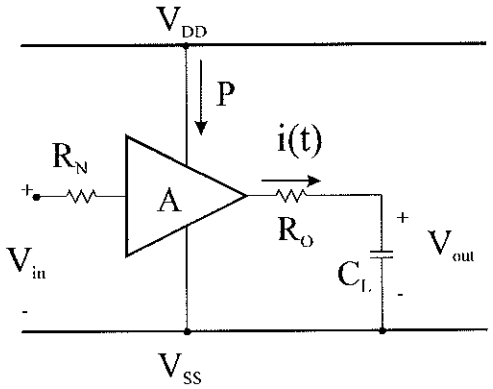

Figure 2.4: minimal switched capacitor autozero circuitry

The model of the switched capacitor amplifier consists of an equivalent noise resistor R_N, an ideal amplifier with gain A , a output resistance R_o and a load capacitance C_L. As the amplifier is ideal it uses no static power, it has in itself no output resistance and the only band-width limiting factor is the low pass filter formed by the output resistance R_o and the load capacitance C_L. The amplifier is connected to power supplies V_{DD} and V_{SS}. The dynamic power is delivered through V_{DD}.

We will now define :

$$R_o = \frac{1}{g_m} \cdot A \tag{2.6}$$

$$R_N = \gamma \cdot \frac{1}{g_m} \tag{2.7}$$

Equations 2.6 2.7 states that the output resistance and the noise resistance always will be proportional the $fraq1g_m$ *of a semiconductor. And thus dependent of the quiescent current in the semiconductor. Neither switches, nor switching scheme has been added to this model, as their effect can be modeled by the correction factor* γ *to the noise resistance* R_N*. This correction factor will also be dependent of the actual amplifier topology.*

The first step is to calculate the total noise power at the output (see [8], pp. 83) :

$$V_{No}^2 = \frac{\gamma \cdot A \cdot kT}{C_L} \tag{2.8}$$

In switched capacitor circuits the total noise power is important because the white noise will be sub-merged and all of the available noise power will be situated from $-f_S/2$ *to* $+f_S/2$*. Where* f_s *is the sampling frequency (see appendix C)*

As the signal power is $V_{pp}^2/8$ *then the S/N is :*

$$S/N = \frac{V_{pp}^2/8}{\gamma \cdot A \cdot kT/C_L} \cdot OSR \tag{2.9}$$

We are only interested in the noise power from -f/2 to +f/2 so the S/N has been multiplied by the over-sampling factor $OSR = \frac{f_S}{f}$*.*

Now we will calculate the dynamic power consumption. The autozero circuit samples the signal each T_S *holds the value in* $T_S/2$ *and then returns to zero for* $T_S/2$*. The output wave-form can be seen in Fig. 2.5. This figure also shows the current delivered from the power-supply* V_{DD}*.*

Because the charge stored on the capacitance is dumped before a new value is sampled then the capacitor C_L *can be interpreted as a resistor* R_{eq} *of value :*

$$R_{eq} = \frac{T_S}{C_L} \tag{2.10}$$

This is of course an approximation, which only holds for $1/f \gg T_s$*. The power dissipated in this fictive resistance can only be delivered through the power-supply* V_{DD}*. From this the mean current delivered from the power supply* V_{DD} *can be calculated to :*

$$i_{mean} = \frac{V_{pp}}{R_{eq}\sqrt{8}} = \frac{f_S \cdot C_L \cdot V_{pp}}{\sqrt{8}} \tag{2.11}$$

From this the total minimum dynamic power consumption can be calculated :

$$P_{dyn} = i_{mean} \cdot V_B = \frac{1}{\sqrt{8}} \cdot S/N \cdot \gamma \cdot A \cdot kT \cdot f \tag{2.12}$$

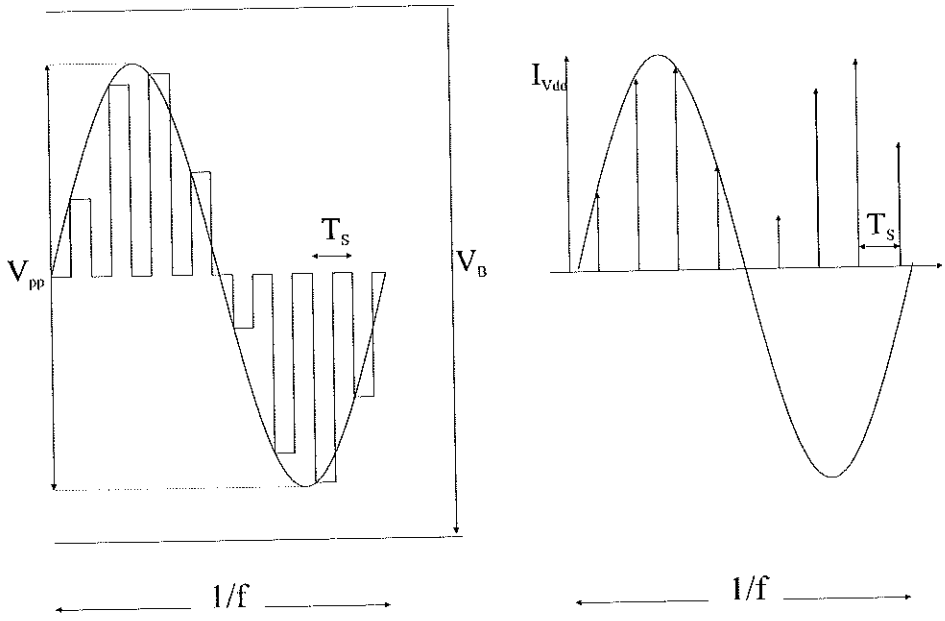

Figure 2.5: Wave-form of output signal and current delivered trough V_{DD}.

The static current consumption can now be calculated from settling requirements. The settling is of the exponential type with time constant determined by R_o and C_L. The settling time t_s is :

$$t_s = \frac{1}{g_m} \cdot A \cdot C_L \cdot ln\frac{1}{\varepsilon} \tag{2.13}$$

Where ε is the relative settling error.

We will now assume that the maximum g_m for a given current can be achieved. This implies that $g_m = \frac{I_{bias}}{n \cdot V_t}$. The amplifier must settle within $T_S/2$. This gives us :

$$I_{bias} = \frac{n \cdot V_t}{T_s/2} \cdot A \cdot C_L \cdot ln\frac{1}{\varepsilon} \tag{2.14}$$

From this the static power consumption can be calculated to :

$$P_{stat} = V_B^2 \cdot C_L \cdot \frac{nV_t}{V_B} \cdot \frac{2}{T_S} \cdot A \cdot ln\frac{1}{\varepsilon} = P_{dyn} \cdot 4 \cdot \sqrt{2} \cdot A \cdot \frac{nV_t}{V_B} \cdot ln\frac{1}{\varepsilon} \tag{2.15}$$

If we then assume that $A = 1$, $nV_t = 65mV$ and $\varepsilon = 0.001$ then P_{stat} equals P_{dyn} when $V_B = 2.5$ V. So if $V_B < 2.5V$ then the static power dominates.

■

So what conclusion can we draw from the above example ? First of all, static power dissipation is reduced as the maximal signal swing increases. I.e. as the supply voltage increases. This is though under the assumption that the capacitance's can be scaled. The above example shows that even for the largest possible dynamic power consumption the static power consumption will normally dominate. One can think of examples where the dynamic power dissipation will dominate over the static power dissipation, but in nearly all practically designs the static power consumption will be

the main power consumer. So the conclusion is then that low total power dissipation is achieved when the static power dissipation is minimized and the supply voltage should be chosen as large as possible.

2.3 The Current Efficiency of Opamps

The interesting parameter for analog signal processing is the current needed to obtain a given signal to noise ratio. This we define as the current efficiency of a opamp. Design of current efficient opamps can be approached in two levels. These are topology and transistor level approach. In the topology level one considers the current efficiency of single stage amplifiers vs. multiple stage amplifiers (i.e. two stage amplifiers). The transistor level approach deals with different ways of implementing gain stages. In the following first the topology level approach will be pursued and then the transistor level. In [9] a comparison of several low power amplifiers using a dedicated software tool was presented. In this we will use a theoretical comparison. The results match the ones of [9].

2.3.1 Amplifier Topology

For many years the traditional ways of realizing opamps has been the traditional two stage or even three stage amplifiers. A g_m stage followed by a low impedance buffering stage has been the de facto standard for discrete opamps for decades. This tradition has been adopted by asic designers without questioning. The only acceptable reasoning for using low impedance output buffering stages is the ability to handle low impedance's without loosing gain. Keeping the signals on chip omits the need of handling low impedance levels.

In the following we will show that from a power consumption view the buffering stage is also unwanted.

We will find the relationship between power and signal to noise ratio for a single stage OTA, a two stage amplifier and a two stage OTA. In the analysis we will use a general model of an amplifier stage Fig. 2.6. In Fig. 2.6 β is the real feedback coefficient, R_{out} is the output impedance of the amplifier, C_L is the load capacitance, R_N is the equivalent noise resistance of the amplifier and A is the open loop gain of the amplifier.

The open loop gain of the amplifier can be expressed as ([8] pp. 82) :

$$A(s) = \frac{1}{s\tau_u(1 + s\tau_p)} \tag{2.16}$$

Where τ_u is the time constant corresponding to the frequency where A equals one. And τ_p is the time constant corresponding to the parasitic pole. This can be seen in Fig. 2.6 We will now use the amplifiers step response to evaluate its performance :

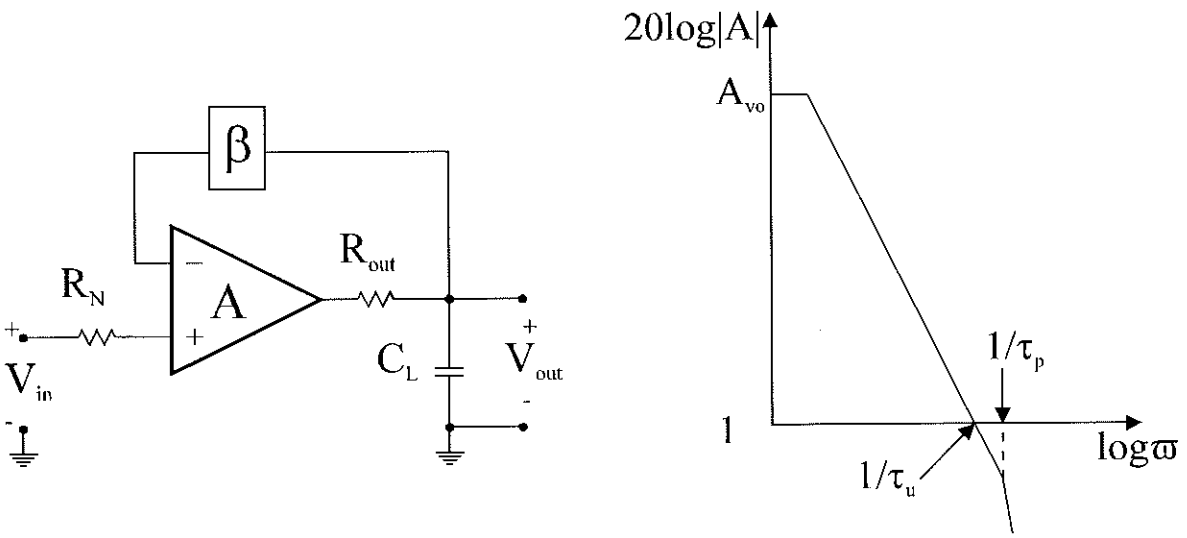

Figure 2.6: Amplifier and its gain as a function of frequency

In Fig. 2.7 a step and the amplifiers response to the step is shown. As the amplifier has a limited bandwidth it will need some time to approach its final value. The settling time $T_s$is defined as the time to settle within an error band ε relative to the final value.

Given the open-loop gain of equation 2.16, the amplifier topology of Fig. 2.6 and assuming linear settling then the settling time can be approximated by (se appendix A) :

$$T_s = (2\tau_p + \frac{\tau_u}{\beta})ln\frac{1}{\varepsilon} \tag{2.17}$$

The second parameter describing the amplifiers performance is the total, integrated white noise at the output. The integrated white noise at the output can be expressed as :

$$V_{no}^2 = \frac{kT \cdot R_N}{\beta\tau_u} \tag{2.18}$$

This does not depend on the parasitic time constant τ_p (see [8], pp. 82.).

Single Stage OTA

For a single stage OTA it is reasonable to assume that the open loop gain has only one pole. This is the pole formed by the output resistance and the load capacitance. The gain of the amplifier can then be written as $G_m \cdot R_{out}$. From this we see that :

$$\tau_u = G_m \cdot C_L \tag{2.19}$$

The first part of the analysis of the signal to noise ratio vs. power relationship, is to calculate the necessary current for a given settling time T_S. As there is only one pole then the current needed is :

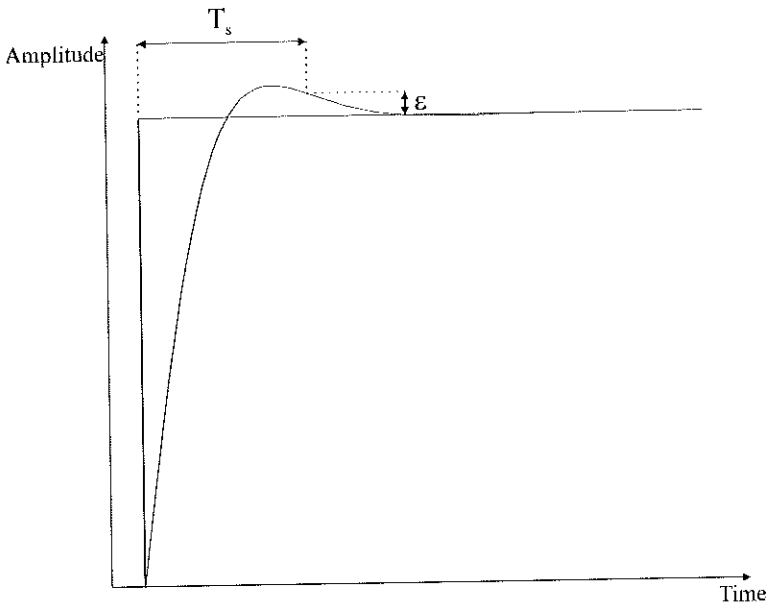

Figure 2.7: Step response, normalized to the final value

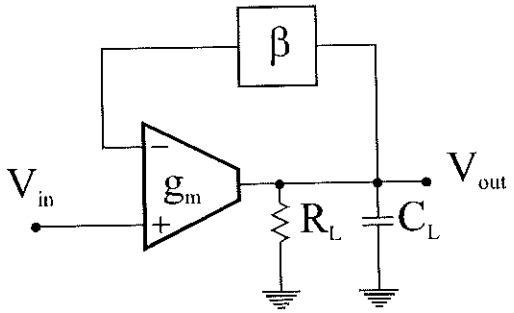

Figure 2.8: Single stage OTA

$$I_{bias} = \frac{nV_t C_L}{\beta \cdot T_s} ln \frac{1}{\varepsilon} \tag{2.20}$$

Here g_m is considered to be $\frac{nV_t}{I_{bias}}$, which is the maximal g_m for any type of semiconductor.

The next step is to calculate the total white noise power at the output. this can be calculated to (see [8], pp. 83.):

$$V_{no}^2 = \frac{kT \cdot \gamma}{\beta \cdot C_L} \tag{2.21}$$

Where $\gamma = R_N \cdot g_m$.

Two Stage Amplifier

A two stage amplifier will always have at least two poles. These normally originate from the first and second stage. In this analysis we will use the well known configuration with a g_m input stage followed by a buffer stage.

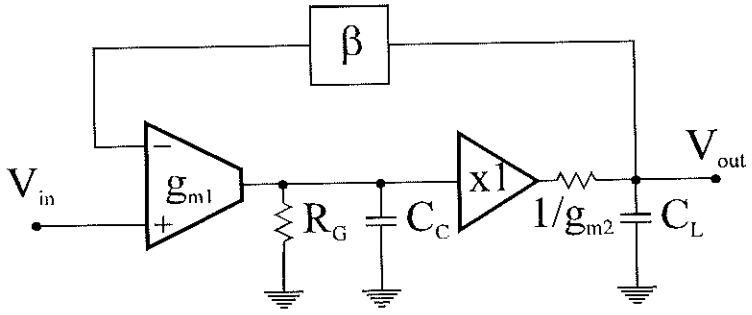

Figure 2.9: Two stage amplifier

The first pole, with a time constant $\frac{\tau_u}{\beta}$ is normally formed by the G_{m1} of the input stage and a compensation capacitor C_c . The second pole, with a time constant τ_p is normally formed by the second stage output resistance $R_o = 1/G_{m2}$and the capacitive load C_{load} on the output. So the two time constants can be calculated as :

$$\tau_u = \frac{C_C}{Gm1} \; and \; \tau_p = \frac{C_L}{G_{m2}} \tag{2.22}$$

The settling time can thus be approximated by :

$$T_s = (2\frac{C_L}{G_{m2}} + \frac{C_C}{\beta \cdot G_{m1}}) \cdot ln\frac{1}{\varepsilon} \tag{2.23}$$

Or if we assume that the $g'_m s$ are $\frac{nV_t}{I_bias}$, which is the maximal g_m for any type of semiconductor then we get :

$$T_s = (2 \cdot C_L \cdot \frac{nV_t}{I_{bias2}} + C_L \cdot \frac{nV_t}{\beta \cdot I_{bias1}}) \cdot ln\frac{1}{\varepsilon} \tag{2.24}$$

Where I_{bias1} and I_{bias2} are the bias currents in the two semiconductors forming the two poles. The total power consumption is then proportional to the sum of I_{bias1} and I_{bias2}. It can be calculated that , for a given settling time the minimum total bias current $I_{bias1} + I_{bias2}$ is :

$$I_{biastot} = \frac{nV_t}{T_s} \cdot (2C_L + \frac{C_C}{\beta} + \sqrt{8 \cdot \frac{C_C \cdot C_L}{\beta}}) \cdot ln\frac{1}{\varepsilon} \tag{2.25}$$

And as the total noise on the output only is dependent on τ_u then :

$$V_{no}^2 = \frac{kT \cdot R_N}{\beta \cdot \tau_u} = \frac{kT \cdot \gamma}{\beta \cdot C_C} \tag{2.26}$$

Two Stage OTA

Now we will calculate the bias current needed to settle and the total integrated white noise of the output of the amplifier. The first step is again to find τ_u and τ_p. These can be found to :

$$\tau_u = \frac{C_C}{Gm1} \; and \; \tau_p = \frac{C_L}{G_{m2}} \tag{2.27}$$

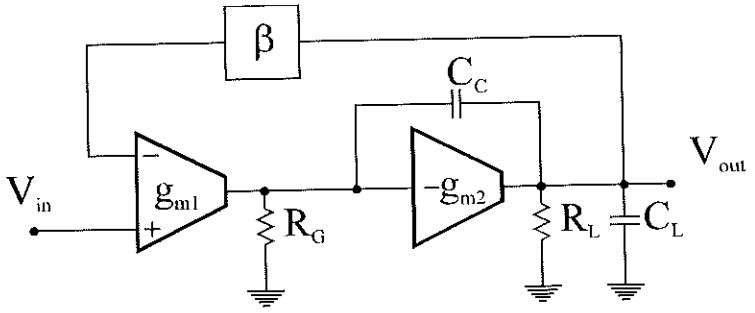

Figure 2.10: Two stage OTA

So it is seen that the two stage OTA actually has exactly the same performance as the two stage amplifier, se equation 2.22. This means that the equations 2.23 to 2.26 can be used for the two stage OTA also.

We have in this analysis not taken the feed-forward path through C_C into consideration . This will further increase the settling time of the two stage OTA compared to the two stage amplifier. Furthermore we have assume that the two time constants τ_u and τ_p are widely spread.

2.3.2 Comparison of Single Stage vs. Two Stage Amplifier and Two Stage OTA

We will now try to compare single stage OTA vs. two stage amplifier and two stage OTA. We will assume that the capacitive load is equal in the three cases. The first step is to compare the integrated white noise on the output. The equations 2.21 2.26 show us that C_C should equal C_L to obtain the same output noise as for the one stage amplifier. This will reduce equation 2.3.1 to :

$$I_{twostage} = \frac{nV_t \cdot C_L}{T_s} \cdot (2 + \frac{1}{\beta} + \sqrt{\frac{8}{\beta}}) \cdot ln\frac{1}{\varepsilon} \tag{2.28}$$

There are two interesting situations. These are the $\beta = 1$ and $\beta \gg 1$. In these two cases equation 2.3.2 reduces to 2 and 6 times equation 2.20. So we can conclude that a two stage amplifier/OTA uses between 2 and 6 times the static power of a single stage OTA. This is a very important point.

Table 2.1: Parameters of single stage, two stage amplifiers and two stage OTA's

	$\beta \simeq 1$	$\beta \simeq 1$	$\beta \gg 1$	$\beta \gg 1$
Amplifier type	$I_{quiescent}$	V^2_{noise}	$I_{quiescent}$	V^2_{noise}
Single stage OTA	$\frac{n \cdot V_t}{T_s} \cdot C_L \cdot ln\frac{1}{\varepsilon}$	$\frac{k \cdot T \cdot \gamma}{C_L}$	$\frac{n \cdot V_t}{T_s} \cdot \frac{C_L}{\beta} \cdot ln\frac{1}{\varepsilon}$	$\beta \cdot \frac{k \cdot T \cdot \gamma}{C_L}$
Two stage Amplifier	$6 \cdot \frac{n \cdot V_t}{T_s} \cdot C_L \cdot ln\frac{1}{\varepsilon}$	$\frac{k \cdot T \cdot \gamma}{C_L}$	$2 \cdot \frac{n \cdot V_t}{T_s} \cdot \frac{C_L}{\beta} \cdot ln\frac{1}{\varepsilon}$	$\beta \cdot \frac{k \cdot T \cdot \gamma}{C_L}$
Two stage OTA	$6 \cdot \frac{n \cdot V_t}{T_s} \cdot C_L \cdot ln\frac{1}{\varepsilon}$	$\frac{k \cdot T \cdot \gamma}{C_L}$	$2 \cdot \frac{n \cdot V_t}{T_s} \cdot \frac{C_L}{\beta} \cdot ln\frac{1}{\varepsilon}$	$\beta \cdot \frac{k \cdot T \cdot \gamma}{C_L}$

2.3.3 Transistor Level Approach

In this subsection the transistor level approach of low power design will be pursued. In this four basic CMOS amplifiers will be analyzed comparing signal to noise ratio's and power consumption. In Fig. 2.11 the four basic amplifiers is depicted. These are : single transistor gain stage, differential stage, inverter gain stage and pseudo differential gain stage with inverters. A comparison can also be found in [8], pp. 75. But there a slightly different approach is used and in this analysis a extra type of amplifier has been added (the pseudo differential inverter). All transistors are operated in weak inversion for maximal g_m and minimum noise.

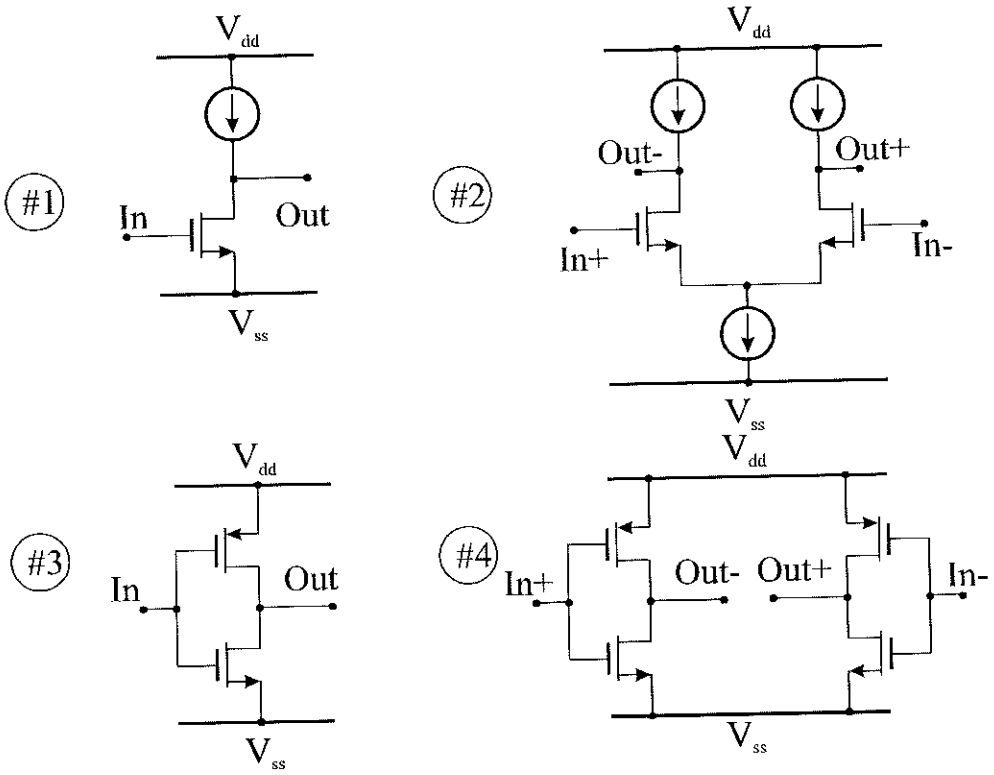

Figure 2.11: Four basic CMOS amplifiers

Table 2.2: Parameters of 4 basic CMOS amplifiers

Amplifier	$I_{quiescent}$	R_N	g_m	V^2_{outmax}	*FOM*
#1 *single transistor gain stage*	1	1	1	1	1
#2 *Differential stage*	2	2	1	4	1
#3 *Inverter*	1	1/2	2	1	4
#4 *Pseudo differential inverter*	2	1	2	4	4

In table 2.2 the important parameters of the amplifiers are resumed. All parameters is compared to the ones of the single transistor gain stage. The important parameters are total quiescent current $I_{quiescent}$, noise resistance R_N, trans-conductance g_m, max-

imum output voltage swing V_{outmax} and a Figure Of Merit (FOM). We will now go through these one by one.

Quiescent Current $I_{quiescent}$

The quiescent currents are all normalized to the quiescent current of a single transistor amplifier. At it is seen stacking of transistors (inverter) does not increase the quiescent current. While paralleling of transistors (differential stage) doubles the quiescent current. And therefore doubles the static power consumption.

Noise Resistance R_N

The noise resistance is a resistor that is equally noisy as the amplifier itself. It is calculated by referring all of the white noise of the amplifier to the input and the calculating the resistor value that would have the same noise voltage spectral density. The noise resistance is a measure of how noisy the amplifier is. The larger value, the noisier it is. All values have been normalized to that of a single transistor. For the single transistor amplifier the noise resistance is (in weak inversion [10]):

$$R_N = \frac{n}{2} \cdot \frac{1}{g_m} \tag{2.29}$$

One notices that the differential stages only has a R_N twice as large as the single ended versions. This means that they have two times more noise power.

Trans-conductance g_m

Maximal trans-conductance g_m for a given current is important, because the trans-conductance sets the settling time of a amplifier.

Maximum Output Voltage Swing V_{outmax}

Using differential configurations of course improves the maximal output swing and thus the maximal signal to noise ratio. Again there is normalized to the single transistor amplifier. One must remember that for every doubling of the signal swing the signal power increases by a factor of four. So using differential stages is very effective in terms of increasing the signal to noise ratio. As the noise power is only increased by a factor of two then we actually gain a factor of two compared to the single stage amplifiers.

Figure Of Merit (FOM)

The figure of merit is a measure of the S/N to power consumption relationship. It takes quiescent current $I_{quiescent}$, noise resistance R_N, trans-conductance g_m and maximum signal swing V_{outmax} into consideration. The signal to noise ratio will be proportional to $1/R_N$ and V_{outmax}^2 And the power consumption will be proportional to $I_{quiescent}$ and $1/g_m$. This means that the figure of merit can be calculated by :

$$FOM = \frac{1/R_N \cdot V_{outmax}^2}{I_{quiescent} \cdot 1/g_m} \sim \frac{SNR}{Power\ consumption} \tag{2.30}$$

Where the values are the normalized values. The larger the FOM the better the S/N vs. power performance. It is seen that a simple inverter and the pseudo differential inverter are by far the most power efficient amplifier types. i.e. it is these amplifier types have the lowest power consumption for a given S/N.

2.4 Low Power Signal Processing: SC or SI ?

Analog designers have two interesting choices when designing analog signal processing circuitry today. Switched capacitor technique (SC) is the well known design technique which has proven its capability in the past 15-20 years. The newcomer is the so called switched current technique (SI). Which one is preferable when designing low power analog signal processing circuitry ? We will compare the basic limitations by analyzing three key factors that are crucial for low power analog signal processing.

2.4.1 S/N Ratio

In both SC and SI the S/N ratio is limited by the capacitor where the signal is stored onto. And by the signal swing on this capacitor. This signal swing is in SC only limited by the power supply. In SI it is on the contrary limited by the effective gate source voltage ($V_{gs} - V_T$). At low voltages thus gives an advantage for SC. This is shown in [11]

2.4.2 Speed for Given Power Consumption

At low currents SC has an advantage over SI because the settling in SI is signal dependent, which is not the case for SC. This means that the bias currents for a given settling time is larger for SI than SC.

2.4.3 Power Consumption

For SI the speed/power ratio and S/N are best with transistors operated in strong inversion (large currents). For SC the contrary is true. It is best operated in weak inversion. This is a small advantage to SC.

2.5 Conclusion

If we summarize, then the main conclusions of this chapter are that low power analog signal processing is not equal to low voltage signal processing. In fact low power analog signal processing benefits from a high voltage power supply. This comes from the fact that the static power consumption needed to obtain a given bandwidth or maximum settling time normally dominates. If capacitance's can be scaled then increasing the supply voltage allows us to decrease the static power consumption.

On the topology level it was seen that using very simple topologies is much more power efficient than using multistage amplifiers. In fact in the worst situation a two stage amplifier/OTA uses 6 times as much static power as a single stage OTA.

On the transistor level four different transistor OTA's were analyzed and their S/N vs. power consumption was found. It was shown that a simple inverter and a pseudo differential inverter amplifier is approximately 4 times as efficient as a differential stage and a single transistor stage. In this the slewrate limitations of the differential stage was not taken into consideration. As the inverter (and the psuedo differential inverter) has no slewrate limitations this further benefits the inverter in the comparison.

Furthermore a brief comparison of the so called Switched Current technique and the well known switched capacitor technique is presented. It is concluded that Switched Current technique is not well suited for low power signal processing. The main reason for using switched current technique is the compatibility with digital CMOS process.

Chapter 3

Low Voltage Techniques

As we have seen in chapter two the maximal signal to noise ratio (S/N) depends directly on the maximal signal swing at the output of the signal processing circuitry. This is in the end only limited by the power supply. If the circuitry doesn't have full rail to rail signal swing at the output, then the S/N will be further limited. As we will see rail to rail input swing is not equally important.

In chapter two it was also shown that the optimal power supply voltage for low power analog signal processing is a very large power supply voltage. I.e. only limited by the maximal operating voltage of the microelectronics technology used.

There are, though situations where the circuitry has to operate on a very low power supply voltage level. As battery operated electronics become more and more important (see chapter one) then the power supply voltage will ultimately decrease to approx. 1.3v-1.5v, which is the battery voltage of a single battery. Also for digital low power electronics the power supply will decrease to approx. 1v-1.5v. The possibility of doubling / tripling the supply voltage can not always be applied. So the conclusion is that circuitry capable of operating on power supply voltages from 1v to 1.5v will be very usefull.

In this chapter we will try to develop techniques that can be used to achieve the maximal signal swing at the output for a given supply voltage. We will first discuss general design techniques of low voltage circuitry. Then we will go through circuitry design for time continuos signal processing circuitry and circuitry for switched or time discrete signal processing. Both examples from the literature and the authors own designs will be shown.

3.1 General Low Voltage Design Techniques

In this section we will discuss general techniques for low voltage signal processing. Furthermore, we will discuss which microelectronics technology to use.

3.1.1 Maximum Output Swing and Minimum Input Signal Swing

To achieve rail to rail output swing transistors have to be operated in a common source coupling. This unfortunately limits the input signal amplitude. The following example will show the point clearly.

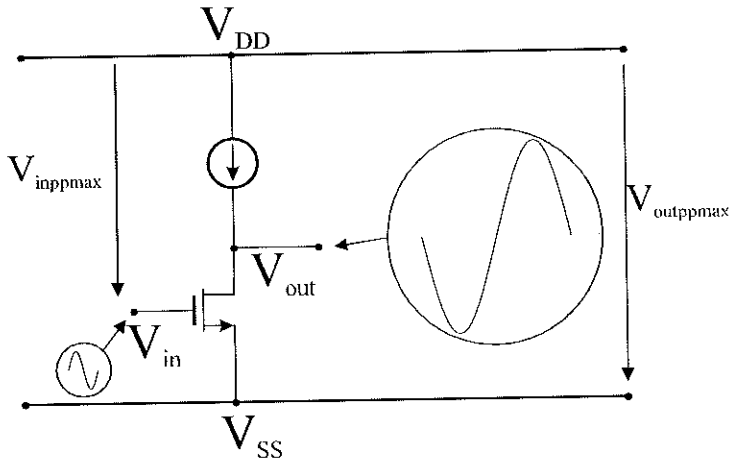

Figure 3.1: Single transistor amplifier

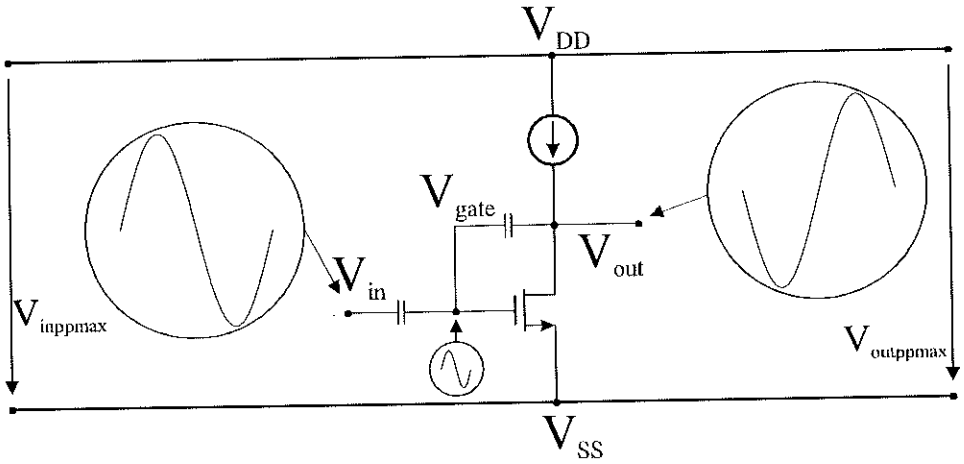

Figure 3.2: Single transistor feedback amplifier

Example 3.1.1
In Fig. 3.1 a single transistor amplifier processing a sine wave is showed. Circuitry stabilizing the working point is not showed. The voltage at the output can not exceed the power supply. At the input the maximal peak to peak voltage is $V_{DD} - V_{SS} - V_{gs}$ *and at the output* $V_{DD} - V_{SS}$*. The difference between the input and the output is the* V_{gs} *voltage of the transistor. When* $(V_{DD} - V_{SS}) \gg V_{gs}$ *then the maximal peak to peak voltage swing at the input and at the output is approximately equal. But when* $V_{DD} - V_{SS} \simeq V_{gs}$ *then the maximal voltage swing at the input is reduced significantly (approaches zero). So at low supply voltages the voltage swing at the input should be very small while the voltage swing at the output is only limited by the supply voltage.*

The amplifier of Fig. 3.1 will have no problems working at low supply voltages, if the gain of the amplifier is high. In this situation input signal amplitude will be small and the output signal amplitude will be large. But if the gain of the amplifier is low, then the amplifier will have to operate under conditions where amplitudes of both input and output signal amplitude are large. Then the amplifier will have problems operating at low supply voltages. The maximal signal amplitudes are depicted in Fig. 3.1.

A solution is depicted in Fig. 3.2. Again circuitry stabilizing the working point is not shown. Now the signal swing at the gate is reduced by negative feedback. Both the input signal swing and the output signal swing is now only limited by the power supply. This can be seen in Fig. 3.2, where the maximal signal amplitudes are depicted. ■

What we saw in the above example, was that the we should design so that the amplifier has rail to rail output swing, but not necessarily rail to rail input signal swing. Furthermore the DC levels of input and output should be set independently. Negative feedback can be used to enhance operation at low supply voltages. These few rules will allow us to design circuitry that operates at supply voltages close to the threshold voltages of the transistors.

3.1.2 Stacking and Level Shifters

When designing circuitry for low voltage operation stacking of transistors should be avoided. A circuitry where stacking of transistors occurs is showed in Fig. 3.3

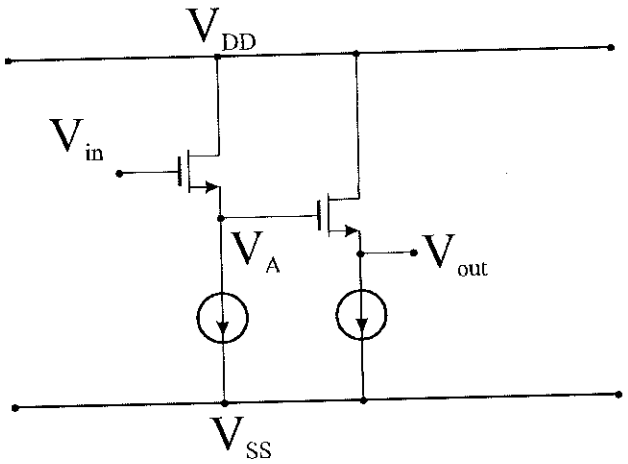

Figure 3.3: Stacking of transistors

Here it can be seen that the bias voltage level will drop from V_{in} to V_A and from V_A to V_{out}. This limits the supply voltage at which the circuitry can operate. This can be avoided by shifting between PMOS and NMOS transistors instead of using only NMOS.

Another technique is to use level shifters. The basic idea about level shifting is to alter the DC level. The best example of a level shifter is the folded cascode.

Also switched level shifting can be applied, the most commonly known is correlated double sampling (see appendix C). This is depicted in Fig. 3.5. In this the input voltage (V_{offset}) is separated from the input by a correlated double sampling scheme.

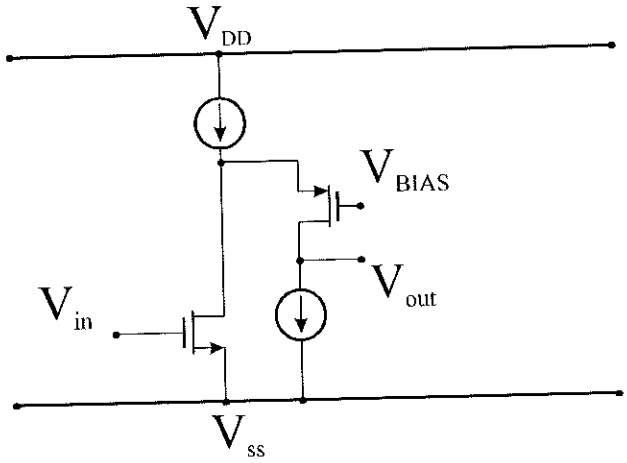

Figure 3.4: Casode used as a DC level shifter

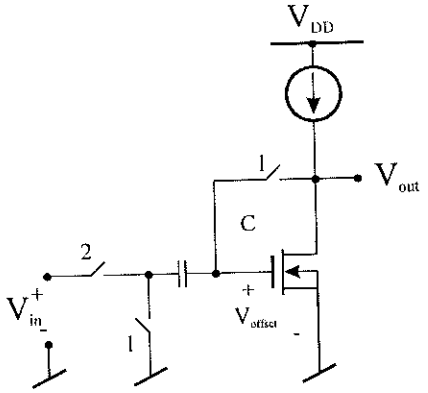

Figure 3.5: Correlated double sampling used as level shifter

3.1.3 Low Voltage Technology, CMOS or Bipolar ?

When designing low voltage amplifiers the question of which technology to use, arises ? In this subsection we will compare bipolar and CMOS technology concerning low voltage operation. In table 3.1, the main low voltage features of CMOS and Bipolar technology is listed. Bipolar has by number the most advantageous features. But does this mean that bipolar is best suited for low voltage design ?

CMOS vs. Bipolar

Table 3.1: Low voltage features of CMOS and Bipolar technology

	CMOS (strong inversion)	*Bipolar*
Maximal current drive	+	++
Control voltage swing	+	++
Low voltage f_T	+	++
Input resistance	++	-

Most of the advantages that bipolar technology possesses arise from the fact that the voltage current characteristic of a bipolar transistor is exponential. This gives a very large output current for a very little control voltage on the input. But the question is, isn't the current drive capability of CMOS large enough ? We will now use an example of a typical $0.5\mu m$ technology to examine this :

Example 3.1.2
A PMOS transistor with $V_T = 0.6V$, $K_P = 44\mu A/V^2$ and $W/L = 1000$ can at a power supply voltage of 1.5V deliver an output current of :

$$I_D = \frac{K_P}{2} \cdot \frac{W}{L} \cdot (V_{DD} - V_T)^2 = 17.7mA \tag{3.1}$$

And with a minimum gate length of $0.5\mu m$ this gives us a gate width of $500\mu m$, which is not a very large transistor. ■

The above example very well illustrates that unless very large currents have to be delivered, CMOS will normally be sufficient.

The exponential voltage current characteristic gives the bipolar transistor another advantage. It can be operated at low power supply voltages still at a high current, giving a high f_T. But again is the f_T of the CMOS large enough ?

Again we will use an example to calculate the maximum f_T for a PMOS transistor operated at a power supply voltage of 1.5V.

Example 3.1.3
The transistor from the example above has a maximum trans-conductance, at a power supply voltage of 1.5V, equal to :

$$G_m = \frac{K_P}{\sqrt{2}} \cdot \frac{W}{L} \cdot (V_{DD} - V_T) = 27.8mS \tag{3.2}$$

And a gate source capacitance of :

$$C_{gs} = \frac{2}{3} \cdot 3.4\frac{fF}{\mu m^2} \cdot 500\mu m \cdot 0.5\mu m = 0.6pF \tag{3.3}$$

So f_T is :

$$f_T = \frac{G_m}{2\pi \cdot C_{gs}} = 7.4GHz \tag{3.4}$$

This is overestimated though, as junction capacitance's and carrier velocity saturation have not been taken into consideration. But still the PMOS transistor will have a very large f_T. ■

The only disadvantage of bipolar technology, that makes it less suitable for low voltage operation, is that it has a very little input resistance compared to CMOS. For a transistor with current gain $\beta = 100$ and collector currents ranging from $10\mu A$ to $10mA$, the input resistance is in the range of $260 - 260k$ *Ohm's*. This makes it very difficult to achieve a high gain in a single gain stage and bipolar designs normally consists of several gain stages in series [12]. This is a major disadvantage. And when it comes to switched techniques, only CMOS can be used.

Special Designed Low Voltage Technologies

So far we have only discussed how to design low voltage circuitry in standard CMOS or Bipolar technology. But what options are there if we want to use technologies that are specially suited for low voltage operation ? Below are listed some features that are commercially available today and which are of special interest when designing for low voltages .

P-doped and n-doped poly.

Low V_T (un-implanted) CMOS transistors

Floating gates possibility

P-doped and n-doped poly can be used to making floating diodes. These are of special interest because they are needed when very high impedance resistors are needed. This gives us the possibility to realize true AC coupled circuits (see [13]). Low V_T transistors are of course interesting because the threshold voltage sets the lower limit of what power supply voltage the circuitry can operate on. Floating gates are also interesting as this circuit technique allows us to adjust the threshold voltages electronically, after the circuitry has been fabricated (see [14]).

3.2 Time Continuos Low Voltage Amplifiers

When designing analog circuitry for low voltage operation one of the major problems is how to design class AB circuits ? Class A/B operation is needed as low voltage operation normally is followed by low power operation. Also class AB operation is needed when large capacitive or small resistive loads have to be driven. We will now go through both a basic class A circuit and some more advanced class AB circuits.

3.2.1 Folded Cascode Amplifier

The simple differential stage has many advantages. One can mention good power supply rejection, good common mode rejection and reasonable linearity. In can be improved for low voltage operation. By adding folded cascodes to the basic differential structure , the input common mode voltage range is greatly improved. This circuit can be seen in Fig. 3.6. The input common mode voltage range furthermore includes ground for PMOS type differential stage. This is a useful feature, as the power supply voltage normally is unipolar.

3.2.2 Pseudo Differential Amplifier with Common Mode Feed-forward Regulation

Another way to implement a differential stage is to use a pseudo differential coupling of two transistors. This can be seen in Fig. 3.7 [15]. The only problem is then to establish common mode control. This has here been implemented as common mode

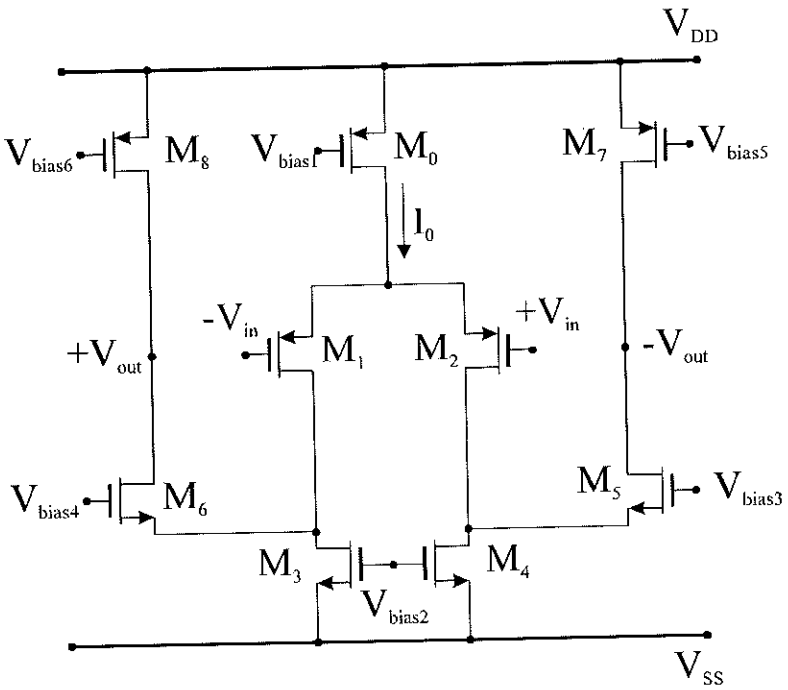

Figure 3.6: Folded cascode amplifier

feed-forward control. The common mode part of the signal is measured by M_3 and M_4. This is via the current mirror (M_5, M_5 and M_6) feed to the drains of the input transistors M_1 and M_2.

3.2.3 Low Voltage Inverter

The standard type inverter has many interesting features seen from a low power point of view (see chapter two). Low noise, low power consumption and class AB operation can be mentioned. But as an ultra low voltage amplifier it is not as useful. This comes from the fact that the transistors in the basic inverter are stacked. This restricts the operation to power supply voltages larger than $V_{TP} + V_{TN}$, which normally is in the range of 1.2V to 1.5V. Instead of connecting the two gates of the inverter directly, they can be connected via a level shifter. This enables operation at power supply voltages of the maximum of the two threshold voltages V_{TP} and V_{TN}. The level shifter is easily implemented as a AC level shifter, se Fig. 3.8. Above frequencies of $f \gg \frac{1}{2\pi \cdot RC}$ the operation of the low voltage inverter is equal to that of the standard inverter type. This was first presented by Krummenacher [16]. Unfortunately the inverter has a very poor PSSR. This can be improved by using the inverter in a pseudo differential coupling. This can be seen in figure Fig. 3.9. It consists of two low voltage inverters, see Fig. 3.8 and four resistors, implementing common mode feedback. Resistors R_{cm2} and R_{cm4} should match. And resistors R_{cm1} and R_{cm3} should match.

Differential signals will not be affected by the common mode feedback, that is, if the resistors match. Differential signal will be amplified with a large factor while common mode signal only are amplified with a factor of one. The ratio between the common mode gain and the differential mode gain is ultimately determined by matching.

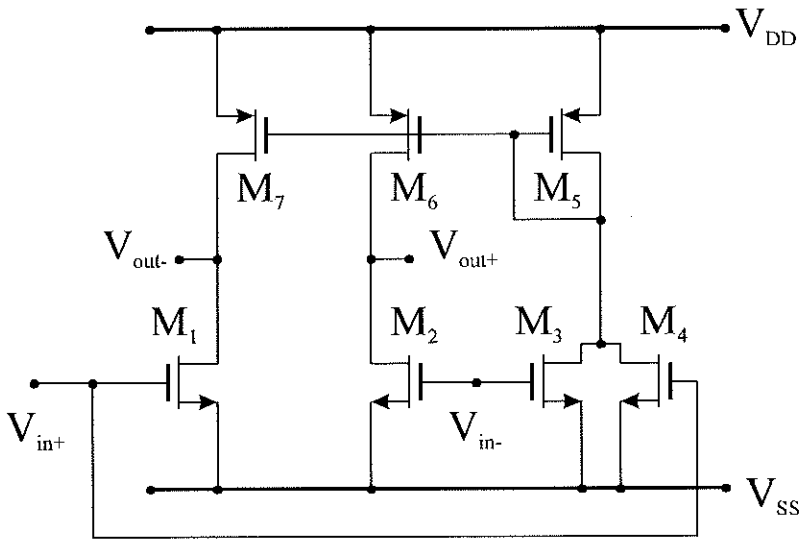

Figure 3.7: Pseudo differential amplifier with feed-forward common mode regulation

Disturbances from the power supply will be processed as common mode signals and is thus suppressed. The suppression is ultimately limited by the matching of the common mode resistors of the pseudo differential inverter.

3.2.4 Adaptive Bias Differential Stage

The simple differential stage has many advantages. One can mention good power supply rejection, good common mode rejection and reasonable linearity. It has though one big disadvantage. It is a pure class A circuitry. In [17] a differential stage / OTA with adaptive bias is proposed. The adaptive differential stage is shown in fig Fig. 3.10. transistors M_1, M_2, M_3,M_5 and M_6 is a normal differential stage, while M_4,M_7 and M_8 is the adaptive bias circuitry. The operation of the adaptive bias circuitry is a current rectifier that rectifies the differential output current and feeds it back to the sources of M_1 and M_2.

So a positive feedback loop assures that the bias current is increased as the differential input voltage increases. If the input pair is in weak inversion, then the input voltage output current transfer function becomes :

$$I_{out} = B \cdot I_0 \cdot \frac{\tanh(V_i/2nV_t)}{1 - D|\tanh(V_i/2nV_t)|} \tag{3.5}$$

Where B is the ratio between the aspect ratios of M_5 and M_3. While the ratio between the aspect ratio's of M_4,M_7 and M_3,M_8, is denoted D. D is the amount of positive feedback (loop gain, I_{dM1} to I_{dM1}), and must stay below 2. In Fig. 3.11 the output current as a function of the input voltage for different D values has been shown.

3.2.5 Low Voltage Class AB Amplifier

When designing low voltage amplifiers on chip normally it is quite sufficient to use single stage amplifiers. The large impedance levels that can be achieved on chip has the effect

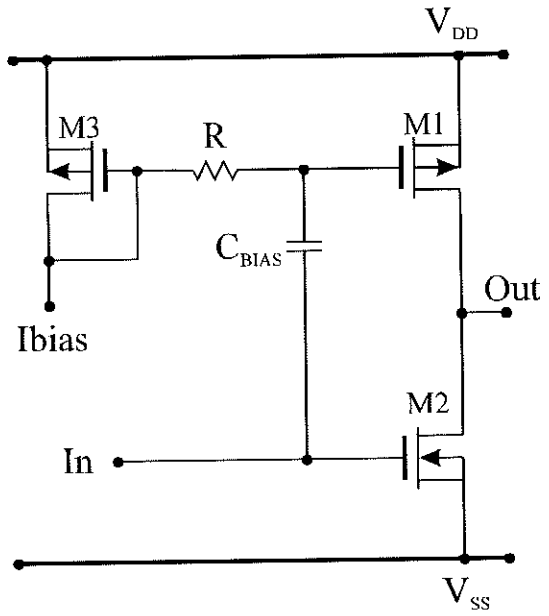

Figure 3.8: Low voltage inverter amplifier

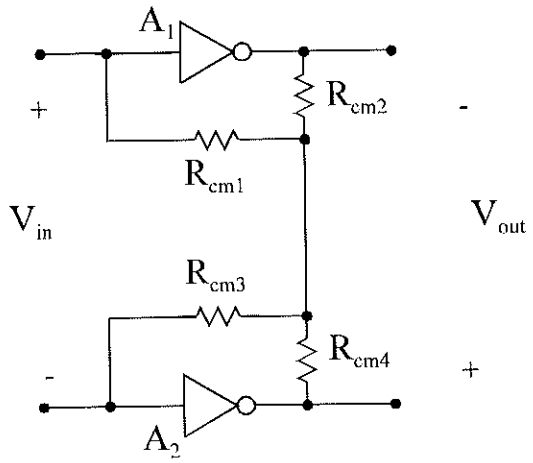

Figure 3.9: Pseudo differential low voltage inverter amplifier

that very large DC gains can be achieved using only single stage amplifiers. But when driving very small off chip resistive loads then the DC gain is grossly affected. The high impedance node where the high gain is achieved has to be isolated from the low resistance load. This means that the amplifier has to be at least a two stage amplifier. At low voltages only common source output stages can be applied. The most difficult task when designing low voltage amplifiers with common source output stages is to precisely to define the quiescent current in the output stage. Several quiescent current control circuits have been proposed (see [18] and [19]). All of these end up being very complicated. A very simple and elegant solution is shown in Fig. 3.12. This has been taken from [8] pp. 43. The operation can be explained as follows. There are two high impedance gain nodes. These are the gates of M_{10} and M_9. The amplifier is compensated with two miller capacitors, C_1 and C_2. The quiescent current control is a integrated part of the amplifier. Aspect ratios of transistors M_3 to M_8 is $\frac{W}{L}$, while

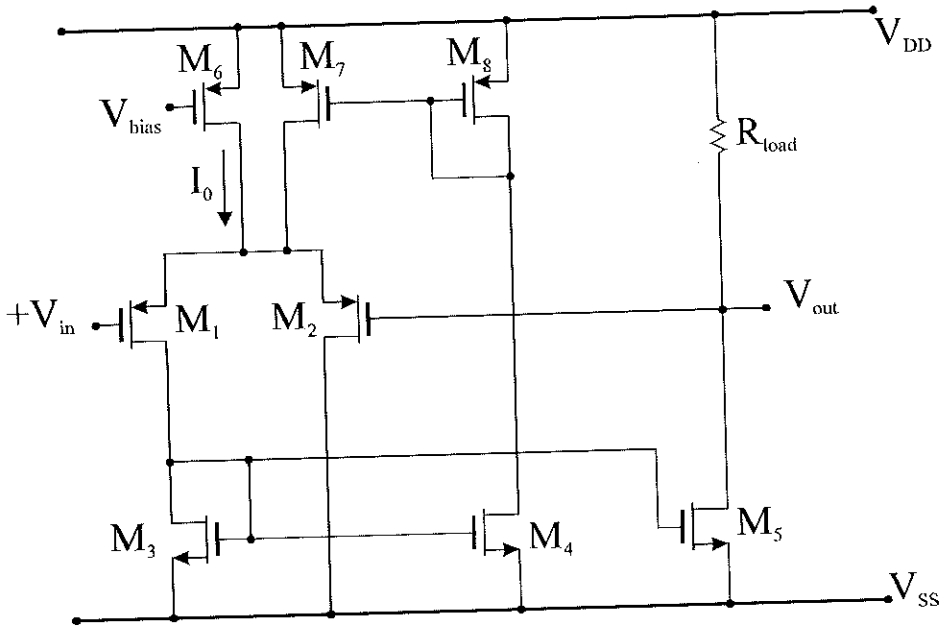

Figure 3.10: Adaptive differential stage

it is $10 \cdot \frac{W}{L}$ for M_9 to M_{10}. This assures that the current efficiency of the amplifier is good and that the quiescent current is not to large. A global feedback loop will assure that the quiescent current of M_5 and M_6 is equal. And as the quiescent current in M_6 is set by the gate source voltage of M_3, thus is the quiescent currents of M_9 M_{10} also set precisely.

3.3 Time Discrete Low Voltage Amplifiers

By introducing switching to low voltage amplifier design, operation at low voltages becomes much more easy to implement and problems with time continuos designs are purely eliminated. Furthermore switching allows us to generate any voltage that are needed to operate the circuitry correctly. Voltages above the power supply voltage can furthermore be generated to enhance the operation of the circuitry.

3.3.1 Switched Inverter Amplifier

The switched inverter was originally proposed by Hosticka [20]. The basic idea of the switched inverter is to separate the gates of the NMOS and PMOS transistor by a bias voltage. In this way stacking is avoided and the switched inverter is capable of operating at very low power supply voltages. Instead of the Ac level shifter introduced in [16], the switched capacitor level shifter is now introduced [21]. We will use the Fig. 3.13 to explain the operation of the switched inverter.

Operation of the Switched Inverter Amplifier

We will use the Fig. 3.13 to explain the operation of the switched inverter. The inverter of Fig. 3.13 is connected as an inverting integrator. The capacitance C is a

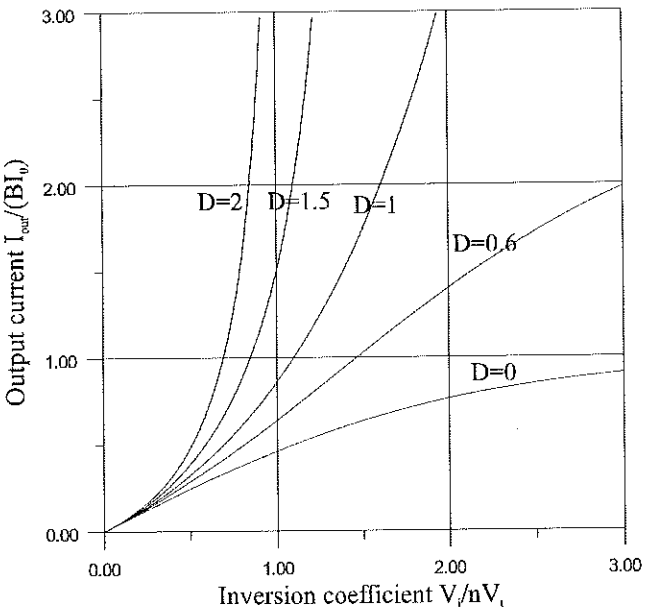

Figure 3.11: Output current of the adaptive amplifier in weak inversion.

switched capacitor level shifter that separates the DC levels of the gates of M_1 and M_4. Transistors M_2 and M_3 are cascoding transistors, which enhance the low frequency gain. The cascoding can be designed to function within 230mV of each of the supply rails. But the inverter will still be able to function rail to rail.

The operation of the switched inverter amplifier is as follows. During phase 1 (the biasing phase), the drain current of M_1 is set by the gate source voltage of M_5. As M_4 is diode connected during phase 1, then the drain current of M_4 is also set precisely. The gain capacitance C_S is connected to ground and the voltage of In- sampled. The integration capacitance C_f is not connected during phase 1. Otherwise the information stored on C_f would be lost during phase1 and no integration would occur. During phase 2 the gain capacitance C_S is now connected to the input and the voltage at node In is again sampled and subtracted. This in fact implements correlated double sampling of the voltage of In. This suppresses the power supply voltage variations and low frequency 1/f noise from the transistors. As the integration capacitance now is connected and the inverter also is connected to the output then the charging of C_S is reflected as a voltage on the output of the inverter.

Improvements of the Switched Inverter Amplifier

The correlated double sampling employed in the switched inverter amplifier greatly increases the poor power supply rejection ratio of the basic inverter. The correlated double sampling is equivalent to a filter function of (see appendix C):

$$H(Z) = 1 - Z^{-1/2} \tag{3.6}$$

Which has an amplitude of :

$$|H(Z)|^2 = |\sin(\pi f/f_s)| \tag{3.7}$$

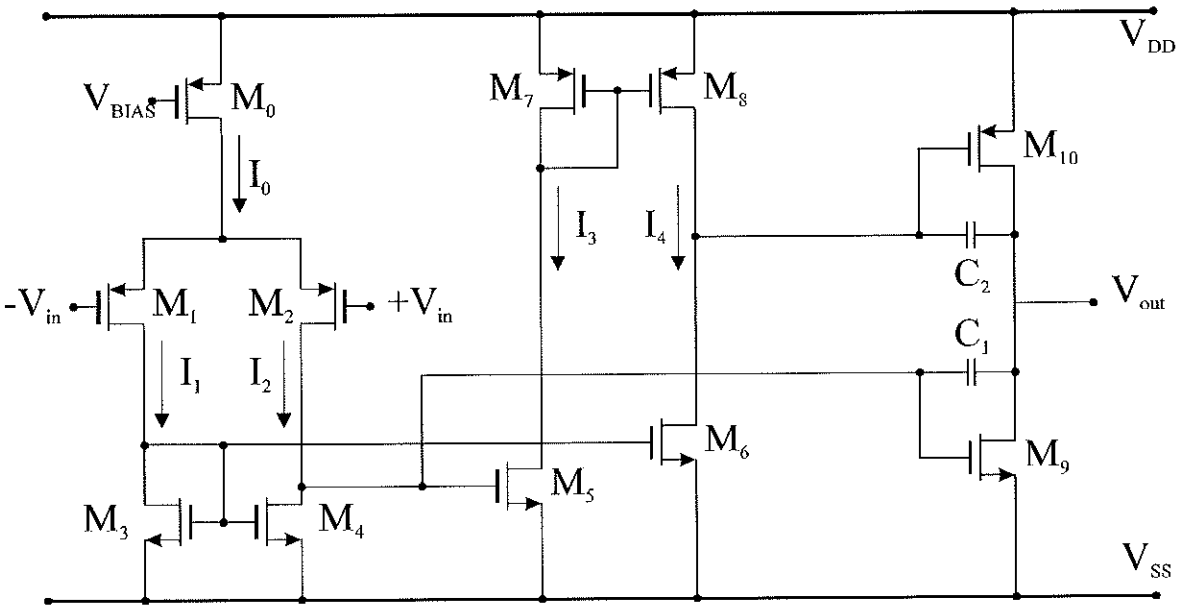

Figure 3.12: Class AB amplifier. $I_1 = I_3$ and $I_2 = I_4$.

Where f_s is the sampling frequency. This has the effect of suppressing low frequency components, but unfortunately frequency components around frequencies of $f_s/2$ are submerged into the low frequency range. This comes from the fact that we sample a signal and half a clock period later we subtract it from a new sampled value. If the frequency of the sampled signal is close to half a clock period then we will effectively get a component near DC. In switched capacitor circuits there will always be disturbances of the power supply voltage at frequencies around $f_s/2$.

The problem only exists at frequencies around multiples $f_s/2$. So we need to enhance the power supply rejection ratio at high frequencies. This can be done by introducing a regulation of the power supply voltage. Such a circuit is shown in Fig. 3.14

The gate of M_2 (capacitance C_2) is charged to such a voltage that the transistor is saturated. The source of M_2 will the be at approximately $V_{DD} - 200mV$. In this way an attenuation of power supply disturbances of approximately 40dB, can be achieved. The drawback of the regulation is that it lowers the effective power supply voltage with about 200mV. This circuitry has not been presented before. Another way to enhance PSRR is to use a pseudo differential coupling of two inverters with common mode feedback, as in section 3.2.3. It will be shown later how this can be implemented.

3.3.2 Switched Buffer Amplifier Stages

An important circuit design block is the buffer amplifier. i.e. an amplifier with unity gain. This is needed when large capacitive or/and small resistive loads have to be driven. There are two ways of implementing switched buffer amplifiers. One is to use the switched inverter in a unity gain, the other to implement a switched source follower stage.

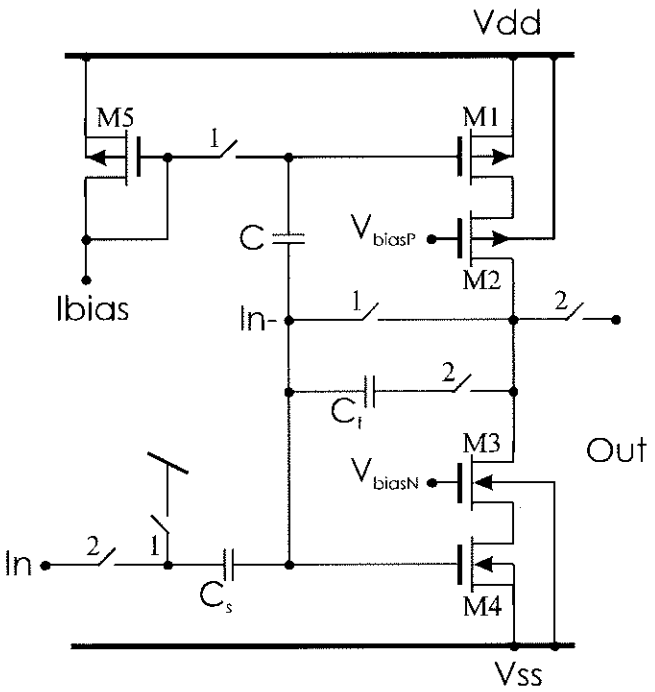

Figure 3.13: Switched inverter amplifier

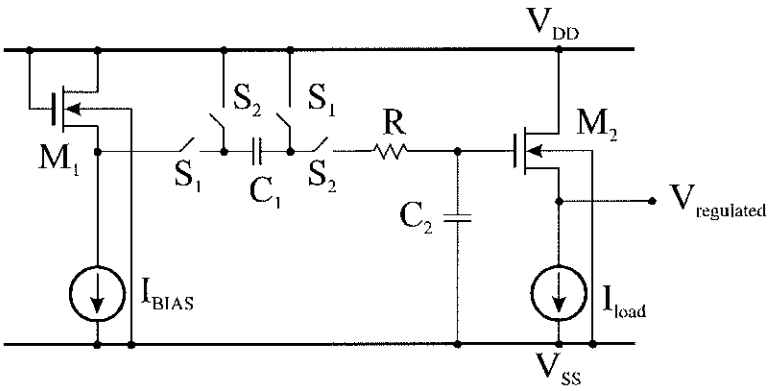

Figure 3.14: Switched capacitor voltage regulation

Switched Inverter Buffer Amplifier

The switched inverter buffer amplifier is a very good example of a circuit that exploits the principle of maximal output swing and minimal input signal swing. At phase 1 the input signal and the input voltage of the inverter is sampled at C_S and at phase 2 the capacitor is flipped. The output voltage will then be very close to the sampled input voltage. The input and output voltage can be rail to rail. The voltage swing at the input of the inverter is very small as the node is virtually ground. This technique can only be used for capacitive loads. A low value resistive load would deteriorate the gain. This is why we need an alternative.

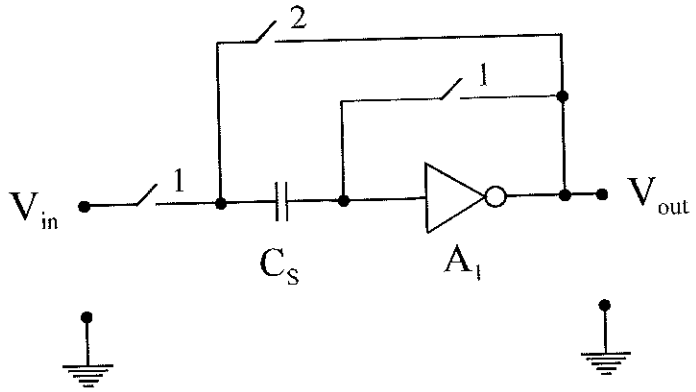

Figure 3.15: Switched inverter buffer amplifier

Switched Source Follower

An alternative, suited for driving low value resistive loads, is the switched source follower. Again switched capacitor level shifting is used to enhance operation. The voltages of the gate nodes, of a push pull source follower, can easily extend the power supply voltage range if a switched capacitor level shifter is used. The operation is as follows.

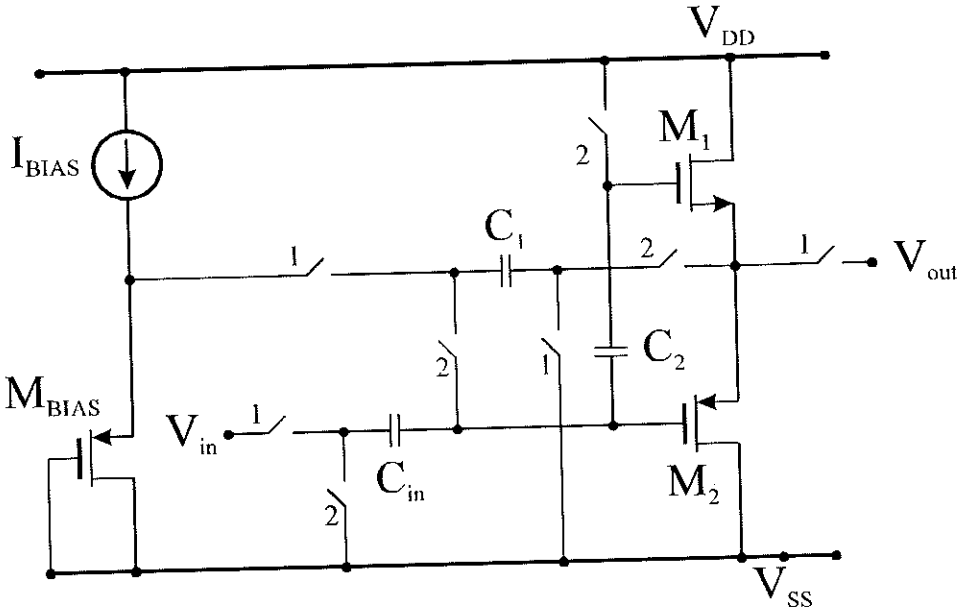

Figure 3.16: Switched source follower stage

During phase 1 the capacitor C_1 is charged to the gate source voltage of M_{BIAS}. At phase 2 the charge is then shared with the gate source capacitance of M_2, while the gate voltage of M_1 is fixed to V_{DD}. Each repeating phase 2 will then charge the gate source capacitance of M_2 until the drain current of M_2 equals the one of M_{BIAS}, which is equal to I_{BIAS}. The drain current of M_1 will then also be equal to I_{BIAS}. In the phase 1, the source follower is then available. The switched source follower has not been presented before.

3.3.3 Fully Differential Switched Inverter Amplifier

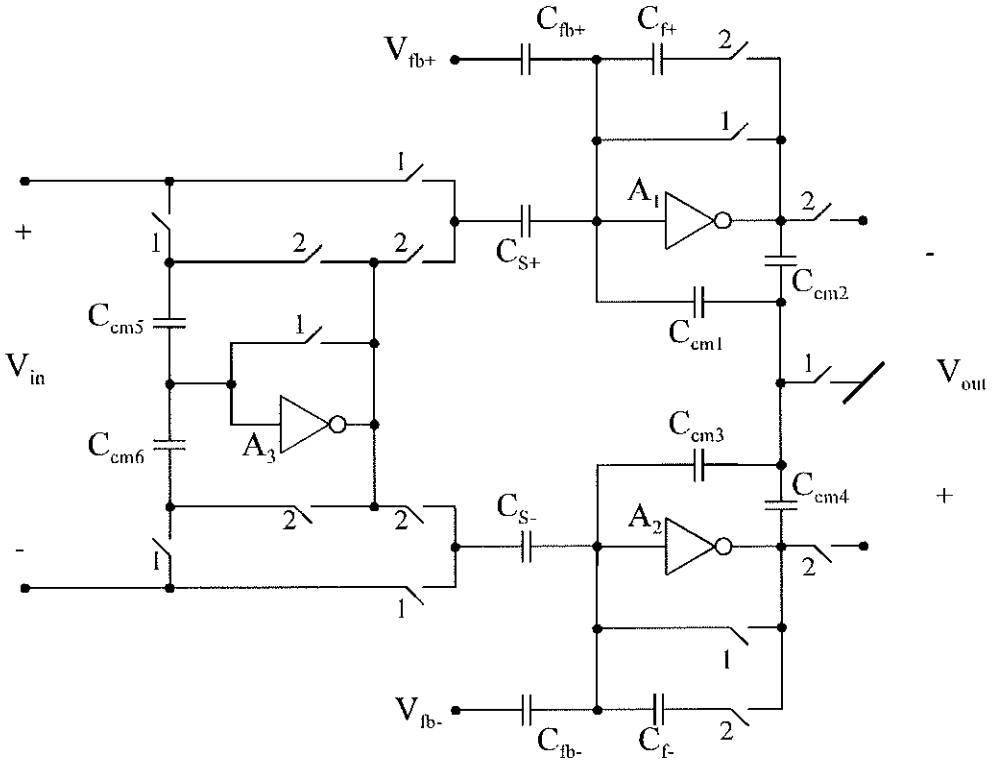

Figure 3.17: Fully differential switched inverter

The switched inverter amplifier can be used to implement a pseudo differential amplifier. This is quite analogue to the time continuos pseudo differential amplifier. But here the common mode feedback resistors have been replaced by their switched capacitor counterparts. I.e. switched capacitors in the common mode feedback instead of resistors. The pseudo differential amplifier can be seen in 3.17. The circuit of 3.17 is a switched capacitor integrator. The pseudo differential operation with common mode feedback has the advantages of enhanced PSRR and improves signal swing. The operation is as follows. At phase 1 the input signal is sampled onto capacitors C_{cm5}, C_{cm6},C_{S+} and C_{S-}. And at phase 2 common mode part of the input signal is subtracted from the sampled voltage of capacitors C_{S+} and C_{S-}. It is thus only the differential part of the input signal charge that is transferred to the integration capacitors C_{f+} and C_{f-}. Furthermore common mode disturbances at the output of the integrator is suppressed by common mode feedback capacitance's C_{cm1}, C_{cm2},C_{cm3} and C_{cm4}. The differential switched inverter amplifier is further discussed in chapter seven.

3.4 Conclusion

It is possible to design circuitry that can operate a power supply voltage just above the threshold voltage of CMOS transistors. CMOS technology is at the moment the most flexible technology for low voltage design. This is mainly due to the very high

input impedance of the CMOS transistor. This allows us to use AC level shifting and switched level shifting.

Especially the low voltage switched circuits are interesting. Switching actually allows us to add all the normal high supply voltage features to low supply voltage circuitry at the expense of increased complexity. Furthermore, a biasing phase normally has to be added.

Chapter 4

Σ Δ A/D Modulators

In this chapter the basic theory of Σ Δ modulators is resumed. This is mainly based on [22] and [23]. Furthermore, considerations concerning low power Σ Δ A/D converters / modulators are treated. A very comprehensive collection of papers of is presented in [24]. Σ Δ A/D converters is, as it will be shown later, interesting from a low power perspective. Furthermore, they possess interesting features when it comes to interfacing of electromechanical systems. This will be shown in chapter five. The advantages of the $\Sigma\Delta$ modulator that have made it so popular is : good linearity and no need for very accurate matching of analog components. The one bit modulator furthermore has the advantage of being very easy to implement at low voltages and at low power consumption.

4.1 Traditional Signal Acquisition

Interfacing continuos time analog signals with their time discrete digital counterparts involves three distinct operations. These are : Anti-aliasing filtering, sampling and quantization. This set of tasks we will denote signal acquisition [23]. In the tra-

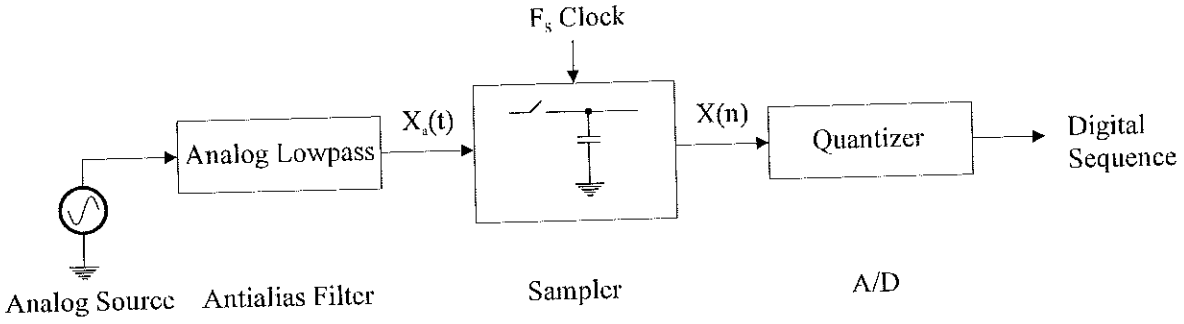

Figure 4.1: Traditional signal acquisition system

ditional signal acquisition systems these tasks are performed separately, se Fig. 4.1. Anti-aliasing (AA) filter assures that the signal to be sampled , including unwanted components such as noise and out of band interference ,is properly bandwidth limited prior to sampling, which would otherwise fold (alias) into the base band (signal band).

Sampling of the band limited signal from the AA filter quantizes the signal in time. At this point the signal is still analog but discrete in time. The last operation is then to quantize the analog signal levels into discrete levels. In the next section we will see how oversampling merges the three signal acquisition operations so that they no longer occur in isolated steps.

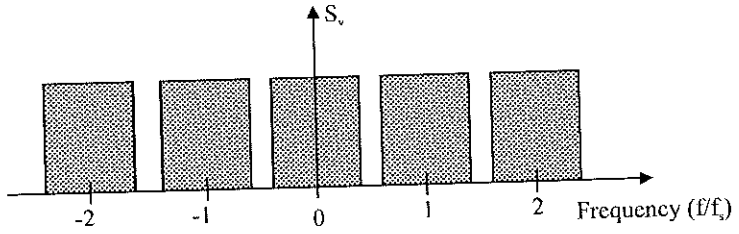

Figure 4.2: spectrum of sampled signal

4.2 Oversampling to Facilitate Anti Alias Filtering

Oversampling equals representing an analog signal at a sampling rate deliberately above (often far above) its nyquist rate. Oversampling has the advantage of moving the spectral replicas away from each other, se Fig. 4.3, thus making the AA filtering a much easier task. In case of very large oversampling factors, analog AA filtering can even be omitted (moved to the digital domain). Fig. 4.2 shows the spectrum of a sampled signal. And Fig. 4.3 shows the same signal sampled at a much higher sampling rate than the nyquist rate. As the analog signal is sampled at a frequency $OSR \cdot F_s$, much larger than F_s it is often not necessary to do the AA filtering at the input.

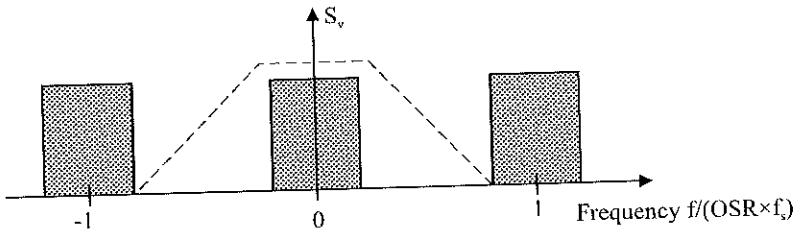

Figure 4.3: Anti-aliasing at a higher sampling rate

Instead the signal is sampled and quantized immediately. Before lowering the sampling frequency to the originally desired F_s, one has to digitally filter the sampled and quantized signal. This is to assure that no aliasing occurs. So the AA filtering has now moved to the digital part of the system. The steps of filtering the signal and lowering the sampling rate is denoted decimation and the block doing this operation the decimator. An over-sampled acquisition system can be seen in Fig. 4.4. If we resume, then there are four steps. Sampling at high sampling rate , quantization, digital low pass filtering and last, lowering of the sampling frequency. The two last operations, filtering and lowering of sampling frequency are normally denoted decimation.

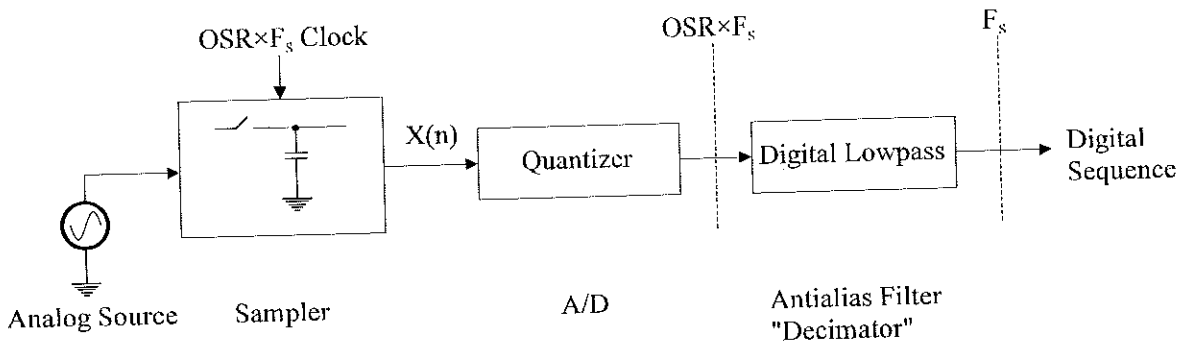

Figure 4.4: Over-sampled signal acquisition system

4.3 Oversampling to Facilitate Quantization

Separate in motivation from AA filtering is the use of oversampling and decimation to increase a quantizers effective resolution. Because the quantization noise is considered to white and its total power is constant one can easily recognize that increasing the sampling frequency will lower the noise level. This is due to the fact that the total noise power which is constant is spread over a larger frequency span, thus giving a smaller amplitude. One could see this as moving a part of the quntization noise to a high frequency were it can be removed by a decimation. The term noise shaping is used for the operation of moving noise outside the signal band. Normally it is used for high pass shaping of the quantization noise spectral density.

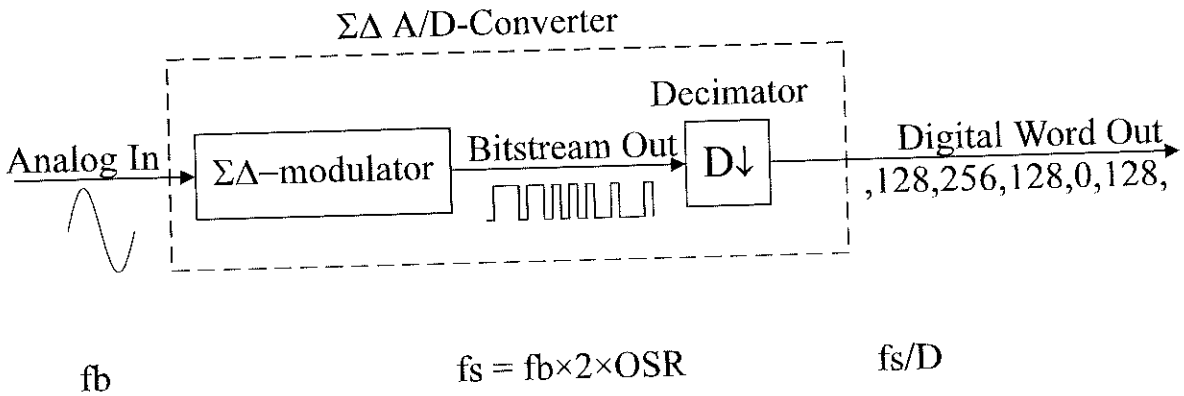

Figure 4.5: 1 bit Σ Δ A/D converter scheme

Noise shaping in conjunction with 1 bit (two level) quantization is especially interesting. Why, will be explained later. Such a scheme can be seen in Fig. 4.5. The modulator converts the analog low frequency signal into a 1bit stream at a very high sampling frequency and the decimator filters the bit-stream and lowers the sampling frequency. The decimator actually converts the bit-stream into digital words. The decimator is a digital filter and is beyond the scope of this work. We will now introduce the Σ Δ modulator and a linear model of it.

4.4 The Σ Δ A/D Modulator

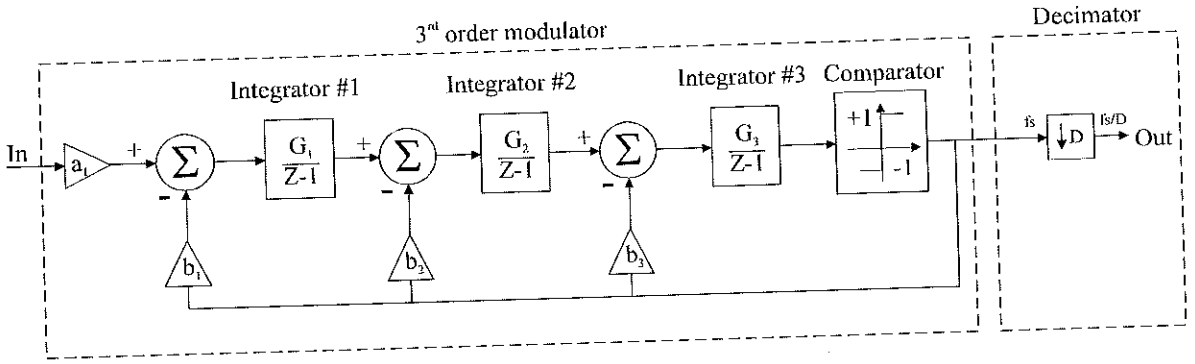

Figure 4.6: A 3^{rd} order Σ Δ A/D converter consists of a 3^{rd} order modulator plus a decimation filter

A Σ Δ A/D converter consists of two blocks. Namely the Σ Δ modulator plus a decimator. The function of the decimator has already been explained. A schematic of a so called 3^{rd} order multiple feedback modulator is showed in Fig. 4.6 There are other types of modulators (e.g. MASH) but as the cascaded type seems to be the most simple to implement and from a low power perspective, these other types have not been dealt with in this work . The principles of noise shaping also applies to other types of modulators. The 3^{rd} order modulator consists of three cascaded integrators (from that the 3^{rd} order). The multi-bit quantization has been replaced by a one bit quantizer. In the figure represented by a comparator. In order to reveal the properties of this structure we will investigate a linear model of the modulator.

4.5 Linear Modeling of Σ Δ Modulators

As the modulator contains a nonlinear element (the comparator) the usual (LTI, Linear Time Invariant) tools for evaluating the frequency properties can not be used. So we will have to model the comparator in such a way that the traditional analysis tools can be used. The simplest way to model the modulator, allowing us to facilitate the usual tools, is to model the quantizer (comparator) by a gain of one plus some additional white noise. This can be seen in Fig. 4.7. At this point we will introduce two transfer functions. The Signal Transfer Function (STF) and the Noise Transfer Function (NTF).

The Signal Transfer Function is the transfer function from the input of the modulator to the output, and the Noise Transfer Function is the transfer function of the noise from the quantizer to the output. These are depicted in Fig. 4.8. As we see the Signal Transfer Function is a low pass filter while the Noise Transfer Function is a high pass function. The signal is left unaffected in the base band while the noise is shaped and moved to higher frequencies. This is the basic nature of noise shaping.

The assumption of the noise being white does not hold as the noise and the signal is correlated. A consequence of using a fixed gain of one for the quantizer is that the NTF changes as the feedback filter is scaled, whereas the real modulator is invariant

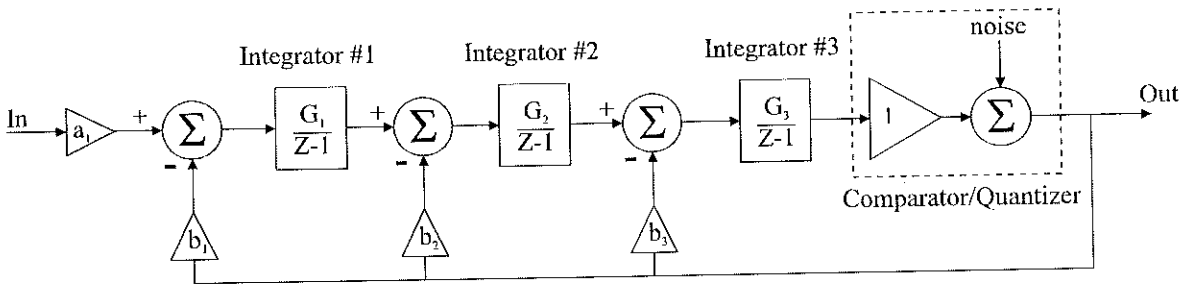

Figure 4.7: 3^{rd} order Σ Δ modulator with quantizer gain of 1

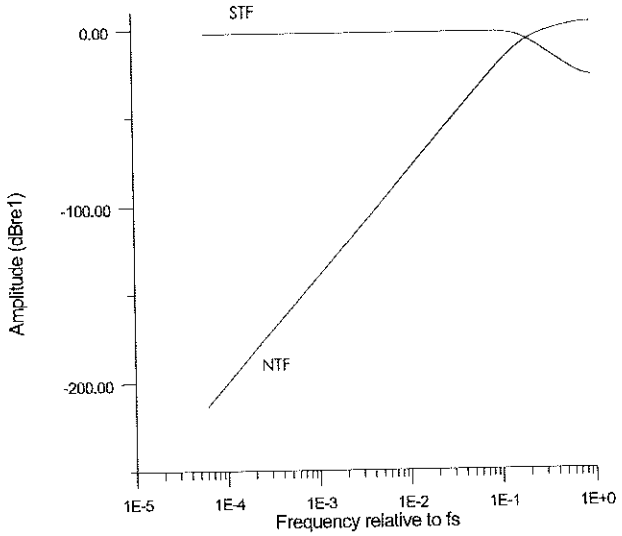

Figure 4.8: Signal transfer function (STF) and noise transfer function (NTF)

to such scaling (the comparator does not look at the amplitude of the signal but only its sign). Also the fully linear model with gain of one has problems predicting stability/instability This leads us to quasi linear modeling, which in fact takes the scaling invariance into account.

4.6 Quasi Linear Modeling of Σ Δ Modulators

We will in the following use the generic Σ Δ modulator model of Fig. 4.9. In this model the gain of the quantizer is not fixed .

It can be derived from Fig. 4.9 that

$$STF_K(z) = \frac{K \cdot G(z)}{1 + K \cdot H(z)} \tag{4.1}$$

$$NTF_K(z) = \frac{1}{1 + K \cdot H(z)} \tag{4.2}$$

This is the signal transfer function and the noise transfer function. Normally H(z)

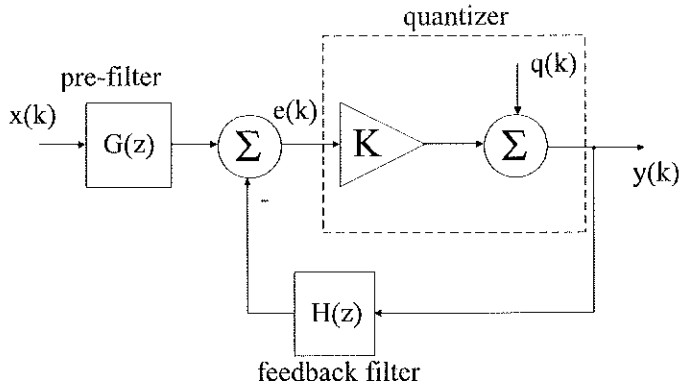

Figure 4.9: Generic Σ Δ modulator with linear quantizer model

is a low pass filter with large gain at DC and G(z) = H(z). This gives us the frequency response as in Fig. 4.8.

We will now make some simplifications and assumptions. First of all, the input signal x(k) is restricted to constant signals. The motivation for this simplification is that the modulator input is heavily over-sampled. Secondly, the quantization noise q(k) is modeled as a stochastic noise source. Finally, the mean value $m_y = E\{y(k)\}$ of the modulator output is used as a descriptive parameter, i.e. the modulator is supposed to operate with a constant input m_x, which gives a prescribed mean output m_y. For the traditional modulator having G(z) = H(z) and where H(z) has very high DC-gain, the modulator loop ensures that $m_y \simeq m_x$. In order to model q(k) as a zero mean noise source, it is necessary that the gain factor K only applies for AC-components, i.e. the gain K is generally not the ratio between the mean values of the quantizer input and output. The linear model of Fig. 4.9 will thus be treated as an AC-model, i.e. it only applies for AC-components of the signals. However the knowledge of the mean modulator output affects the AC-model. It can be shown that, if the noise q(k), is white, has zero mean and variance σ_q^2 then :

$$A(K) = \frac{1 - m_y^2}{\sigma_q^2} \tag{4.3}$$

Where :

$$A(K) = \sum_{k=0}^{\infty} |ntf_K(k)|^2 = \|ntf_K\|_2^2 \tag{4.4}$$

A(k) is equal to the area under the NTF curve (se Fig. 4.8) The ntf(k) with a quantizer gain of K is denoted $ntf_K(k)$. The $ntf_K(k)$ is the impulse response of the $NTF_K(z)$ filter, see equation 4.2. A(K) is normally denoted the noise amplification factor. If we plot A(K) as a function of K for a higher order modulator we see (4.10) that it is a ∪ convex curve and there exists a global minimum which we will denote A_{min}. The noise amplification factor will later be used to predict stability / instability.

If the quantizer output is split up into three components, namely a DC-component, the amplified AC-component and the quantization noise then the quantizer gain can be found to :

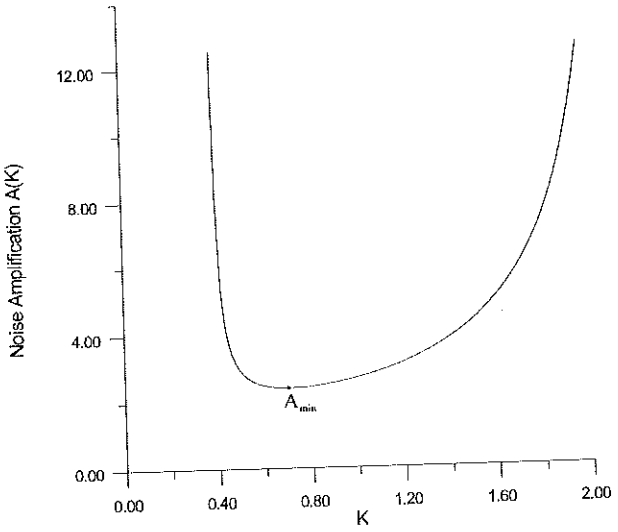

Figure 4.10: A(K) curve for a higher order modulator (≥ 3)

$$K = \frac{Cov(e(k), y(k))}{\sigma_e^2} \tag{4.5}$$

Where σ_e^2 is the quantizer input variance. The analysis methods above were first presented in [25].

4.7 Stability Measures

As the normal linear stability measures have proven to be inadequate regarding stability of $\Sigma\Delta$ modulators new measures of stability have been developed. None of these stability measures use a fixed gain of the quantizer in order to predict the stability of the modulator. Instead they use the frequency response and the impulse response of the NTF in order to predict stability/instability.

4.7.1 Gaussian

The Gaussian stability criterion is based on the assumption that the amplitude distribution of the input signal to the quantizer is Gaussian. From this the quantizer noise variance $\sigma_q^2 = 1 - m_y^2 - K^2\sigma_e^2$ combined with equation 4.3 gives us:

$$A(K) = \frac{1 - m_y^2}{1 - m_y^2 - \frac{2}{\pi} \cdot e^{-2 \cdot (erf^{-1}(m_y))^2}} \tag{4.6}$$

Where m_y is the mean output of the quantizer, and $erf^{-1}(\cdot)$ is the inverse error function. As $m_y \simeq m_x$ A(K) can now be found as a function of the mean value of the input signal. If we now combine equation 4.4 and equation 4.6 we get :

$$A_{eq}(K_{eq}) = A(m_y) \tag{4.7}$$

Where the left hand side is found using equation 4.4 and equation 4.6 for the right hand side. From Fig. 4.10 it is seen that for each A(K) (or mean value m_y) there exists two K values.

It can be shown that the one K value is stable and the other instable.

The exception is the A_{min} value, where only one K value exists (see Fig. 4.10). Here the stable and the instable K values unites to one instable K value. This K value corresponding to A_{min} always gives an instable system.

It can thus be concluded that when the mean value m_y of the output signal is below the value corresponding to A_{min} then the system will be stable. This value will be denoted as the maximum stable amplitude (MSA)

$$A_{min} = \frac{1 - m_y^2}{1 - m_y^2 - \frac{2}{\pi} \cdot e^{-2 \cdot (erf^{-1}(m_y))^2}} \Big|_{m_y = MSA} \tag{4.8}$$

The left hand side can then be found, calculating the minimum of equation 4.4 as a function K. And as $m_y \simeq m_x$ we can formulate it in terms of the mean value of the input signal. The Gaussian stability criterion generally performs better as the modulator order increases. I.e. the accuracy of the Gaussian criterion improves for higher order modulators.

4.7.2 BIBO

The BIBO stability criterion is based on the fact that for a stable modulator the output will stay bounded as long as the input stays bounded. In order to derive the BIBO criterion we will first describe the modulator by the generic model of Fig. 4.11

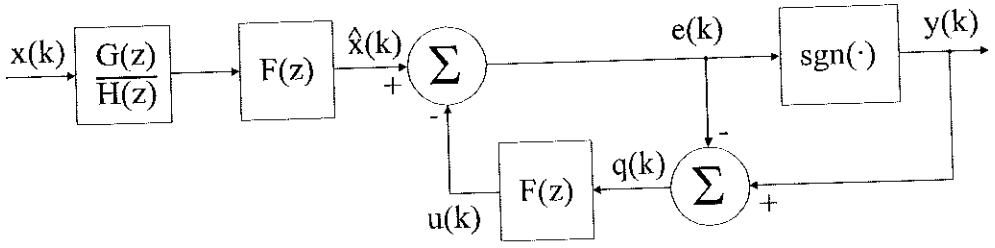

Figure 4.11: Generic modulator model

From this the improved BIBO stability criterion can be deducted :

$$\|x\hat{}(k)\|_\infty \leq 3 - S_{min} \tag{4.9}$$

Where S_{min} is the global minimum of :

$$S(K) = \sum_{k=0}^{\infty} |ntf_K(k)| \tag{4.10}$$

The Gaussian stability criterion and BIBO stability criterion are quite analogue. The Gaussian is based on the two norm of the NTF while BIBO is based on the one norm of NTF. While the Gaussian is quite precise in predicting stability , the BIBO criterion is ironclad but often too conservative.

4.7.3 F_{max}

The third stability criteria that can be used in conjunction with the two others is the F_{max} criteria. It is based on the fact that if $\|f(k)\|_1$ is below 2 then the maximum magnitude of the filter F(z) is also bounded by two (see Fig. 4.11).

$$F_{max} = \|F_{min}(z)\|_\infty \leq 2 \tag{4.11}$$

Where $F_{min}(z)$ is the frequency response of the filter $F_K(z)$ with a quantizer gain of K and minimum one norm.

$$F_K(z) = \frac{K \cdot H(z)}{1 + K \cdot H(z)} \tag{4.12}$$

All of these three can be used for the characterization of the stability of the modulator. The question is then, what do we need three stability criteria for ? This will now be explained in the following subsection.

4.7.4 MSA and Reliability

In [22] the term a 'reliable' modulator is introduced. What is a reliable modulator. In [22] it is shown that certain types of modulators have a very low escape rate, i.e. they are instable but the instability is so weak that it is only revealed during very long simulations. Simulation times that are much longer than what can be practically processed numerically today.

The normal way of determining the MSA by simulations is to use a ramp input revealing the true MSA. But if the modulator is unreliable then the sweep rate needed to reveal instability could be so small that it is not feasible to simulate the MSA this way. Furthermore a unreliable modulator designed for a MSA of 0.4 might be instable at much lower input levels than the designed MSA.

A reliable modulator is on the contrary characterized by a high escape rate, i.e. it reveals its instability very quickly. It should be remembered that every modulator can be brought to oscillate for certain internal states. Reliable modulators quickly reveals the oscillation.

How do we separate the reliable modulators from the unreliable ones ?

In [22] a method of exhaustive search for long transients leading to instability is introduced. For different input levels the states in the modulator is pertubated several thousand times and the maximum time to instability is picked out. This can then be plotted as a maximum transient plot. A maximum transient plot for a very reliable modulator is seen in Fig. 4.12. The reliability is seen as a very low level of the maximum transient length up to approx. 0.45 which also was the simulated MSA.

The question is now how do we design reliable modulators ?

It is shown in [22] that reliability is strongly connected to the two parameters S_{min} and F_{max} being too high compared to A_{min}. We will later describe a design method for higher order modulators that gives highly reliable modulators with a very good dynamic range.

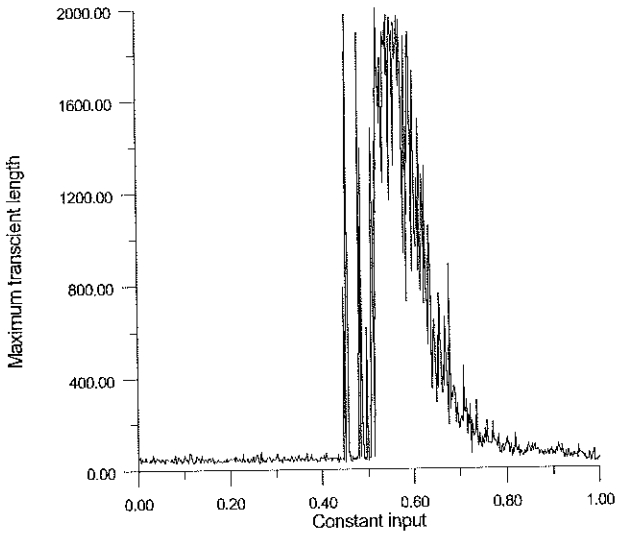

Figure 4.12: Plot of maximum transient length versus constant input

4.8 Performance Prediction

In this section we will describe a method of evaluating the performance of a $\Sigma\ \Delta$ modulator.

4.8.1 Maximal Signal to Noise Ratio SNR

First we will try to estimate the quantizer gain. This can be done remembering that, when operating, the modulator will tend to minimize the noise power at the input of the quantizer. This could also be stated as :

$$min(||ETF_K(k)||_2^2) \tag{4.13}$$

Where $ETF_K(Z) = \frac{-F_K(Z)}{K}$. The corresponding K can then be used as the quantizer gain

An approximate measure of the base band noise power for zero input can be found by calculating :

$$\sigma_b^2 = \frac{1}{A_{eq}} \int_0^{f_b} |\frac{1}{1 + K_{eq} \cdot H(e^{(j\pi f)})}|^2 df \tag{4.14}$$

Where f_b is the upper base-band limit frequency relative to half the sampling frequency. By using the K found from equation 4.13 then A_{eq} and finally σ_b^2 can be found.

An estimate of the maximal signal to noise ratio SNR_{max} can then be found using :

$$SNR_{max} = 10 \log(\frac{MSA^2}{2 \cdot \sigma_b^2}) \tag{4.15}$$

Where MSA can be calculated using equation 4.8 and the input signal is assumed to be sinusoidal. The question is now what MSA should we design for ? Inspecting equation 4.15 it seems that increasing MSA will also increase SNR_{max}. This is also true to some extent. But designing for a high MSA is equal to designing for a low

cutoff frequency of the NTF filter function, which gives a poor suppression of the quantization noise. This can be observed by simulating the A_{min} of a given NTF and the finding the corresponding MSA. An optimal MSA (or cutoff frequency of NTF(z)) exists.

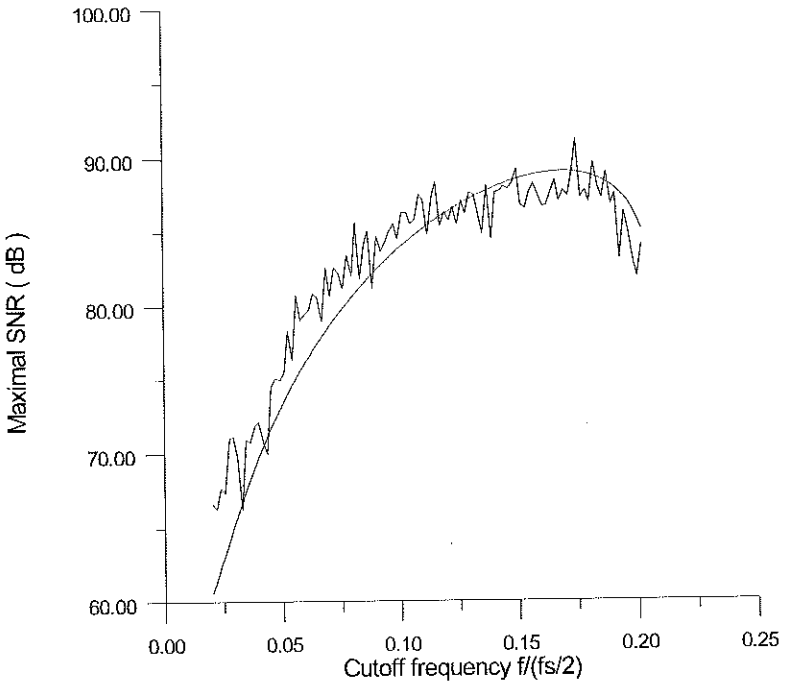

Figure 4.13: Maximal SNR vs. NTF cutoff frequency

In Fig. 4.13 the peak signal to noise ratio vs. cutoff frequency of the noise transfer function NTF of a third order modulator. The NTF was a butterworth high pass filter function. The smooth curve is SNR based on the prediction of the SNR, while the tagged curve is simulated SNR of the modulator. It can be seen that the optimum of the maximal SNR is around 0.15 - 0.175 relatively to half the sampling frequency. In [22] it is stated that the optimum normally is situated around an MSA of 0.35 which in this case corresponds to a cutoff frequency of 0.19. In this, the in band tones has also been taken into consideration. This will now be explained.

4.8.2 In Band Tones

The existence of in band tones generated by the modulator and how to avoid them will now be explained. The in band tones are unavoidable but they can be suppressed so much that they are of no importance. The ideal modulator will, when exposed to a signal, generate harmonics. These will be odd order if the input signal is symmetric. If a DC is present then also even order harmonics will be present. The modulator generated harmonics will always be present. They will though be heavily suppressed by the feedback loop. The amplitude of the harmonics are thus very dependent of the loop gain. From these simple facts we can conclude that increasing the modulator order and/or increasing the cutoff frequency of the NTF filter will diminish the harmonics. This is due to the increased loop gain. Increasing the cutoff frequency of the NTF filter

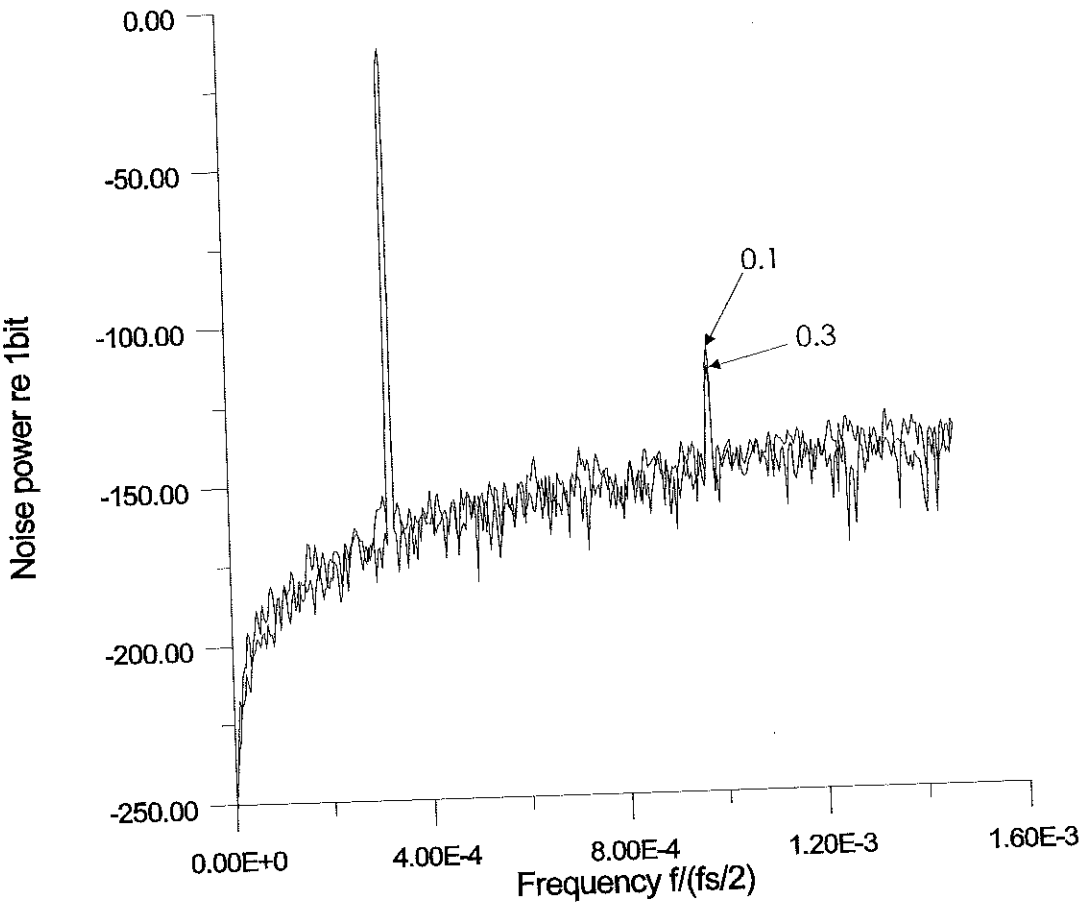

Figure 4.14: Harmonics of two 3^{rd} order modulators with NTF cutoff frequency of 0.1 and 0.3 relatively to $f_s/2$

will lower the harmonic distortion but unfortunately it is not the optimum for maximal SNR. In [22] it was stated that 0.19 would be an good choice for the cutoff frequency of the NTF filter. In this both considerations of maximal SNR and an acceptable level of harmonics has been taken into consideration. At it is seen from Fig. 4.14 the signal amplitude of the two modulators is exactly equal but the 3^{rd} order component is for the modulator with cutoff frequency of 0.3 somewhat lower. In Fig. 4.15 two 4^{th} order modulators with cutoff frequencies of the NTF filters of 0.1 and 0.3 relatively to $f_s/2$. It is seen that the 3^{rd} order component of the 4^{th} order modulator with cutoff of 0.1 is much lower than the one of the 3^{rd} order modulators, see Fig. 4.14. And for the 4^{th} order modulator with NTF cutoff of 0.3 it has totally disappeared. The cutoff of 0.3 is though far too high as NTF cutoff frequency for optimum SNR is approx. 0.14 relatively to $f_s/2$. But what can be learned from these examples is that higher order modulators generally perform a better coding of the signal. i.e. tones are better suppressed. When designing $\Sigma\ \Delta$ modulators one has to trade off between optimum SNR and suppression of harmonics.

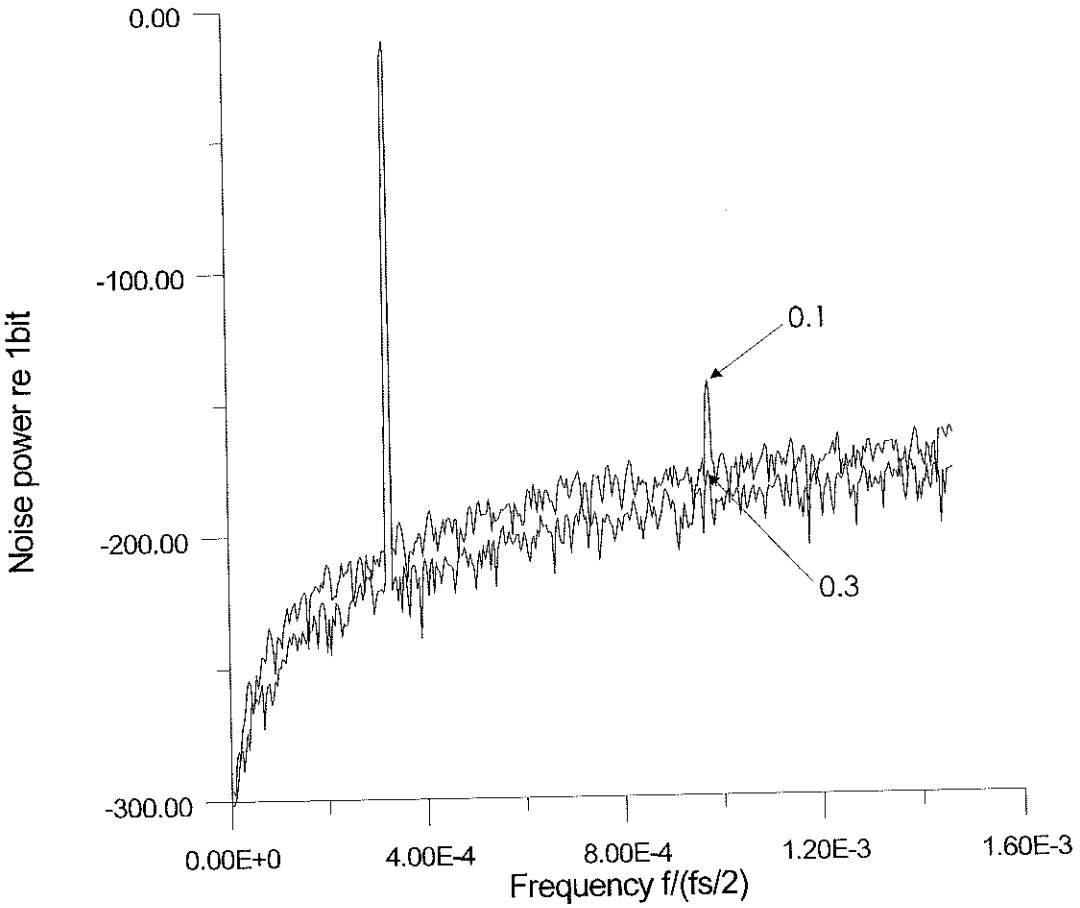

Figure 4.15: Harmonics of two 4^{th} order modulators with NTF cutoff frequency of 0.1 and 0.3 relatively to $f_s/2$

4.9 Low Power Σ Δ Modulators and Design Procedures

As a Σ Δ modulator is an analog circuit then an interesting performance measure is the SNR for a given power consumption and especially the lowest power consumption for given SNR, we will now treat ΣΔ modulators from that point of view. i.e. how to design low power ΣΔ modulators. That is ΣΔ modulators that consumes minimum power for a given SNR. But first of all. Why are ΣΔ modulators so interesting from a low power perspective ?

4.9.1 Why Low Voltage / Low Power Σ Δ Modulators ?

One of the objectives of introducing over-sampled ΣΔ A/D converters was that a large part of the analog signal processing could be performed in the digital domain. It is obvious that this is an advantage as the amount of analog signal processing is reduced. But is it also advantageous from a low power perspective ?

In chapter one it was seen that when dynamic range exceeds 60-80dB then digital signal processing uses less power than analog. It is worth noting that this is with to-

day's digital technology. More advanced technology will favor digital signal processing even more. In [26] it is stated that the power consumption of the digital part of a Σ Δ modulator can be as low as 20% of the total.

Another is point to consider is the use of oversampling. One might falsely conclude that over sampled A/D converters are very power consuming. For fixed capacitance values of analog signal processing the power consumption will normally increase linearly with the sampling frequency, But one should remember (see chapter two) that the signal to noise ratio S/N in over-sampled analog signal processing is proportional to both capacitor and oversampling rate OSR:

$$S/N \sim C \cdot OSR \tag{4.16}$$

And that the consumed power will be proportional to processed frequency times $OSR \cdot C$

$$Power \sim f \cdot C \cdot OSR \tag{4.17}$$

This actually means that increasing the oversampling rate OSR does not mean extra power consumption as long as the capacitance value can be scaled accordingly, keeping the product $C \cdot OSR$ constant.

4.9.2 Analog Noise vs. Quantization Noise

In the ideal ΣΔ modulator the only noise source is the shaped quantization noise. But when implementing a real ΣΔ modulator noise from analog circuitry will add to the total noise. In Fig. 4.16 noise sources of the three integrators of a third order modulator are depicted. It is easily recognized that apart from quantization noise only noise from the first integrator is of importance. This is due to the fact that the transfer function from noise1 to the output are a low pass filter with gain close to one at low frequencies and transfer functions of noise2 and noise3 to the output is high pass functions. This can be exploited to minimize the power consumption dramatically. As the noise from the first integrator is dominant the following integrators are allowed being noisier without affecting the total SNR of the modulator. This means that the power consumed in the integrators following the first integrator can be scaled down. Typically by a factor of four to ten.

4.9.3 Choosing and Designing Modulator NTF

We will now describe how to choose and design the modulator NTF. The first task is to design the NTF filter. The choice made will affect both stability and maximal SNR, using the design procedure in [22] or [27] and [28]. The design method of [22] has been extended to low power modulators.

NTF Filtertype

We have seen that the stability of the modulator is solely determined by the NTF. And it is described by the three parameters A_{min}, S_{min} and F_{max}. The reliability and MSA of the modulator depended directly on these three parameters and could be simulated

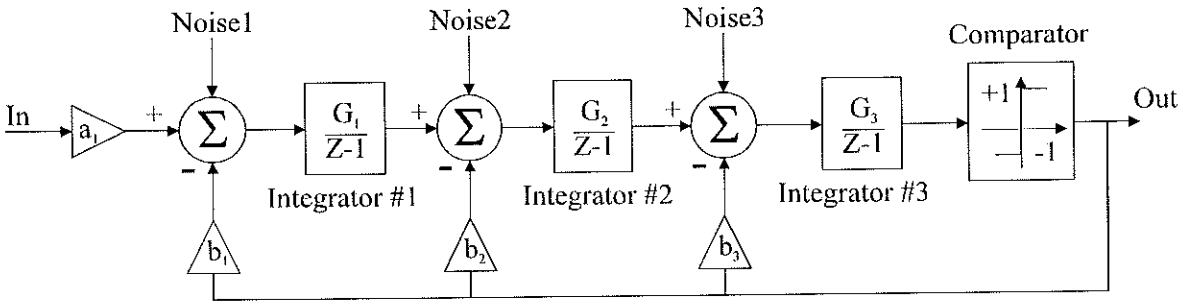

Figure 4.16: 3^{rd} order modulator with analog noise sources

by a maximum transient plot and a slowly increasing ramp. As for designing reliable modulators choosing a butterworth NTF seems as a good choice [22]. What MSA /cutoff frequency to design for is more complicated when looking at low power ΣΔ modulators. Also the order of the NTF has to be chosen.

Modulator Order

As we have seen it is advantageous that the modulator is of high order. First off all the quantization noise will be suppressed effectively and furthermore high order modulators perform a better coding. i.e. suppression of harmonics are better. The penalty for using high order modulators in a low power design are minimal. This is because the power consumption of the integrators can be scaled without affecting the total SNR. We can thus with high order modulators still maintain low power consumption, as the analog noise and the distortion of the first integrator is dominant. So the design of a ΣΔ modulator can be separated in to different tasks, designing a ideal ΣΔ modulator structure that do not influence the performance of the total modulator and an analog part optimized for minimum power consumption for a given SNR

NTF Cutoff Frequency

The question is now what the cutoff frequency of the NTF filter should be ? First we remember that the power consumption of analog signal processing under certain conditions is proportional to the quiescent current consumption (see chapter two). From this it can argued that the power consumption is proportional to $\frac{1}{V_p^2}$, where V_p is the peak value of the sine wave processed.

$$Power \sim \frac{1}{V_p^2} \tag{4.18}$$

If we divide the S/N of the modulator with its power consumption we can find an optimum cutoff frequency concerning S/N/Power. This is depicted in Fig. 4.17 Both

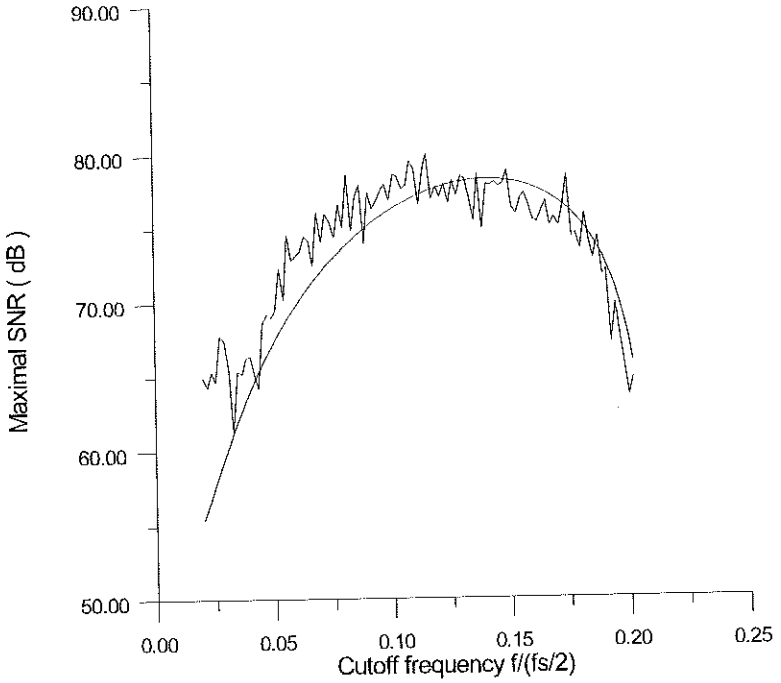

Figure 4.17: Maximal S/N/Power vs. NTF cutoff frequency

simulated (tagged curve) and predicted SNR (smooth curve) are shown. It is seen that the optimum cutoff frequency is around 0.10 to 0.15 relatively to half the sampling frequency

4.10 Conclusion

In this chapter we have treated the $\Sigma\Delta$ modulator from a theoretical point of view. Stability measures and design procedures have been presented. Furthermore tools to predict the performance have been presented. And last low power $\Sigma\Delta$ modulators are treated. It is argued that $\Sigma\Delta$ modulators are fully compatible with low power designs. Finally, design procedures for low power $\Sigma\Delta$ modulators are presented.

Chapter 5

Force Feedback of Electromechanical Systems

In this chapter a so called electromechanical system is described. It is shown that the $\Sigma\ \Delta$ has numerous advantages as an interface circuitry to mechanical sensors. In this chapter the sensor analyzed is a capacitive microphone.

5.1 Electromechanical Systems

One of the most commonly used electromechanical systems is the crystal oscillator, the crystal is used as a mechanical band pass filter.
The combination of electronic circuitry or electrical and mechanical element is here called an electromechanical system. Why are such systems so interesting ? Apart from the obvious advantages of a crystal oscillator, electromechanical systems haven't been very popular due to price and size. What makes them so interesting now is the perspective of making mechanical micro sized sensors using photolithography adopted from micro electronics technology, which allows them to be integrated "on-chip" [29]. This opens up the possibility of adding extra functionality. Feedback loops give the possibility of controlling overall parameters, linearity and using the mechanical sensor as a integrated part of the circuitry.
As a large part of my Ph.D. work has been focused on a force feedback mode microphone this will be used a an example of a electromechanical system.

5.2 The Differential Capacitive Microphone

In Fig. 5.1 a principle of a differential capacitive microphone is shown [30]. The principle is as follows. It consists of two fixed perforated back plates and a movable middle membrane. An incoming sound pressure will cause the membrane to deflect. Thus increasing the capacitance from the membrane to back plate # 2 and decreasing the capacitance between the membrane and back plate # 1. The differential capacitance value is then proportional to the incoming sound pressure.
The microphone is intended to operate inside a force balanced feedback loop. Because the membrane is kept in a virtually fixed position, the air gap can then be made

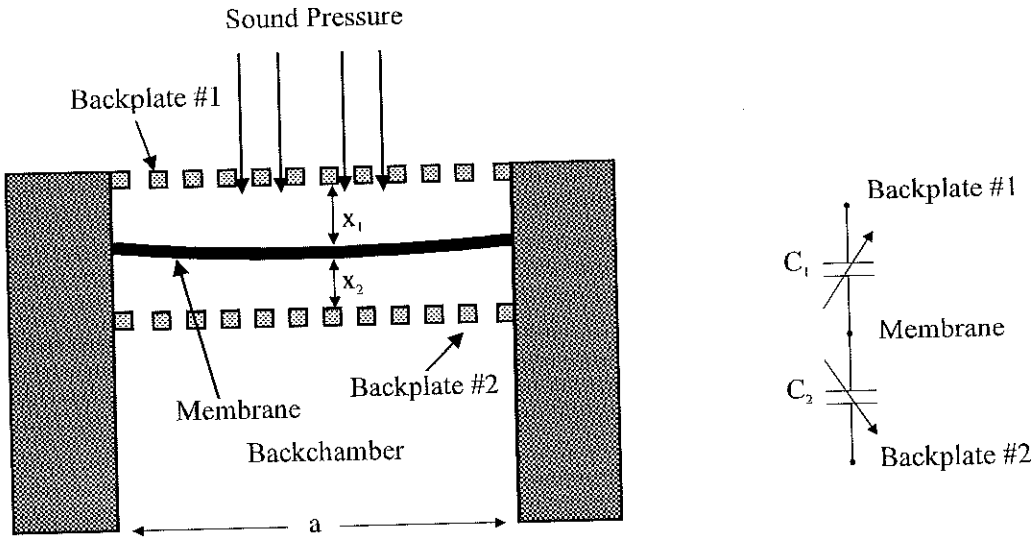

Figure 5.1: Differential capacitive microphone and electrical equivalent

smaller and the membrane softer. This gives advantages in sensitivity. But one relies fully on the feedback-loop. So it crucial that the feedback-loop is active in the entire signal band, from DC to above the resonant frequency. The microphone does not have separate terminals for feedback and detection so they have to be applied at the same terminals.

5.2.1 Frequency Response of a Microphone

A microphone is an electro acoustical system. To evaluate the frequency response it is custom to make an electrical equivalent circuit of the microphone. Normally nonlinear effects are disregarded. In electrical equivalents force is substituted by voltage and velocity by current. An electrical equivalent circuit of the differential microphone is shown in Fig. 5.2 [30] [31].

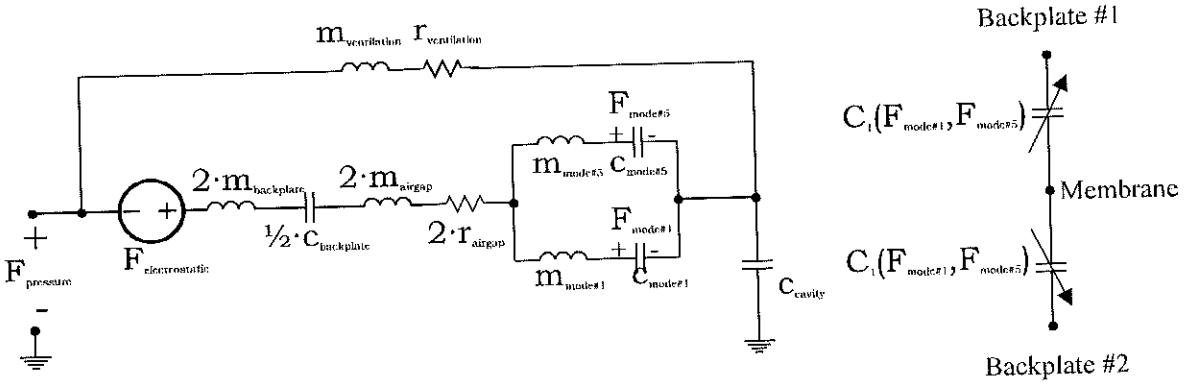

Figure 5.2: Electrical equivalent circuit of the differential microphone

We will now try to explain what the different parts of the microphone (Fig. 5.1) corresponds to in the electromechanical equivalent. The input is a force equal to the incoming pressure divided by the area of the membrane. Electrostatic force acting on the membrane is represented by $F_{electrostatic}$. The back plates are represented by

$m_{backplate}$ and $C_{backplate}$ which are the mass and compliance of the back plates respectively. The mass of the air between the membrane and the back plates are represented by m_{airgap}. As the squeezing of the air between the membrane and the back plates acts as a loss of energy then this is represented as a resistance r_{airgap}.

The membrane itself has several resonance modes. It is not all of them that can be detected. Some of them are symmetrical and therefore do not affect the total capacitance change. It can be shown that the two first modes that can be detected are mode #1 and mode #5 [32]. These are modeled as resonance circuits $m_{mode\#1}$ $c_{mode\#1}$ and $m_{mode\#5}$ $c_{mode\#5}$. There are infinite orders of modes but the ones above the fifth are not shown here. The total deflection of the membrane can thus be calculated as a superposition of the deflection in the different modes. This total deflection changes the capacitance's C_1 and C_2. A ventilation hole to prevent static pressure gradients is modeled by $m_{ventilation}$ and $r_{ventilation}$.The back chamber of the microphone is represented by c_{cavity}.

In Fig. 5.3 the frequency response of a microphone with two modes incorporated is shown. The force acting on the membrane is $1Pa \cdot 10^{-6}m^2$. Both the displacement amplitude and phase are sown. As one sees, there are two resonance peaks and between these a double complex left half plane zero. The zero has a very high Q which equals zero real part, i.e. the resonators have no loss. A high Q has the consequence that the amplitude at the zero is very small, ideally zero. This can be seen on the phase characteristic which suddenly jumps from -180^o to 0^o.

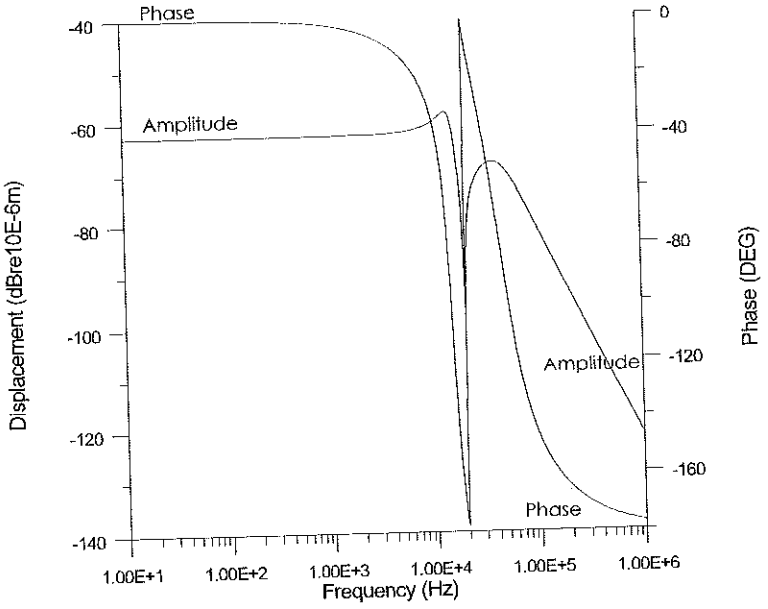

Figure 5.3: Frequency response of microphone. Bottom left, amplitude. Top left, phase

To explain what happens we will depict the membrane modes close to the zero. In Fig. 5.4 the two dominant modes # 1 and # 5 are shown. The deflection has been exaggerated. The total deflection is the super-position of the two. This can also be seen on Fig. 5.4.The zero in the frequency response represents the situation where the two modes cancels each other. At frequency just beneath the zero the phase shift of mode # 1 will dominate and just above the phase shift from mode # 5 will dominate.

And as mode # 5 is leading 180° of mode # 1 at the zero then the phase will jump 180° .

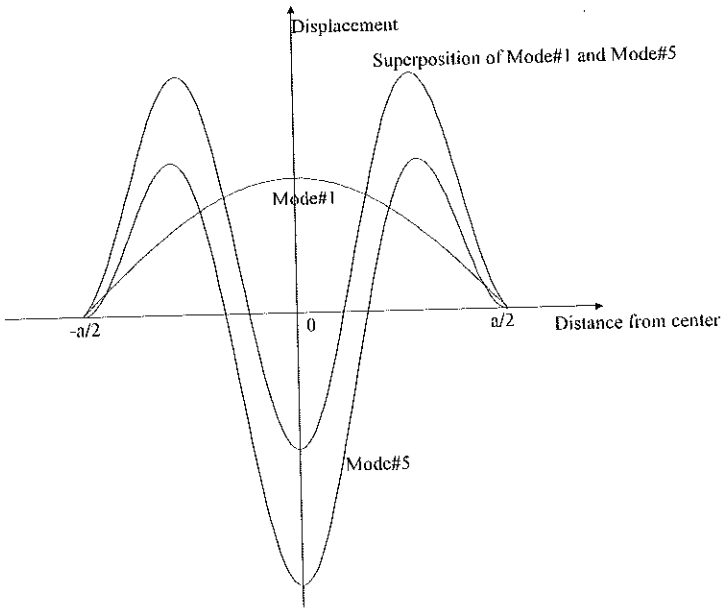

Figure 5.4: Mode #1 and #5 at a frequency just beneath the zero

The question is now, will this cancellation of modes happen in a real microphone ? The cancellation of the modes assumes that the two modes will be exactly 180° out of phase. In Fig. 5.2 the two modes have been modeled as loss-less resonators. If losses are added to the two modes then the two modes will not be 180° out of phase and the high Q of the zero will be reduced.
In measurements on real microphones the high Q zero as in Fig. 5.3 has not been observed. It can thus be questioned if the high Q zero will appear in the real world.

Nevertheless we will in the following use the model of a microphone with a very high Q zero as this is the worst case scenario.

5.2.2 Measuring Deflection

If we want to apply feedback to the microphone we would normally need to be able to apply feedback also at frequencies close to DC. This means that we have to be able to measure deflections at DC. There are only two ways this can be done. One is to use a sampled detection scheme [33] and the other is to apply a high frequency AC signal at the capacitance's [34]. The variation of the capacitance's will then AM modulate the carrier and a demodulator can be used to move the signal from the carrier to DC. In Fig. 5.5 the carrier and the two signal components around the carrier can be seen. At negative frequencies the spectra is repeated. The sampled spectra has a similarity with the AM modulated signal. The difference is that the signal components are repeated around $n \cdot \frac{f_s}{2}$, where $n \in]-\infty;\infty[$. And there is no carrier Fig. 5.6. The switching scheme is a two phase non overlapping clock scheme with 50% duty cycle.

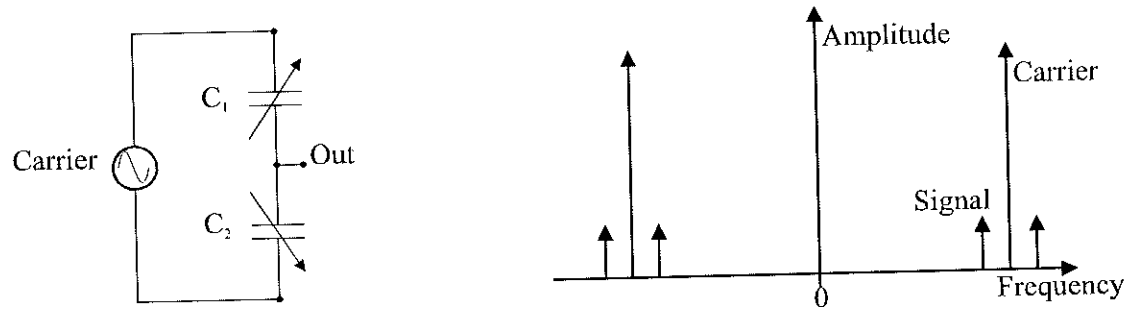

Figure 5.5: AM detection and output spectrum

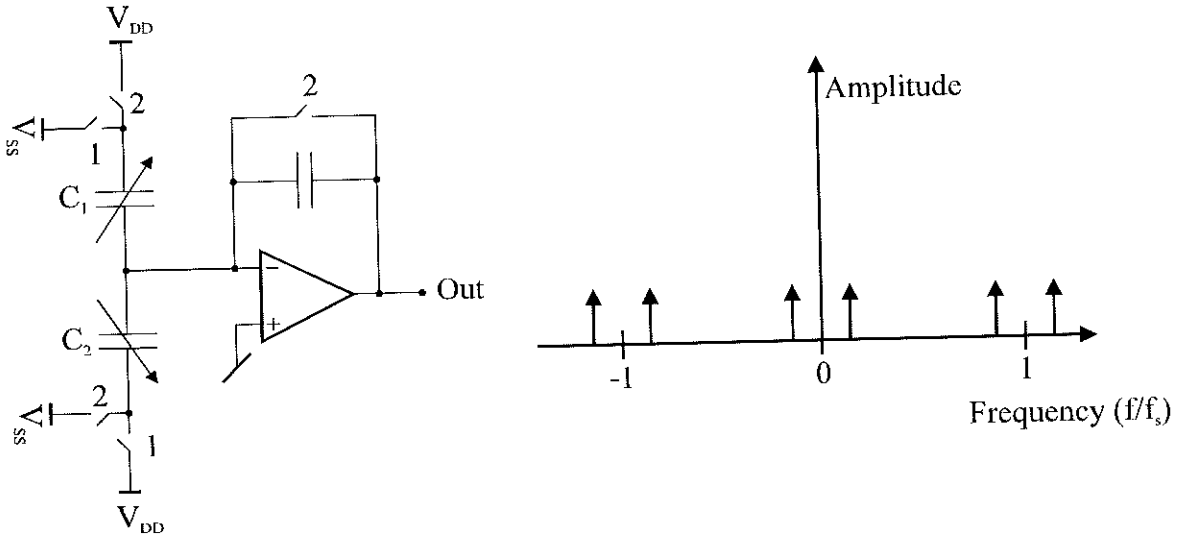

Figure 5.6: Sampled detection scheme and output spectrum

5.2.3 Electrostatic Feedback

If we want to apply feedback to the microphone this can be done by pressing a voltage over the capacitance's. A voltage of V_{ref} will act with a force F on the membrane.

$$F = \frac{\varepsilon_0}{2}(\frac{V_{ref}}{X_0})^2 \tag{5.1}$$

Where X_0 is the rest value of the distance between the membrane and the back plate. As the voltage to force function (equation 5.1) inherently is nonlinear it is necessary to invent schemes that cancels this non-linearity out. An option is in case of a differential microphone to suppress $+V_{ref}$, $-V_{ref}$ at the back plates #1, #2 and the feedback signal V_{fb} at the middle electrode this gives a total voltage to force function of :

$$F = \frac{\varepsilon_0}{2}(\frac{V_{ref} - V_{fb}}{X_0})^2 - \frac{\varepsilon_0}{2}(\frac{V_{fb} - V_{ref}}{X_0})^2 = 2 \cdot \frac{C_0}{x_0} \cdot V_{ref} \cdot V_{fb} \tag{5.2}$$

Which in case of fixed X_0 and V_{ref} are seen to be perfectly linear. But this linearity in only achieved is case of totally matching of the two capacitors and it requires generation of a negative supply voltage ($-V_{ref}$). A better way is to use a pulse-width modulated feedback signal with constant feedback voltage. The width of the pulse will

then determine how large a force we apply. In case of a differential microphone we can apply the force at both terminals and thus we have the opportunity to apply both positive and negative forces. The pulse-width can be both time continuos and time discrete. The latter is very interesting and will be treated later.

5.2.4 Separation of Feedback and Detection

Until now we have discussed how to detect and how to apply feedback, but not how to separate the feedback signal and the detected signal. This separation is needed as the feedback signal is applied at the same terminals where the deflection is detected. There are basically three ways of implementing this separation.

1. **Time multiplexing**
2. **Frequency multiplexing**
3. **Correlated double sampling**

Time Multiplexing

The first option is to use two time slots. One for detecting and one for applying feedback [33]. This requires that the detection method is sampling.

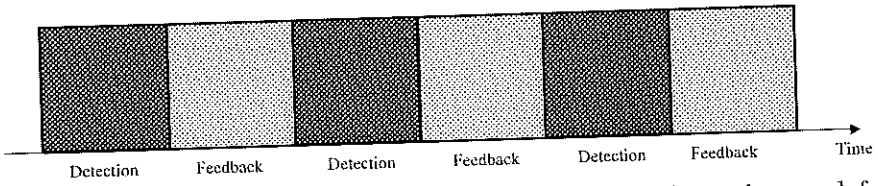

Figure 5.7: Time multiplexing. Different time slots for detection and feedback

Frequency Multiplexing

The second arises from the fact that the feedback signal and the detection signal can be applied at the same time but separated in frequency. This requires that the detection method is an AM modulated signal. A filter can then be used to pick out the AM signal [34].

Correlated Double Sampling

An offset (low frequency signal) used to apply the feedback is removed from the detected signal by correlated double sampling. This has the drawback that the correlated double sampling only is effective at low frequencies. So the separation of feedback signal and detected signal is only effective at low frequencies [35].

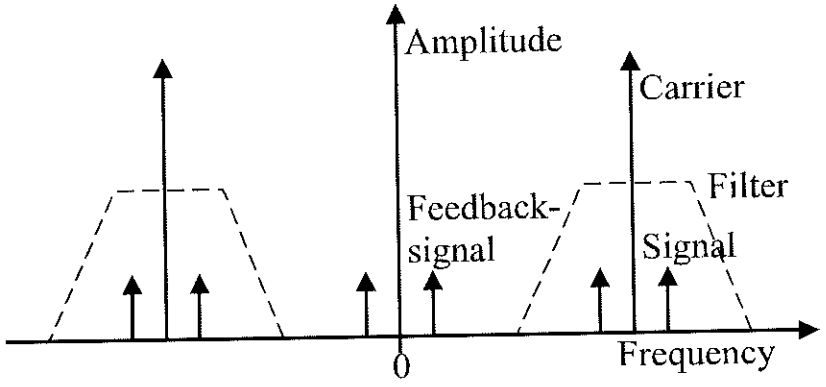

Figure 5.8: Amplitude modulated detection and low frequency feedback

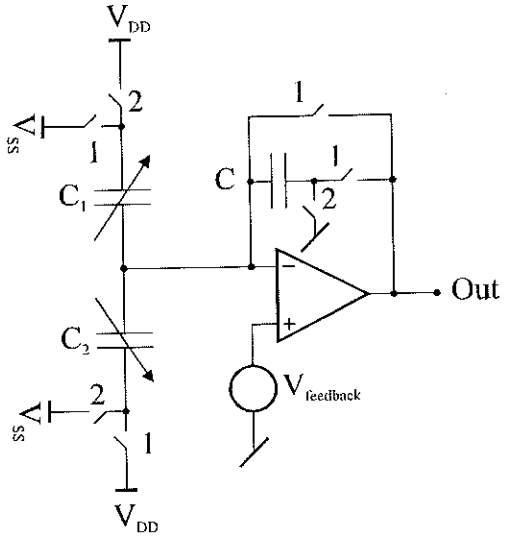

Figure 5.9: Correlated double sampling used to separate feedback and detection

5.2.5 Overview

If we should summarize the possibilities of detection and feedback then the conclusions will be : The feedback signals should be quantized in time, not in levels. This gives us the advantage of linear feedback. In case of a differential microphone it is advantageous to only apply the feedback at on terminal at a time. This is actually equivalent of applying positive or negative force. If low voltage / low power operation is required then the time multiplexed solution is very convenient.

All of this leads us to one very interesting implementation of a detection for a force feedback differential microphone : The electromechanical Σ Δ modulator. This will be described in the following section.

5.3 The Electromechanical ΣΔ Modulator

As discussed in chapter one signal processing in the future will mainly be done in the digital domain. So the sensors of the future will have to have digital output.

A feedback scheme that implements both force-feedback of a microphone and a

digital output is shown in Fig. 5.10. The scheme of Fig. 5.10 actually resembles that of a 3^{rd} order $\Sigma\Delta$ modulator. The difference is that the first integrator has been replaced by the microphone. The role of the microphone is in fact to act as an electromechanical integrator i.e. it is an integrated part of the noise transfer function [35]. At the same time this scheme implements force feedback of the microphone. The output of the modulator is a bit-stream. So a decimator has to be added to convert the bit-stream into a digital word. In the following electromechanical $\Sigma\Delta$ modulator will be treated thoroughly. First we will discuss how good an electromechanical integrator the microphone is.

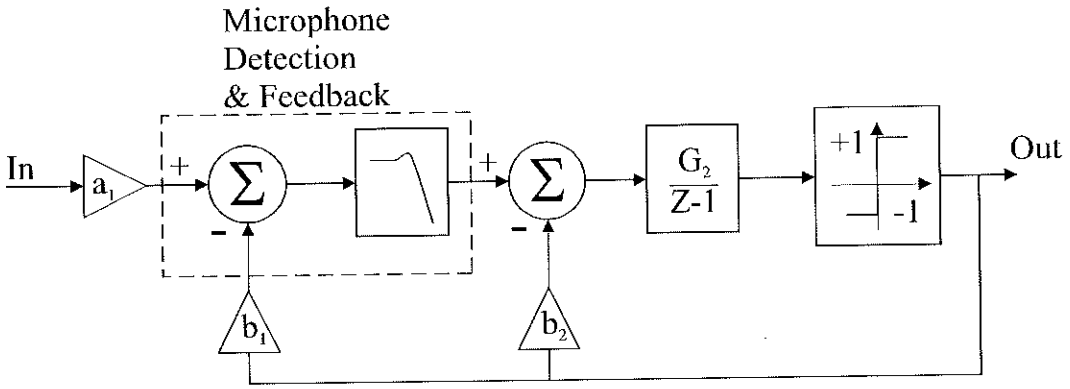

Figure 5.10: Electromechanical Σ Δ modulator

5.3.1 Designing Noise Transfer Function

We will now discuss how to design the noise transfer function of the electromechanical Σ Δ modulator. The electromechanical Σ Δ modulator of Fig. 5.10 has three feedback coefficients. But as the microphone has a second order characteristic, the NTF is effectively a third order NTF. So we have actually lost a degree of freedom. We will now discuss how to regain the extra degree of freedom. This will enable us to use the methods developed in chapter four.

PD Compensation, Adding a Zero

We will now introduce a proportional differentiating (PD) compensation block into the modulator structure. I.e. we will ad a zero in the loop. The electromechanical Σ Δ modulator with a PD compensation block can be seen in Fig. 5.11. The PD compensation block is equal to a filter function of :

$$PD(z) = 1 + b_0 \cdot Z^{-1} \tag{5.3}$$

Where b_0 is used to adjust the extra degree of freedom. i.e. we now have a fourth order modulator with four degrees of freedom. We will now show how to calculate the coefficients of the modulator and we will compare the performance of the electromechanical Σ Δ modulator with the ideal modulator. Furthermore we will point out what advantages and disadvantages there might be to the electromechanical Σ Δ modulator.

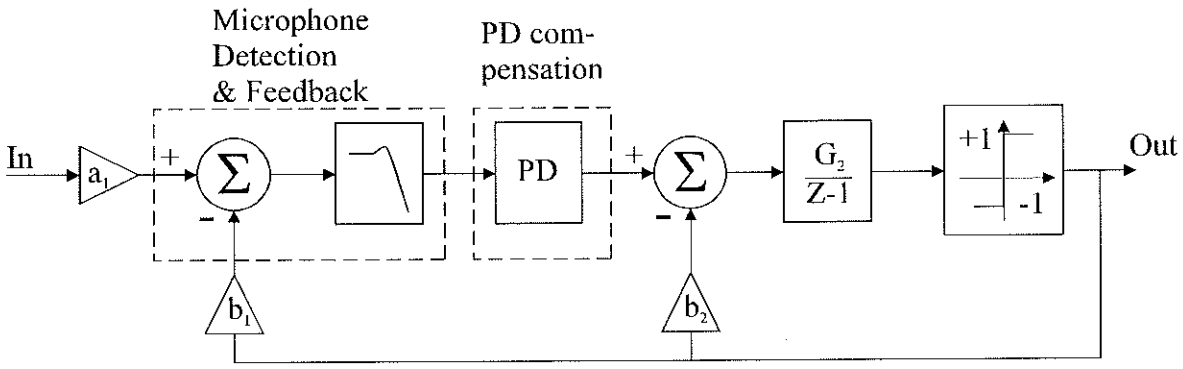

Figure 5.11: Electromechanical Σ Δ modulator with PD compensation

NTF Coefficients

We will now describe the procedure when designing the noise transfer function using a microphone with a PD compensation. First of all we notice that the sampled frequency response of the microphone can be approximated by :

$$H(z) \simeq \frac{\frac{\omega_1+\omega_2}{2 \cdot f_s}}{(1-Z^{-1})^2} \tag{5.4}$$

Which should equal a double integration of $\frac{1}{(1-Z^{-1})^2}$. So the microphone should be preceded by a gain of $\frac{2 \cdot f_s}{\omega_1+\omega_2}$. Where ω_1, ω_2 and f_s are the two resonance frequencies of the microphone and the sampling frequency. Now the coefficients can easily be calculated setting coefficient b_n equal to b'_{n+1}. Where b'_{n+1} is the coefficients of the normal modulator type. The zero b_0 of the PD compensation should equal $1 - \frac{b'_1}{b'_2}$

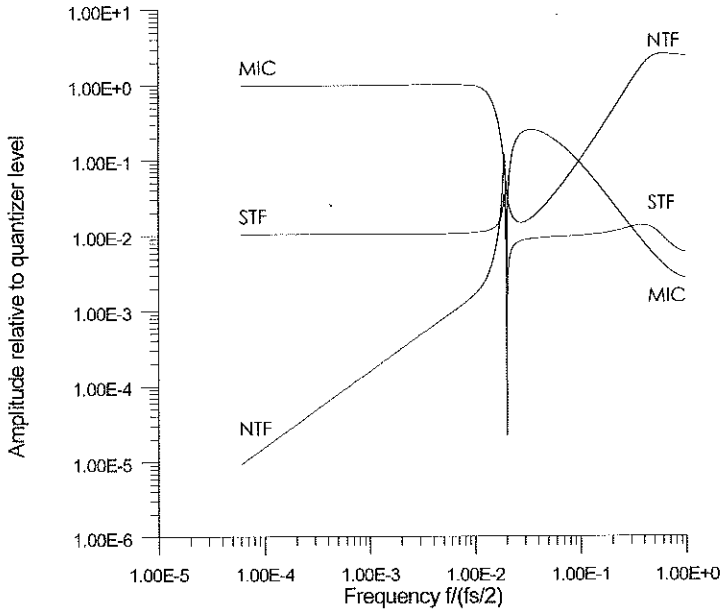

Figure 5.12: NTF, STF and sampled microphone frequency response of an electromechanical Σ Δ modulator

In Fig. 5.12 both NTF and STF of a 3^{rd} order electro-mechanical $\Sigma\Delta$ modulator is depicted. As it is seen the NTF is a high pass filter function with a 60dB/decade roll off at high frequencies. At low frequencies the roll off is only 20dB/decade. This is due to the fact that the microphone is not an ideal integrator so at low frequencies it is only the last integrator that is suppressing the quantization noise. One can see that the zero in the microphone response actually implies that the NTF has a peak. What consequences this have for stability and reliability will be discussed later.

5.3.2 Closed Loop Membrane Deflection

As one of the main reasons for placing the microphone inside a force feedback loop is to achieve better linearity , then we are interested in what the closed loop deflection of the membrane is. That is the feedback will reduce the movement of the membrane. At low frequencies it can be calculated to $\frac{b_1'}{b_2'}$. This can be seen in Fig. 5.13.

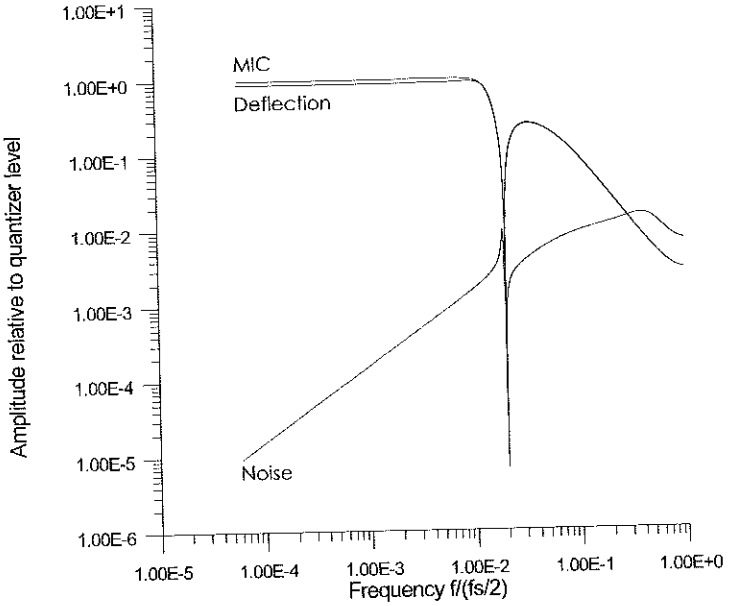

Figure 5.13: Closed loop deflection, residual noise and sampled microphone frequency response of an electromechanical Σ Δ modulator

Reducing Microphones Non-linearities

As the microphone is a differential structure all even order non-linearity's cancels out. This means that the force F vs. relative deflection x function will be of the type

$$F(x) = a \cdot x + b \cdot x^3 \tag{5.5}$$

The first part of the equation is the linear part and the second is the undesirable nonlinear part. If the movement is reduced by a factor of k so is the third order component reduced by a factor of k^3.

Inter-modulation Noise and Sampling Frequency

The non linearity's of the microphone has another implication than just adding harmonics. The quantization noise will by inter-modulation be folded into the base band. This effect can be evaluated by multiplication of the NTF with the microphones frequency response. The result is the residual quantization noise. By assuming that all of this noise will be folded into the base band one can evaluate the deterioration of the SNR. The residual noise can be seen in Fig. 5.12. The residual noise power can then be found integrating the area under the curve. In the worst case all of the noise power will be folded into the base band. As the residual quantization noise normally is represented as voltage one has to use the voltage to movement function (see equation 5.1) to calculate the residual quantization noise power in the base band. It can be shown that normally the residual quantization noise is not of importance. One should remember that at low frequencies the movement is reduced by feedback and at high frequencies the mechanical roll off of the microphone itself minimizes the movement. All of this reduces deflection and thus non linearity's. The conclusion is that choosing the sampling frequency much larger than the base band will diminish the residual quantization noise. Normally an OSR of 64 to 128 is quite sufficient. But simulations on the actual system will have to be performed.

5.3.3 Stability and Reliability

We will now discuss what implications of using a microphone as a integrator have on stability of the modulator. There are three things that distinguishes the microphone from the ideal integration.

Non Infinite Low Frequency Gain

First there is the non infinite gain at low frequencies. This has the effect that the A_{min} value is lower than expected from the ideal modulator structure. This is due to the fact that the in band suppression of quantization noise is poorer than of the ideal modulator.

Microphone Resonance Peaks

The second is that the microphone peaks at the resonance frequencies. This has only a minor influence on the three stability parameters A_{min}, S_{min} and F_{max}.

Microphone Zeros

As it is seen from Fig. 5.12 the 3^{rd} order ΣΔ modulator has a peak in the NTF. This is due to the fact that the microphone has a zeroes between the resonance peaks. The consequence is that the effective noise suppression at the zero only is equal to that of a single integration. This causes the NTF to peak at the microphone zero. This effect on the three stability criteria is that A_{min} is not affected significantly. As A_{min} is based on the two norm of the impulse response of the NTF, only the largest values of the NTF contributes significantly to A_{min}. The S_{min} and F_{max} is on the contrary

affected as these are one norm based. i.e. the peak of the NTF contributes to S_{min} and F_{max}. We will now summarize the stability parameters of the electromechanical Σ Δ modulator. The modulator is a third order modulator with a NTF cutoff frequency of 0.19.:

Table 5.1: A_{min},S_{min} and F_{max} of an electromechanical Σ Δ modulator and an ideal modulator

Modulator type	A_{min}	S_{min}	F_{max}
Electromechanical Σ Δ modulator	*1.12*	*3.42*	*2.21*
Ideal Σ Δ modulator	*2.41*	*3.23*	*1.87*

We clearly see that the S_{min} and F_{max} values of the electromechanical Σ Δ modulator clearly are to high compared to the A_{min} value.

5.3.4 Overview

By adding a zero in the feedback loop of a electromechanical Σ Δ modulator one achieves the same number of degrees of freedom as for the ideal modulator structure. The electromechanical Σ Δ modulator has though a very poor suppression of in band quantization noise while the S_{min} and F_{max} clearly are to high. Which gives an unreliable modulator. Furthermore the moving of the microphone is not reduced significantly. These drawbacks are the reason why we will now introduce a slightly different approach.

5.4 Electromechanical Digital Feedback

We will now introduce another solution which is nearly identical to the electromechanical Σ Δ modulator. The difference is the design approach. The approach is now to separate the design of the modulator and the feedback. This approach differs from electromechanical Σ Δ modulator by the amount of feedback around the microphone. A similar solution is presented in [36].

5.4.1 Designing Feedback Loop, PID Compensation

In Fig. 5.14 a feedback loop consisting of a microphone, a PID (proportional, integrating and differentiating) compensation and a 1st order Σ Δ modulator is depicted. We will now show how the design of the loop and the Σ Δ modulator can be separated.

Modulator Stability and Reliability

It can be shown that when the gain of the feedback loop with feedback coefficient b_1 is much lower than one at the cutoff frequency of the NTF, then the stability of the following Σ Δ modulator will not be affected. That is , the feedback branch with coefficient b_2 (see Fig. 5.14) should dominate at frequencies close to or above the cutoff

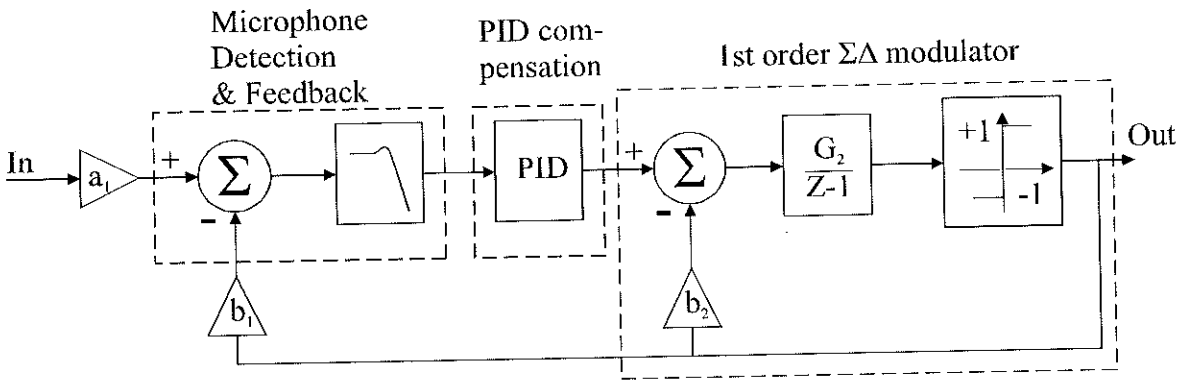

Figure 5.14: Electromechanical feedback with PID compensation plus Σ Δ modulator

of the NTF. When this is fulfilled, then the stability of the Σ Δ modulator will not be deteriorated. And another surprising conclusion: the whole system will also be stable. In fact the cutoff of the NTF can be viewed as a maximum gain bandwidth. And unlike normal feedback theory, the feedback can be extended beyond the resonance frequency of the microphone. In Fig. 5.15 the NTF, STF and the sampled microphone response is shown.

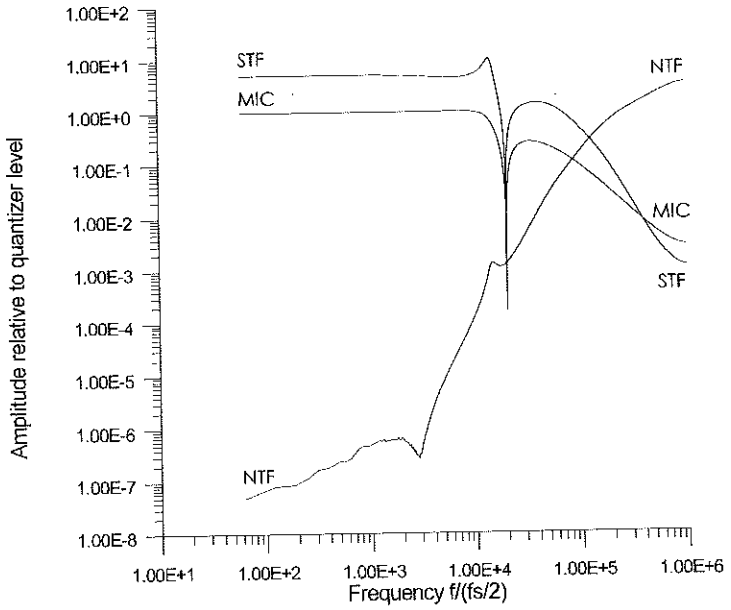

Figure 5.15: NTF, STF and sampled microphone frequency response of an PID compensated feedback loop

The table 5.2 summarizes the stability parameters of the PID compensated digital feedback vs. the ideal Σ Δ modulator. As it is seen this design procedure only has a minor effect on the stability parameters.

Table 5.2: A_{min},S_{min} and F_{max} of a PID compensated digital feedback and an ideal Σ Δ modulator

Modulator type	A_{min}	S_{min}	F_{max}
PID compensated	*2.39*	*3.21*	*1.87*
Ideal Σ Δ modulator	*2.41*	*3.23*	*1.87*

5.4.2 Closed Loop Membrane Deflection and Residual Quantization Noise

As it is seen in Fig. 5.16 the moving of the membrane is greatly reduced in most of the frequency span. At very low frequencies the movement is ideally reduced to zero.

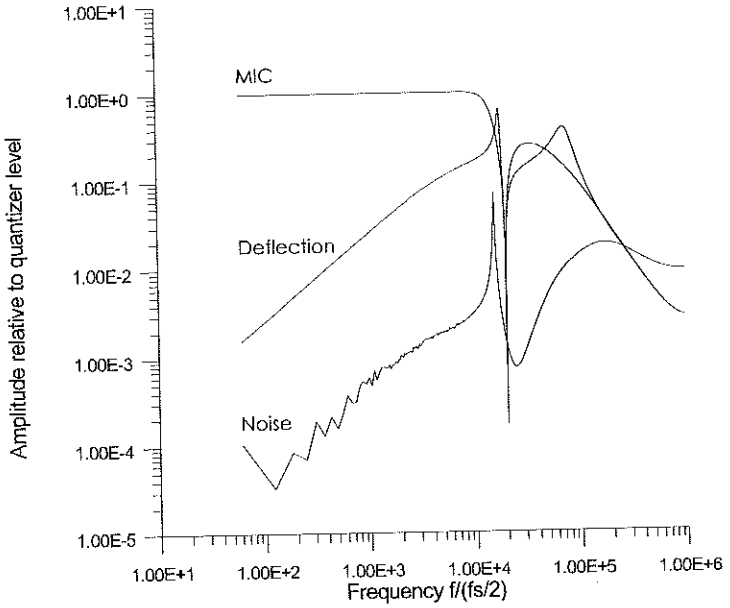

Figure 5.16: Closed loop deflection, residual noise and sampled microphone frequency response of a PID compensated feedback loop

5.4.3 Overview

The basic design concept was in this part to separate the design of the modulator and the feedback loop. It was seen that as long as the gain of the feedback loop around the microphone does not affect the high frequency part of the modulators noise transfer function, then the stability of the whole system will not be affected. This follows from the fact that it is mainly the high frequency components of the NTF which contribute to the stability parameters. I.e. the stability is mainly determined by the high frequency part of the modulator NTF.

5.5 Conclusion

Feedback of electromechanical systems offers many benefits. Linearity, parameter control and direct digital conversion can be mentioned. In this chapter, design of electromechanical digital feedback loops in connection with a capacitive microphone is described. What special features do these offer ? First of all by using a PWM signal feedback with only two voltage levels we have linearized the voltage force function. Secondly the output of the circuitry is a one bit digital signal. And thirdly, the feedback loop reduced the deflection of the membrane, thus increasing linearity dramatically. A very surprising effect of using the high order modulator structure in conjunction with a PID compensation is that the feedback actually can be extended beyond the resonance of the microphone. This is due to the fact that the feedback branches of the modulator dominates the stability of the whole system. This will be true as long as the feedback loop does not affect high frequency part of the modulator. So the combination of a feedback loop and a modulator is very advantageous.

Part II

Applications

Chapter 6

A Low-Noise/Low-Power Preamplifier for Capacitive Microphones

In this chapter a design of a microphone preamplifier for hearing aid applications is presented. The amplifier operates at a power supply voltage of 1v-1.5v. The total current consumption including a bias generator is $40\mu A$. The amplifiers maximum sound level allowed is more than 120 dB SPL (Sound Pressure Level), with a typical noise level of 25 dB(A) SPL[1] (A-weighted). This gives a dynamic range 95dB. The amplifier is optimized for a capacitive microphone with a capacitance of 1.2pF. The amplifier is fully integrated in a $0.7\mu m$ n-well CMOS technology.

6.1 Introduction

Current capacitive microphones for hearing aids use an electret design for the microphone. The principle of the electret microphone is that a permanent charge is captured in a poly-amide layer. A schematic drawing of an electret microphone can be seen in Fig. 6.1.

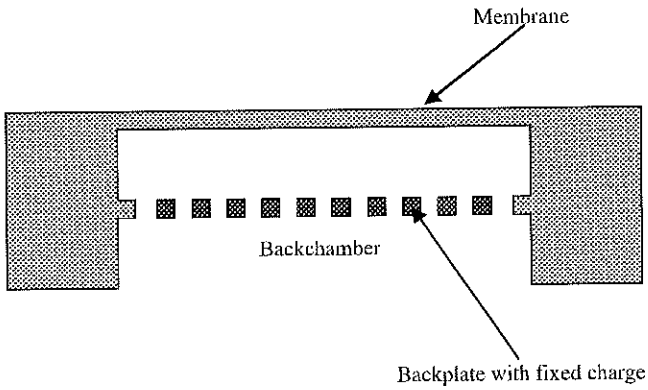

Figure 6.1: Electret microphone (not to scale).

[1]94dB SPL ~ 1Pa

To explain the function of the electret microphone we will first introduce a very simple linear model of the microphone.

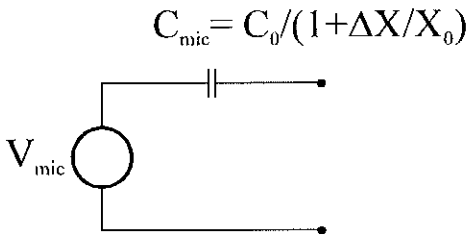

Figure 6.2: Electrical equivalent of an electret microphone

In Fig. 6.2 a model of an electret microphone is introduced. It consists of a capacitance and a voltage source. The capacitance between the membrane and the back-plate is represented by C_{mic}. The voltage source V_{mic} is proportional to incoming sound pressure and the proportionality constant is denoted the sensitivity. The sensitivity is normally in the range of 10mV/Pa -20mV/Pa. Here we will assume a sensitivity of 15mV/Pa. We notice that the voltage across the microphone terminals as a function of the deflection ΔX of the membrane is :

$$V_{mic}(\Delta X) = \frac{Q_0}{C_0} \cdot (1 + \frac{\Delta X}{X_0}) \tag{6.1}$$

Where Q_0, C_0 and X_0 is the permanent charge, quiescent value of microphone capacitor and quiescent value of the distance between membrane and back-plate. We see that keeping the charge on the microphone capacitance constant makes the deflection to voltage function linear with respect to the deflection.

As the electret microphone represent a capacitive source for the preamplifier one will have to optimize the noise performance of the preamplifier keeping that in mind. A capacitive source will always have an associated leakage resistor. This resistor will introduce low pass filtered white noise. The total noise power of a capacitive source will be equal to (see app. C):

$$V_{noise}^2 = \frac{kT}{C_{mic}} \tag{6.2}$$

As the effort at the moment is focused on reducing the size of the microphones then the microphones capacitance value will also be reduced. This means that low noise amplifiers matching low value capacitive sources are needed. At the moment capacitive microphones with C_{mic} of 1pF is the smallest size. In traditional designs, a junction FET in a source follower configuration is used to buffer the signal from the microphone. This can be seen in Fig. 6.3. In consists of the microphone (C_{mic} and V_{mic}) , a very large value bias resistor of $6 Gohm's$, the JFET and a source resistor.

As we saw from 6.2 the noise power is only dependent of the microphone capacitance C_{mic}. But increasing the bias resistor will move the noise power to low frequencies where it is of no importance. This will be discussed later. Due to gate leakage current of the JFET the bias resistor can not be larger than approximately $10 Gohm's$. This is due to the fact that increasing the bias resistor will also alter the bias voltage of the JFET. Other disadvantages of a junction FET source follower are : poor PSRR (Power Supply Rejection Ratio) and low output swing. A JFET amplifier is described

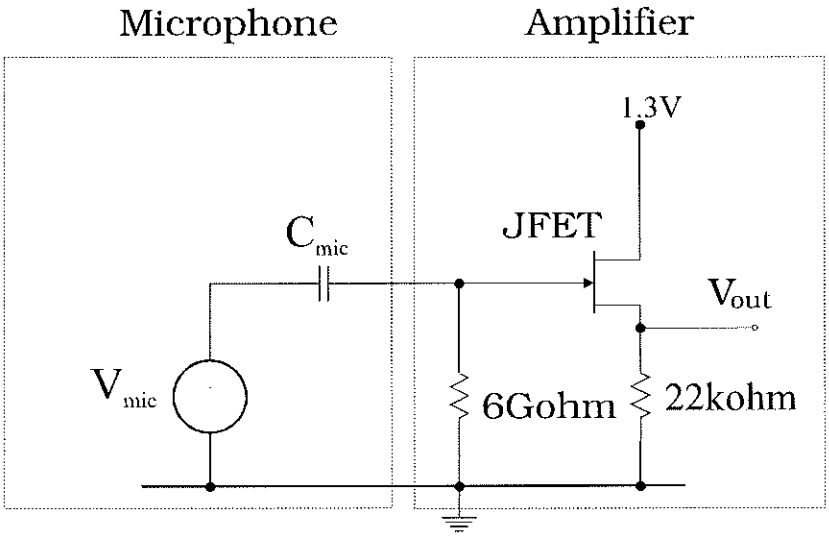

Figure 6.3: Traditional JFET source follower

in [37].

In order to improve the noise performance of the preamplifier, MOSFETS which show a negligible gate leakage current, can be used. We will then show how two zero biased diodes can used as bias resistors with extremely high impedance levels. Furthermore using analog CMOS circuit design principles will allow us to obtain a superior PSRR and full output swing. In [38] a BiCMOS amplifier is described. First we will point out the noise sources of the CMOS amplifier and optimization strategies.

6.2 CMOS Amplifier Noise, Matching a Capacitive Source

Fig. 6.4 shows an equivalent CMOS input stage with all noise sources represented as voltage and current sources. Noise from a CMOS amplifier matching a capacitive source can be divided into three noise sources. The first is the noise from the bias resistor, the second is the thermal white noise from the amplifier and the third is the amplifier low frequency 1/f noise. The latter was in old technologies very dominant at low frequencies. But as it will be shown it is of no importance in today's high performance CMOS technology. The microphone is represented by C_{mic} and V_{mic}, while capacitors C_P, C_f, C_{in} represents parasitic capacitance, feedback capacitance and input capacitance of the input stage.

The spectral noise density $(V/\sqrt{Hz})$of a typical CMOS amplifier can be seen in Fig. 6.5. As it is seen the noise from the bias resistor will dominate at very low frequencies. The slope of this noise will be 20dB/decade. At frequencies above f_{equal} the 1/f noise will dominate with a slope of 10dB/decade. And at frequencies above $f_{noise\ corner}$ the thermal white noise from the input stage will dominate.

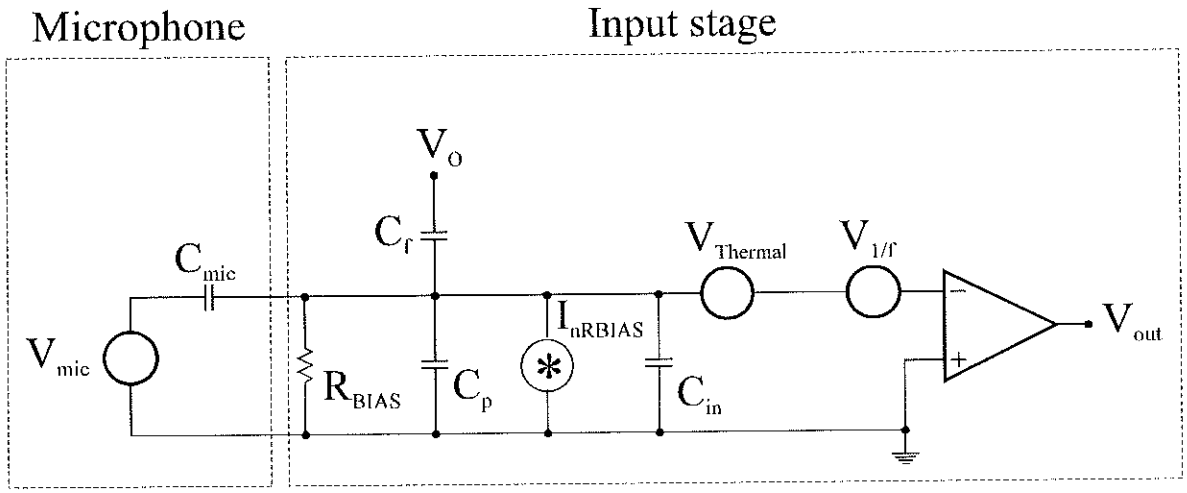

Figure 6.4: Amplifier with noise sources

Now we will calculate the three contributions one by one and show how to optimize for the best signal to noise ratio. This will be done keeping in mind that normally the total noise power is calculated using an A-weighting function. The ear is less sensitive to noise at very high and very low frequencies. On the other hand the ear is very sensitive to noise at frequencies around 1kHz. The A-weighting function is used to take this account. In order to calculate the signal to noise ratio directly we will refer the noise to the input of the amplifier.

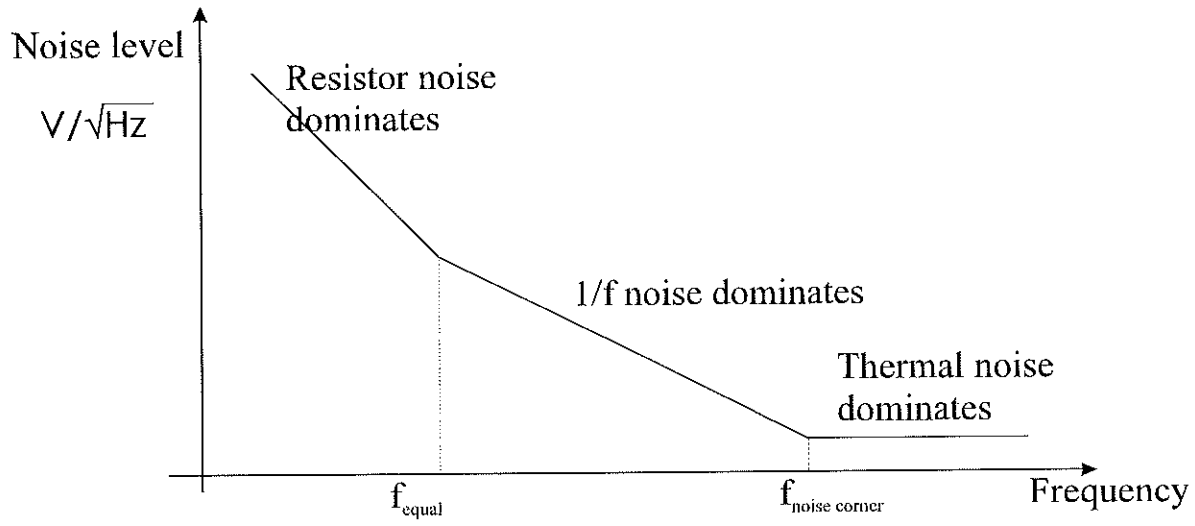

Figure 6.5: Noise, typical spectral density

6.2.1 Bias Resistor Noise

The bias generated thermal noise is in Fig. 6.5 represented as a current noise source. It can be calculated that the noise spectral density of noise coming from the bias resistor

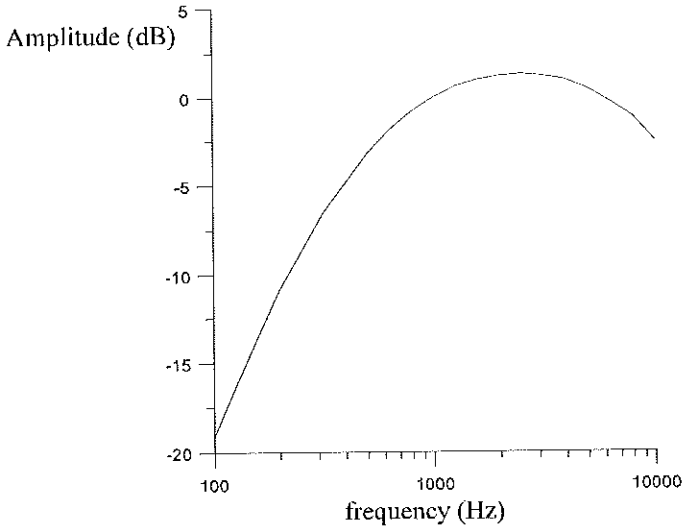

Figure 6.6: The A-weighting function

at the input is :

$$V^2_{RnoiseIn}(f) = \frac{4kTR_{bias} \cdot (C_{mic} + C_f + C_p + C_{in})^2}{1 + (2\pi f R_{bias}(C_{mic} + C_f + C_p + C_{in}))^2} \cdot \frac{1}{C^2_{mic}} \tag{6.3}$$

This can at frequencies above $\frac{1}{2\pi R_{bias}(C_{mic}+C_f+C_p+C_{in})}$ be approximated by :

$$V^2_{RnoiseIn}(f) \simeq \frac{4kT}{R_{bias}} \frac{1}{(2\pi f \cdot C_{mic})^2} \tag{6.4}$$

From this we can see that increasing C_{mic} will reduce the noise spectral density. But normally this is not an option as the microphone capacitance normally is given. Another possibility is to increase the bias resistor R_{bias}. Here it should be noticed that increasing the bias resistor will not decrease the total noise power as this is given by equation 6.2. But it will in fact move the noise power to lower frequencies where it is suppressed by the A-weighting function, se Fig. 6.6.

6.2.2 Input Stage White Noise

When designing amplifiers matching a capacitive source there are two aspects one has two consider. One is the noise of the amplifier. Normally this is minimized designing the input transistor with a very large aspect ratio. The second issue is the capacitive loading of the microphone. Here there is a contradiction. To obtain the smallest noise the input transistors have to have a large aspect ratio, i.e. the input capacitance of the amplifier will be large. Because of the large capacitive loading of the microphone the signal will be damped and the SNR will be deteriorated. This shows that the parameter we want to optimize for is the SNR. At the same time it is obvious that optimal input transistor dimensions must exist given the largest possible SNR.

In this sub-section we will first give equations for input capacitance, white noise and transconductance of CMOS input stages. Then we will calculate the optimal aspect

ratio $\frac{W}{L}$. This will be calculated for strong inversion operation only, but in appendix D all inversion regimes are treated.

It is a well known fact that thermal white noise of a CMOS transistor in strong inversion equals :

$$I^2_{noisedrain}(f) = 4kT\frac{2}{3}K_P\frac{W}{L}(V_{gs} - V_T) \tag{6.5}$$

At the same time the input capacitance of the input stage is :

$$C_{in} = \frac{2}{3a}WLC_{ox}\alpha \tag{6.6}$$

Where $\alpha = 1 + \frac{3L_d}{2L}(1 + a)$ and a equals 2 for a differential stage and 1 for source follower and common source stage. The input capacitance C_{in} accounts for gate source capacitance and overlap capacitance's. If one wishes to take gate bulk capacitance into account then α can be modified to $\alpha = 1 + \frac{3L_d}{2L}(1 + a) + \frac{n-1}{2n} \cdot a$.

From this and Fig. 6.4 the input referred equivalent noise can be calculated as :

$$V^2_{noiseequitherm}(f) = 4kT\frac{2a}{3}\frac{L}{\sqrt{2I_DK_PWL}}(1 + \frac{2}{3}\frac{WLC_{ox}\alpha + \frac{3a}{2}(C_p + C_f)}{aC_{source}})^2 \tag{6.7}$$

At is seen a optimum exists. This comes from the fact that increasing the aspect ratio will lower the noise but also increase the gate area and thus the damping of the signal due to capacitive loading. The optimum is located at :

$$WL = a\frac{C_{mic}}{2C_{ox}\alpha} \tag{6.8}$$

Or it can be interpreted as :

$$C_{in} = \frac{a}{3} \cdot (C_p + C_f + C_{mic}) \tag{6.9}$$

And the value associated with the minimum is :

$$V^2_{noiseequitherm}(f) = 4kT\frac{2a}{3}\frac{L}{\sqrt{aI_dK_P}}\sqrt{\frac{C_{ox}\alpha}{C_p + C_f + C_{mic}}}(\frac{4}{3}\frac{C_{mic} + C_p + C_f}{C_{mic}})^2 \tag{6.10}$$

So the channel length should be as small as possible. This indicates that a small line width technology should be used. As we see a differential stage is twice as noisy , considering the thermal noise, as a single transistor stage.

6.2.3 Input Stage Low Frequency 1/f Noise

For 1/f noise there also exits optimal input transistor dimensions. In this subsection we will first give equations for input capacitance, 1/f noise and transconductance of CMOS input stages. Then we will calculate the optimal aspect ratio $\frac{W}{L}$. Also here we will only do the calculations for strong inversion operation. In appendix D all inversion regimes are treated.

It is a well known fact that low frequency 1/f noise of a CMOS transistor in strong inversion equals :

$$I^2_{noisedrain1/f}(f) = \frac{1}{f}\frac{K_f \cdot I^{AF}_{drain}}{L^2 C_{ox}} \tag{6.11}$$

From this and Fig. 6.4 the input referred equivalent noise can be calculated as :

$$V^2_{noiseequi1/f}(f) = \frac{a}{2}\frac{1}{f}\frac{K_f}{K_p W L C_{ox}}(1 + \frac{2}{3}\frac{WLC_{ox}\alpha + \frac{3a}{2}(C_p + C_f)}{aC_{mic}})^2 \tag{6.12}$$

Where $\alpha = 1 + \frac{3L_d}{2L}(1 + a)$ and a equals 2 for a differential stage and 1 for source follower and common source stage. Here α can also be modified to take the gate bulk capacitance into account. Again an optimum exists. This comes from the fact that increasing the aspect ratio will lower the noise but also increase the gate area and thus the damping of the signal due to capacitive loading. The optimum is located at :

$$WL = a\frac{3}{2}\frac{C_p + C_f + C_{mic}}{C_{ox}\alpha} \tag{6.13}$$

Or it can be interpreted as :

$$C_{in} = (C_p + C_f + C_{mic}) \tag{6.14}$$

And the value associated with the minimum is :

$$V^2_{noiseequi1/f}(f) = \frac{4}{3}\frac{1}{f}\frac{K_f \alpha}{K_p}\frac{(C_{mic} + C_p + C_f)}{C^2_{mic}} \tag{6.15}$$

As it is seen the minimal 1/f noise of a given technology only depends on $\frac{K_f \alpha}{K_p}$ and the capacitance values. This indicates that a technology with a very thin oxide should be used. Further more it is seen that a differential stage is equal as noisy as a both source follower and a common source stage.

6.2.4 Total Optimization of Input Stage Noise

As we have seen there exists two optimal input stage designs [39]. These corresponds to the situations where 1/f noise or channel white noise is dominating. In this design the input stage was designed to achieve minimum 1/f noise. If both 1/f noise and channel white noise has to be considered then optimization using SPICE has to be performed. One has to be aware that an accurate model level has to be used. One solution is to use the EKV (Enz-Krummenacher- Vitoz) MOST model [40]. In appendix D white noise and 1/f noise is treated in all inversion regimes.

6.2.5 Minimization of Total Noise

The total noise from the amplifier consist of contributions from the input transistors and from all other transistors. Having minimized noise from input transistor one should

assure that contributions from all other transistors are negligible to those of the input transistors. This is easily done, keeping in mind, that the transconductance g_m of the input transistors should be larger than all other transistors. If we assume strong inversion operation then the white noise of each transistor is :

$$I^2_{white\ noise} = \frac{W}{L} \cdot K_p \cdot V^2_{dsat} \tag{6.16}$$

Where V_{dsat} is the saturation voltage of the transistor. So we see that it is a weighting between low noise and low voltage operation. Furthermore all other transistors should be longer than the input transistors gate lengths. This comes from the fact that the low frequency 1/f noise is inverse proportional to the gate length.

6.3 Amplifier Topology

As the amplifier is intended to operate at a power supply voltage of only 1-1.5V this puts some restrictions on the chosen amplifier topology. In chapter three low voltage design techniques are treated. To achieve the largest possible dynamic range it is necessary that both the amplifier generated noise power is low and at the same time that the maximal signal swing at the output is as large as possible. This can be achieved by setting the DC level of the output is in the middle of the supply rail. This implies that the DC level of the high impedance node and the output must be set independently. We will in the following show how.

6.3.1 Biasing of Input Stage

We have seen that the bias resistor noise is minimal when the resistor value is as large as possible. Normally the bias resistor is in the G ohm's range. The only way of implementing high impedance resistors in a standard CMOS technology is to use well diodes. The small signal impedance of a zero voltage biased diode is [41] :

$$R_{diode} = \frac{V_t}{I_{DSS}} \tag{6.17}$$

Where the leakage current is I_{DSS}. For a minimum diode of the technology used it is 10fA, which gives us a resistance value of 1.3T ohm. This is indeed a large value. The well diode has one disadvantage. They are always accompanied by a parasitic well-substrate diode. This is seen in Fig. 6.7. If the technology used has the option of both n-doped and p-doped poly then fully floating diodes can be implemented.

In this design a standard CMOS technology was used.

6.3.2 Setting the DC Level of the Output Stage

Traditionally bias resistor from input to output is used to set the DC level of the output stage. This can be seen in Fig. 6.8. But this is not an optimal solution. The DC level of the high impedance node and the output can not be set independently and furthermore the signal on the output of the amplifier will be seen directly by the diode.

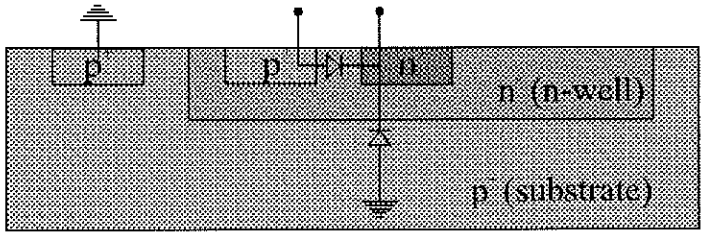

Figure 6.7: Well diode schematic and implementation

This will limit the voltage swing on the output and introduce severe non linearity. This comes from the fact that the diode has a non linear current voltage characteristic. Furthermore, the high impedance node is the interface node to the chip, it has to be protected by protection diodes. This in fact sets a limit to how small we can design the diode, i.e.it sets a lower limit of the achievable noise level. The diode has to be relatively low impedance compared to the protection diodes.

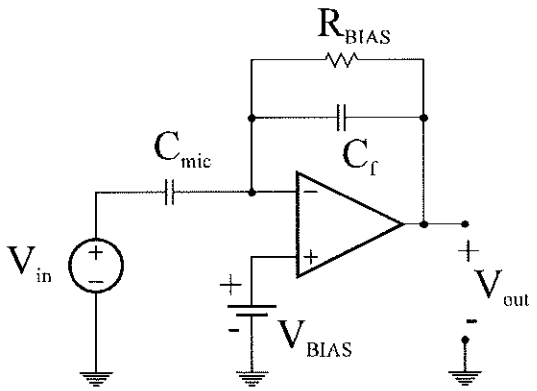

Figure 6.8: Capacitive amplifier with traditional biasing

To eliminate these problems we will use the protection diodes as biasing to the first stage also. So the protection diodes now have two functions, protection and biasing. This can be seen in Fig. 6.9. In this scheme the protection diodes set the DC level and the AC level across them is virtually zero, because of the feedback loop. To set the DC level of the output we have used a DC servo feedback. The output is divided by a factor of 10 and compared to a reference voltage. Effectively the AC voltage across the well diode is only 1/10 of the output voltage. This enhances linearity. The drawback of this scheme is that it is more complex and it can not operate on very low power supply voltages. This is seen noticing that the output of A_2 only can function if the DC level is 100mV above ground.

A simpler solution that does not have these drawbacks is a differential difference amplifier (DDA) [42] [43]. This can be seen in Fig. 6.10. This consists of a charge amplifier and a DC servo feedback. One of the amplifiers of Fig. 6.9, amplifier A_2 has been replaced by a differential input. This extra differential input can be implemented using only 3 transistors. Furthermore the inputs of the upper differential input can be biased at a DC level equal to Gnd. Therefore this circuitry is able to operate at very

low supply voltage.

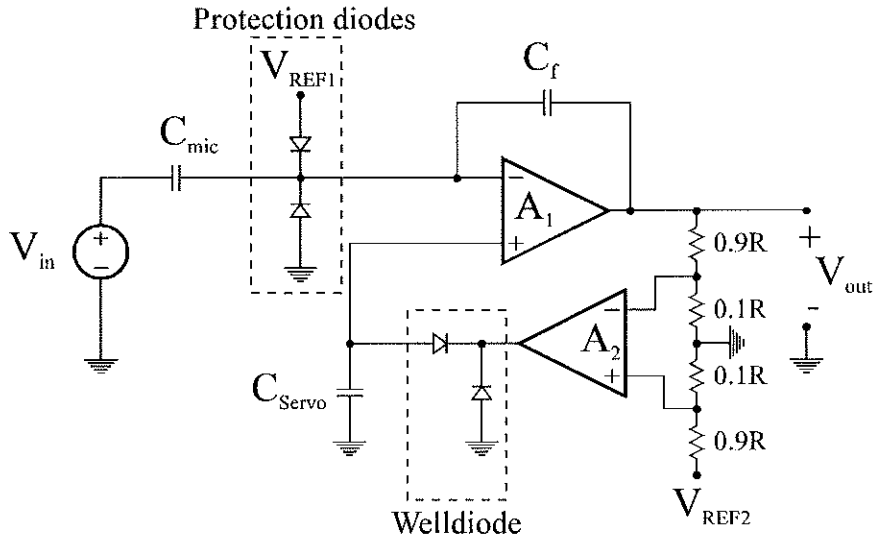

Figure 6.9: Capacitive amplifier with servo feedback

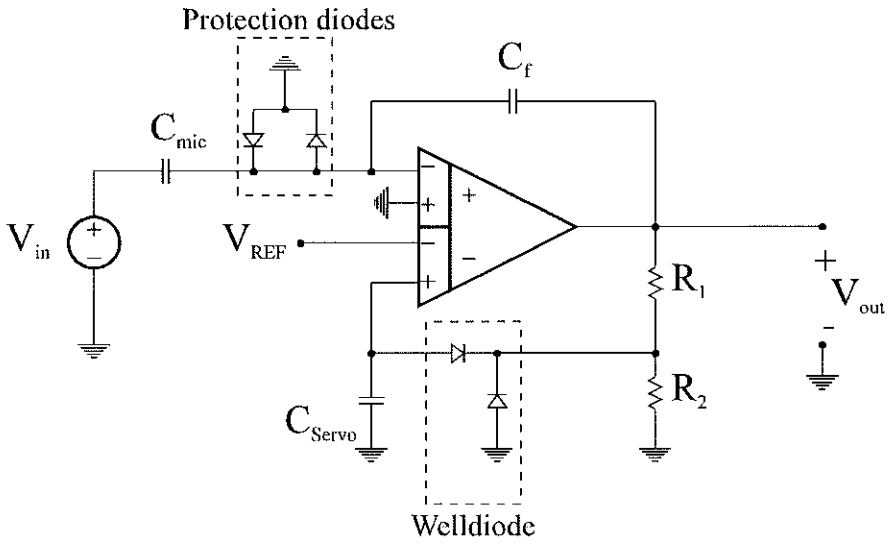

Figure 6.10: Differential difference amplifier

We will now explain the differential difference amplifier (DDA). A block diagram of the DDA is showed in Fig. 6.11. The upper input stage of Fig. 6.10 is denoted diff1 and the lower diff2. These are actually g_m stages so they are easily summed.

Below the unity gain frequency of the DDA the transfer function from V_{mic} to V_o is calculated to :

$$A_{mic}(S) = \frac{V_{out}}{V_{mic}} = -\frac{C_{mic}}{C_f}\frac{1}{1+\eta}\frac{S}{S+\omega_o\frac{\eta}{1+\eta}} \tag{6.18}$$

And from V_{REF} to V_{out} :

$$A_{REFout}(S) = \frac{V_{out}}{V_{REF}} = (1+\frac{R_2}{R_1})\frac{\eta(S)}{1+\eta(S)}\frac{S+\omega_o}{S+\omega_o\frac{\eta(S)}{1+\eta(S)}} \tag{6.19}$$

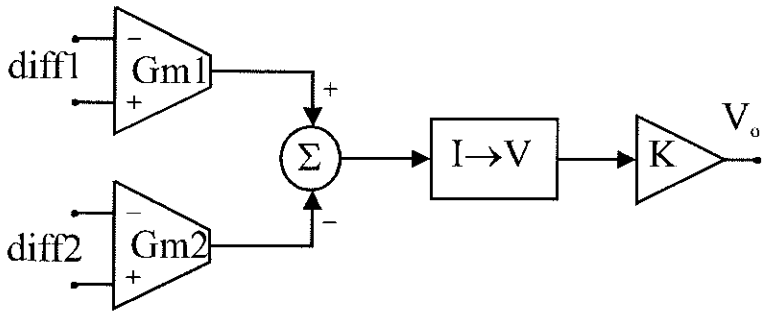

Figure 6.11: Differential difference amplifier

Where

$$\omega_o = \frac{2}{R_{diode}(C_{mic} + C_p + C_f)} \tag{6.20}$$

and

$$\eta(S) = \frac{1 + \frac{C_{mic}}{C_f}}{1 + \frac{R_2}{R_1}} \frac{Gm2}{Gm1} \frac{1}{1 + \frac{S}{\omega_2}} \tag{6.21}$$

We see that it is desirable if $\eta \ll 1$. Then $A_{in}(s)$ equals the gain of a charge amplifier. And the gain $A_{ref}(s)$, will be very small above ω_o. $\eta \ll 1$ can be obtained by $C_{mic}/C_f \ll R_2/R_1$ and Gm2 $\ll$ Gm1.

6.4 Implementation

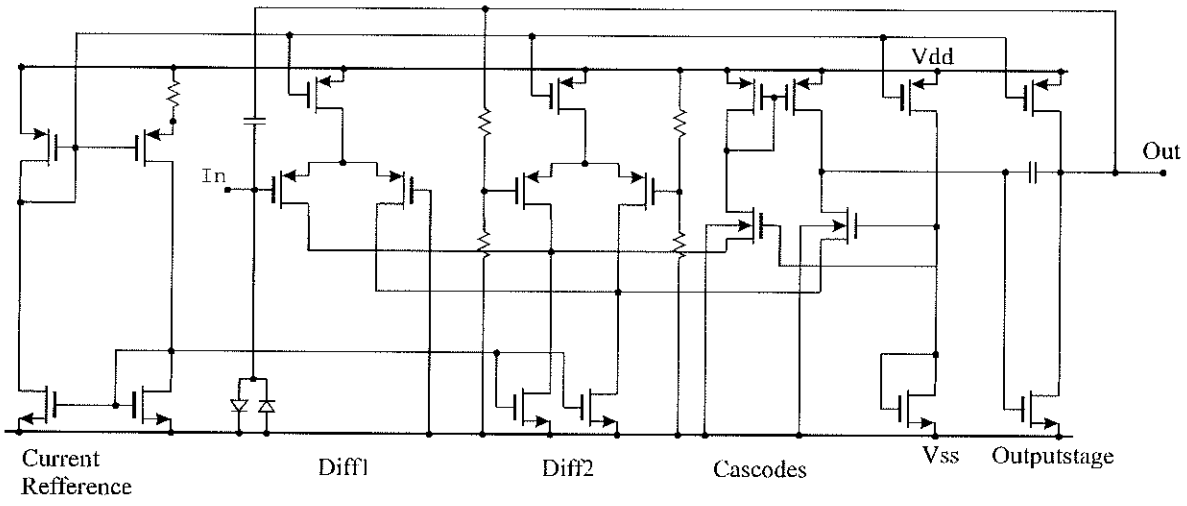

Figure 6.12: Schematic of total amplifier

The schematic of the amplifier is shown in Fig. 6.12. It consists of 5 sections. A current reference [8], input stage (Diff1), bias input stage (Diff2), folded cascode and last a single transistor output stage. This configuration has been chosen because of its ability to operate at very low voltages. The current reference is a standard current reference with the two PMOS transistors operating in weak inversion [8]. Input stage Diff1 is

operated at a larger current than Diff2. This is to reduce noise and assure a total gain close to C_f/C_{mic}. The cascodes are operated close to V_{ss}. This is to assure that Diff1 can handle voltages as low as V_{ss} on its input. Output stage is a single transistor biased by a current generator and miller compensated by a capacitor. Bias input stage (Diff2) is connected to V_{dd} and Out. Resistors are chosen in such a way that the bias voltage at the output always is $V_{dd}/2$. Last, the input is biased by two diodes of minimum size. This is two assure the best SNR possible. These diodes serve as ESD protection diodes also, but as they are very small the protection is not very efficient. The implemented version is not implemented as a charge amplifier with a servo feedback. This will though be implemented in the next version. A microphotograph of the amplifier can be seen in Fig. 6.13.

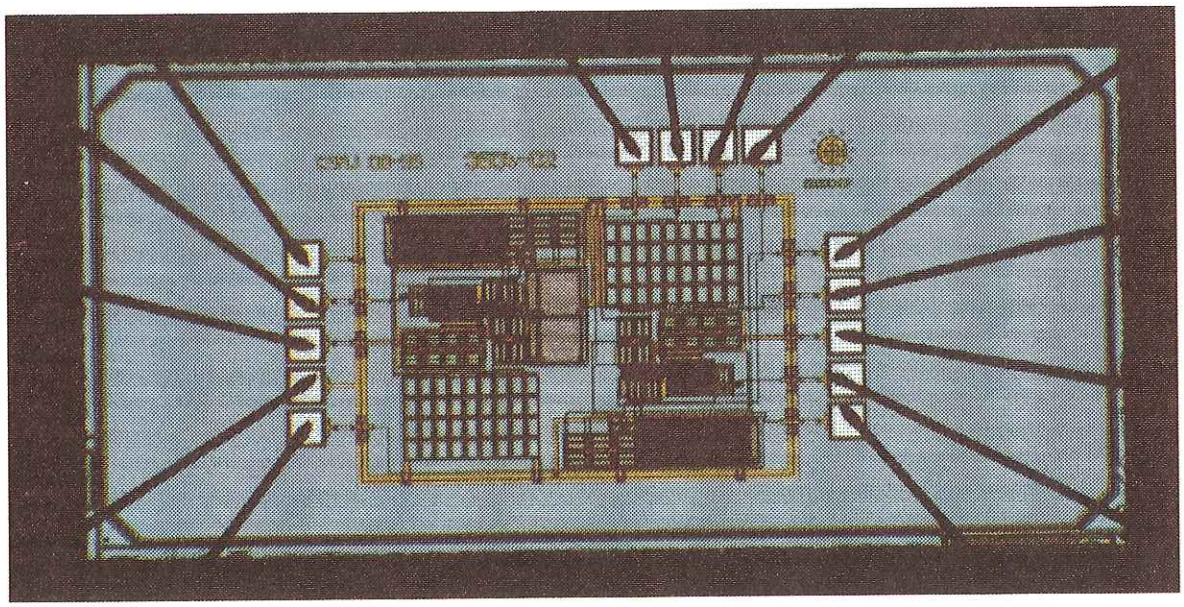

Figure 6.13: Microphotograph of amplifier

6.5 Experimental Results and Simulations

The amplifier has been integrated with a 1.2pF capacitance simulating the microphone capacitance.

6.5.1 Static Measurements and Simulations

It has been verified that the amplifier can operate at a supply voltage of 1V-1.5V. The current drain was simulated to $30\mu A$ and measured to $36\mu A$ -$40\mu A$ (10 samples). The measured output swing is approx. $0.5V_P$ at a supply voltage of 1.5V. This corresponds to a maximum input sound level of more than 120 dB SPL (sensitivity of 15mV/Pa).

6.5.2 Dynamic Measurements and Simulations

In this section we will compare simulation results and measurements. We will point out some problems with the existing design and solutions to these problems.

Overloading

During the test of the amplifier it was noticed that when the amplifier was overloaded it saturated and returned to normal operation very slowly. This saturated state may last for several minutes. The pulse overloading the amplifier was introduced via the power supply from a solder iron switching on and off. When totally shielded and battery driven this could not be observed. So is this likely to occur ? Normally the output from a microphone does not contain high frequency pulses with large amplitudes. But it is known that dropping the microphone on the floor can give pulses in the range of 50-100V. This will most certainly saturate the amplifier.
So what happens when the amplifier saturates ? It can be explained as follows. When the amplifier is saturated, the high impedance node at the input is charged. The diodes will now discharge the node. In the beginning this discharging is fast but as zero voltage is approached then the only current discharging the node, is the leakage current of the bias diodes. And this current is very small. Because of the large DC gain A_{DC} (approximately 300 times) then the effective time constant of the amplifier is :

$$\tau = A_{DC} \cdot R_{diode} \cdot (C_f + C_p + C_{mic} + C_{in}) = A_{DC} \cdot \frac{V_t}{I_{DSS}} \cdot (C_f + C_p + C_{mic}) \quad (6.22)$$

In this design this was equal to $300 \cdot 1.3T\Omega \cdot (0.38pF + 1.2pF + 0.2pF + 1.78pF) = 390sec.$ This is in fact a time constant of 6min and 30 sec !!! Normally this situation never occurs because the voltage across the diodes is virtually zero. But when the amplifier is overloaded then it cannot assure that there is zero voltage across the diodes.

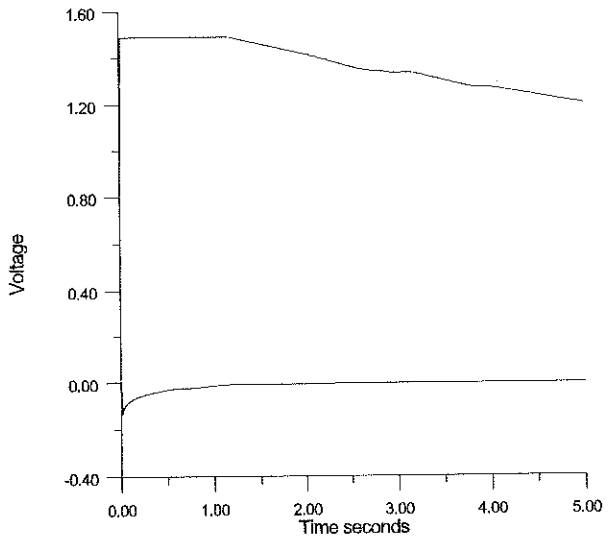

Figure 6.14: Overload response of implemented solution. Voltage across diodes and output voltage.

There are two solutions to this problem :

Lower the DC gain from the high impedance node to the output and/or detect whether the amplifier is saturated and then force the high impedance to ground with a switch. In Fig. 6.14, Fig. 6.15 and Fig. 6.16 are shown the output of the amplifier when overloaded by a pulse with amplitude of 1V and a rise time of 100nSec is showed. The three plots show the implemented solution, one with low DC gain and one with a switch that forces the amplifier to settle quickly.

As we see the two solutions are both very effective. The one with the switch resetting the amplifier is though the most effective. This solution needs a detection circuitry. Both the high impedance node and the amplifier output can be used to detect saturation. We will now explain the three Fig. 6.14 to Fig. 6.16.

In Fig. 6.14 we see the output of the implemented solution and the voltage over the bias diodes, when the amplifier has been exposed to an overloading pulse. It is seen that the amplifier returns very slowly to its bias conditions. It was measured that the amplifier settled within 10 to 15 minutes. This is of course far to slow.

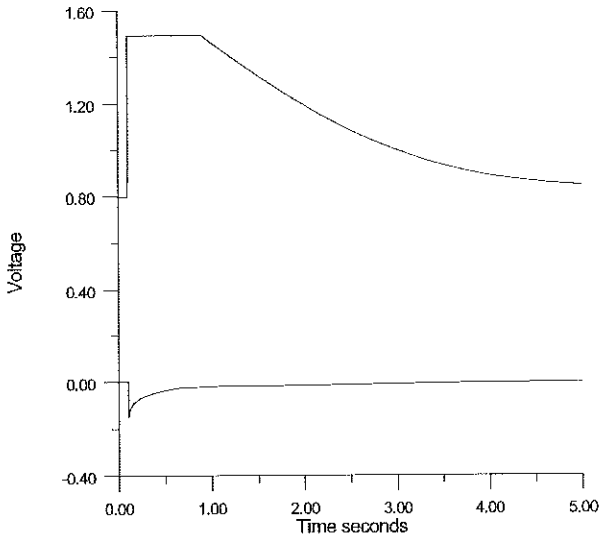

Figure 6.15: Overload response of solution with low DC gain from high impedant node to output

The second Fig. 6.15 shows the amplifier but with a lower DC gain from voltage over the diodes to the output. It is seen how the amplifier returns within 5 -10 seconds.

The third Fig. 6.16 shows the implemented amplifier exposed to a pulse that saturates it two times. The first time a switch resets the amplifier and it is seen that the amplifier returns almost instantaneously. After the second pulse the amplifier is left to return to equilibrium itself. As it can be seen this is very slowly. To detect when to reset the amplifier one needs a circuitry that detects if the amplifier has been overloaded. This can be done both on the high impedance node and on the output of the amplifier. Detecting on the output a time lag is needed. This is not necessary when detecting on the voltage across the bias diodes.

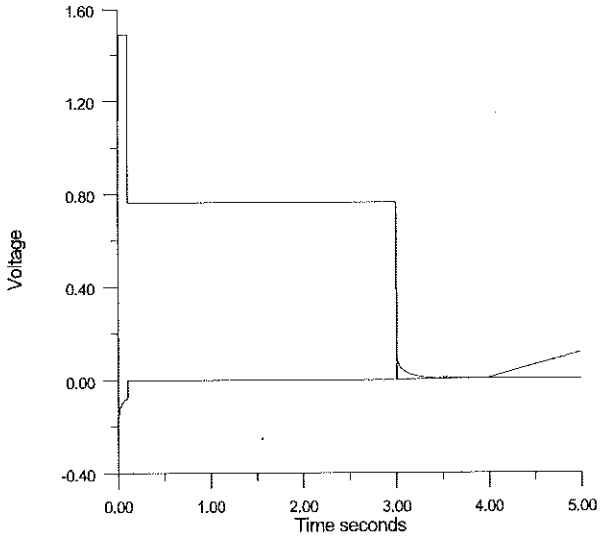

Figure 6.16: Overload response of solution with reset switch

Frequency Response and PSSR

Gain has been measured to 2.96 ~ 9.42dB @ 1kHz. This was simulated to 3.03 ~ 9.63dB @ 1kHz. Fig. 6.17 shows the measured gain A_{mic} as a function of the frequency. The peak located at 300kHz is due to capacitive loading of 100pF(cables).

Noise

Fig. 6.18 shows the simulated and the measured noise at the output of the amplifier. This is worth a notice. The white noise level is approx. 6dB higher than simulated. Some of the transistors are biased in moderate inversion and as SPICE level 2 and level 3 overestimates the transconductance in this area, this might explain some of the difference between measurements and simulation. Simulation has to be done using the EKV MOST model [40] or the BSIM3v3 model. This has not yet been done as these models are yet not an integrated feature of PSPICE. The low frequency noise is much lower than expected. This is quite surprising. The noise corner is situated at a very low frequency (approx. 40Hz). This is though, only based on measurements from 10 samples of a single run. One might expect that this varies from batch to batch. But the simulated noise-corner was approx. 400Hz so the 1/f noise performance was much better than expected. The total noise level was simulated to 24B(A) SPL. And it was measured to 25dB(A).The frequency range was 100Hz to 10Khz. As the amplifier was designed to operate on a supply voltage of 1.0V and the V_{T0} of the PMOS transistors was 0.9V this means that the noise level can be decreased if a technology with a lower threshold voltage is used.

6.6 Conclusion

A preamplifier optimized for capacitive microphones with a very low source capacitance has been presented. It utilizes a new design. A DDA is used to amplify the signal from the microphone. Expressions for optimal gate area concerning noise are given. The

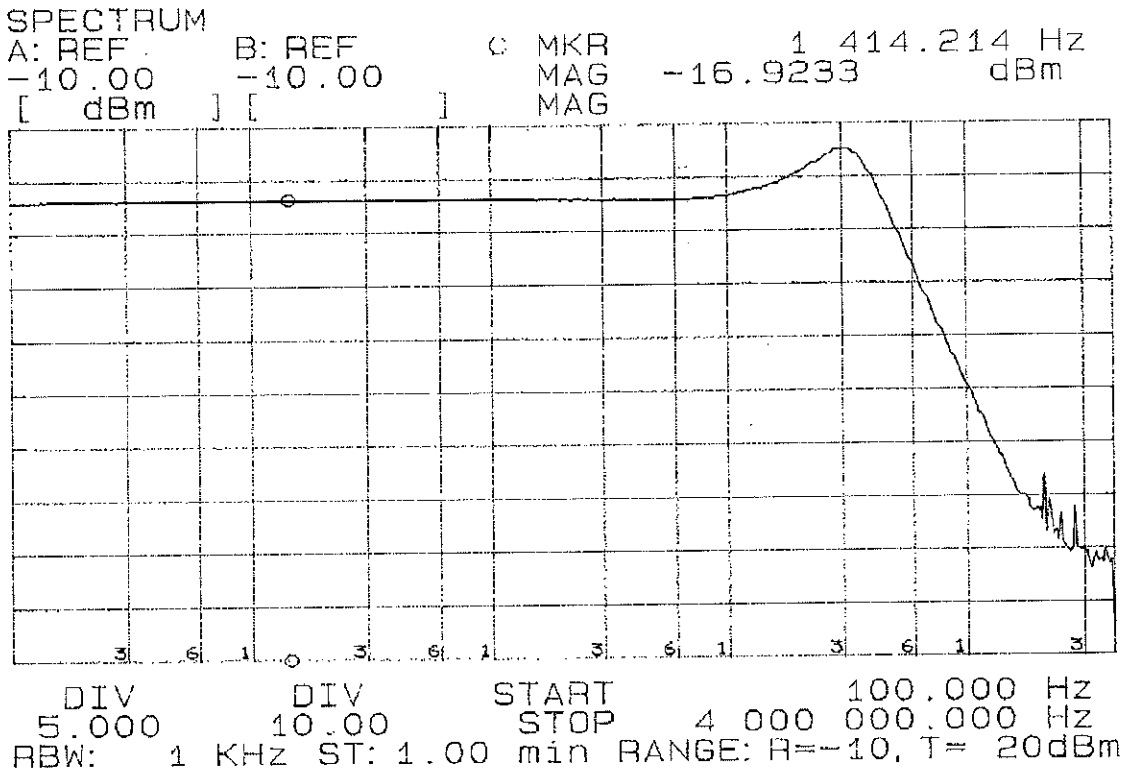

Figure 6.17: Measured gain as a function of frequency. Frequency : 100Hz to 4MegHz. 5dB/div. Gain = 9.42dB @ 1khz.

preamplifier is implemented in a CMOS $0.7\mu m$ technology. Noise measurements differ from the simulations. White noise is larger and low frequency noise is smaller. This is due to the inadequate model levels used in PSPICE. The total measured noise level is equivalent to 25dB(A) SPL. This compared with the maximum sound level allowed of more than 120 dB SPL gives us a dynamic range of 95dB at a supply voltage of 1.5V.

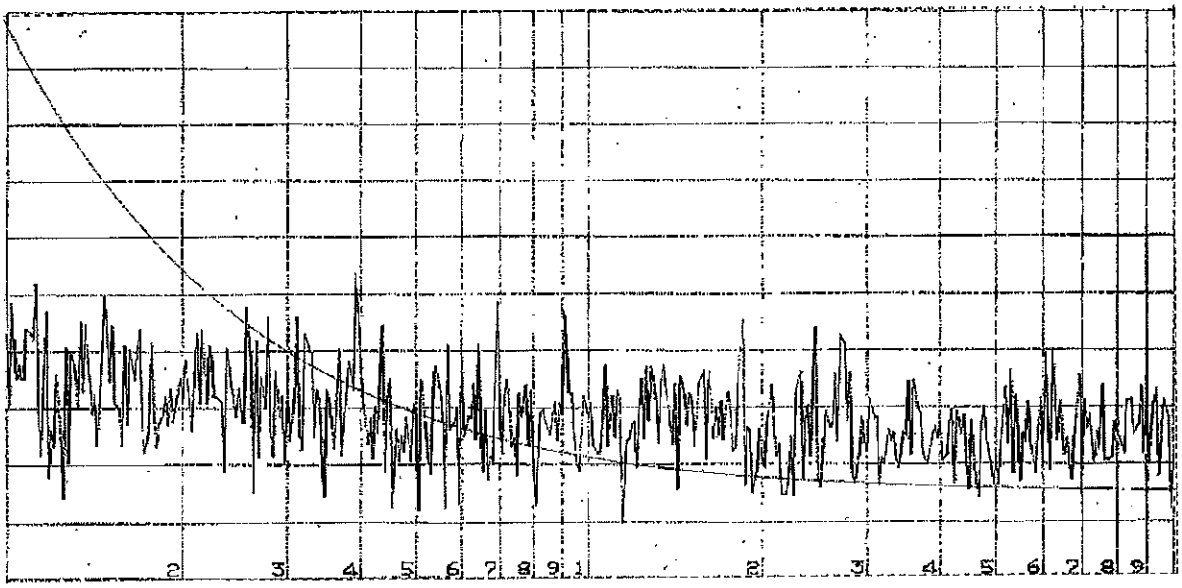

Figure 6.18: Measured vs. simulated noise. Frequency: 100Hz to 10kHz. Scale : 0nv to 800nv(Rms)

Chapter 7

A High Resolution SC 1bit $\Sigma\Delta$ Modulator for Low Voltage Low Power Applications

In this chapter a 3^{rd} order $\Sigma\Delta$ modulator for low power low voltage applications is presented. It was intended to be part of a digital force feedback loop with a microphone, as described in chapter five. However the modulator can be used in stand alone applications as well.
The modulator has been implemented in a 0.7μm n-well CMOS technology. The maximum resolution is 87dB equivalent to 14 bits of resolution. This is achieved with a signal-band of 5kHz, over-sampling ratio (OSR) of 128 and a sampling frequency of 1.28MHz.
The modulator operates at two supply voltages. The analog part is operated at a supply of 1-1.5V, while the digital part and switches is operated at a supply of 3v. This is to achieve lowest power consumption without degrading the performance. As the total current drain is $100\mu A$ then the total power consumption is approximately 150 μ watts. Examples of low power 1bit $\Sigma\Delta$ modulators can be found in [44] and [45]. The very low power consumption is achieved by using of efficient class AB amplifiers in a fully differential configuration utilizing capacitive common mode feedback.

7.1 Introduction

Why are $\Sigma\Delta$ converters so suited for low voltage low power operation ?
First of all the anti aliasing is moved to the digital domain. As seen from chapter one high performance signal processing is best performed in the digital domain when the question is low power consumption [1] [26]. Secondly multi bit quantization is replaced by 1 bit noise shaped conversion [22]. This is actually the main reason why $\Sigma\Delta$ converters have achieved so much attention during the last years. As the quantizer is only one bit it is inherently linear. i.e. no matching is required. Besides from this, the one bit quantizer is very easy to implement at low voltages. It can be implemented as a comparator and some few switches. In this design it is implemented as a comparator, a voltage reference and some few switches. First we will discuss the modulator topology.

7.2 Modulator Topology

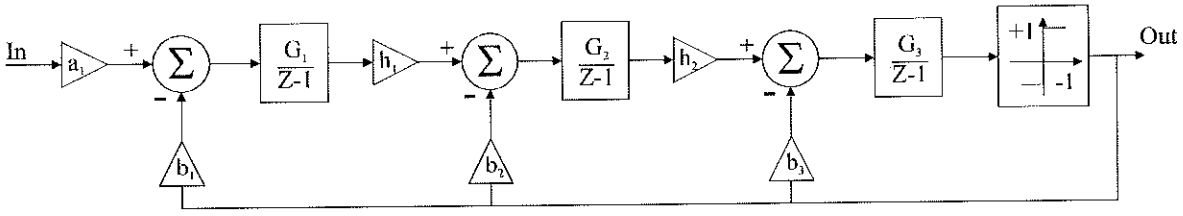

Figure 7.1: Implemented ΣΔ modulator topology

The implemented modulator type is a third order with multiple feedback [22]. It can be seen in Fig. 7.1. It consists of 3 integrators and a quantizer.
When one wants to design a modulator then the first step is to select a suitable NTF, as described in chapter four[22]. Here a Butterworth high pass filter-function has been chosen as this has proven to produce a very reliable modulator [22]. The term "reliable" is discussed in chapter four[22]. Next the cutoff of the filter-function has to be chosen. In this case it has been chosen from a maximum dynamic range criteria [22]. This gives a cutoff frequency of 0.19 relatively to f_s. A better choice when designing low power converters would have been 0.15, But at the moment at which the design was initiated, this was not recognized. The next step is to scale so that the first term of the NTF impulse response equals one. This is to assure causality, i.e. to assure that the modulator can be implemented [22] [28]. In all of this the linear gain of the quantizer has been set to one. This is true as the quantizer is invariant to scaling. The last step is to now to scale the coefficients so that the maximal internal signal swing is fully exploited at signal level equal to MSA. The MSA of a Butterworth NTF with cutoff frequency of 0.19 relatively to f_s is 0.45.

The signal swings of the unscaled modulator can be seen in figures Fig. 7.2 to Fig. 7.4. It is seen that the signal swings are 0.5 , 1.5 and 2.0 on the output of the first, second and third integrator respectively. The NTF coefficients have then been scaled so that internal signal swings are 1.0 at an input level equal to MSA. It is interesting to note that the shape of the amplitude distribution of the output of the third integrator is clearly Gaussian shaped. This was actually the assumption when the Gaussian stability criterion was developed. In this design extra scaling coefficients h_1 and h_2 were introduced. The reason why these were introduced will appear later. In figure Fig. 7.2 a simulation of the ideal implemented topology is shown. It is seen that the quantization noise is clearly shaped. The low signal can also be seen. The coefficients are summarized in table. 7.1.

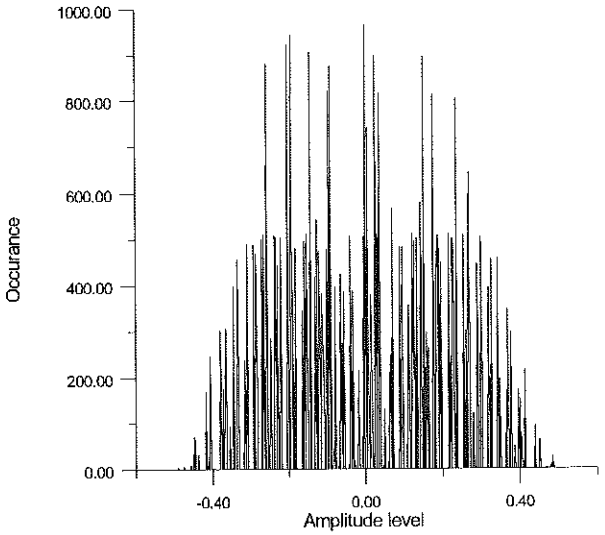

Figure 7.2: Amplitude distribution at output of first integrator

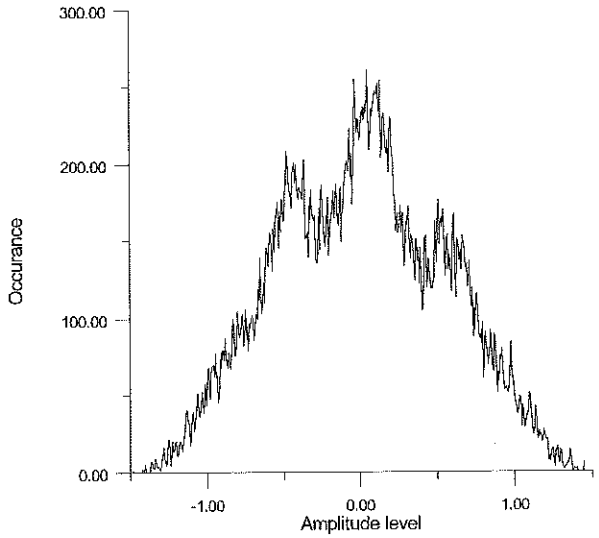

Figure 7.3: Amplitude distribution at output of second integrator

7.3 Switched Capacitor Implementation of Modulator

In this section we will deal with the transistor implementation of the modulator. The main building blocks are, integrators, comparator and a voltage reference. Besides from these there are : clock-generator, voltage doubler / tripler and a digital finite state machine (FSM). The secondary building blocks will not be dealt with in details. In Fig. 7.6 is pictured an overall schematic. And in Fig. 7.7 the non overlapping clock phases 1 and 2 are shown. We will now describe the overall function and design criteria's and then detailed discuss each block.

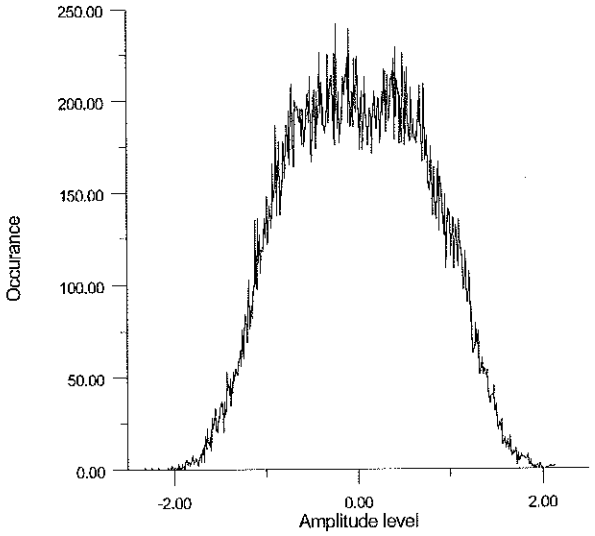

Figure 7.4: Amplitude distribution at output of third integrator

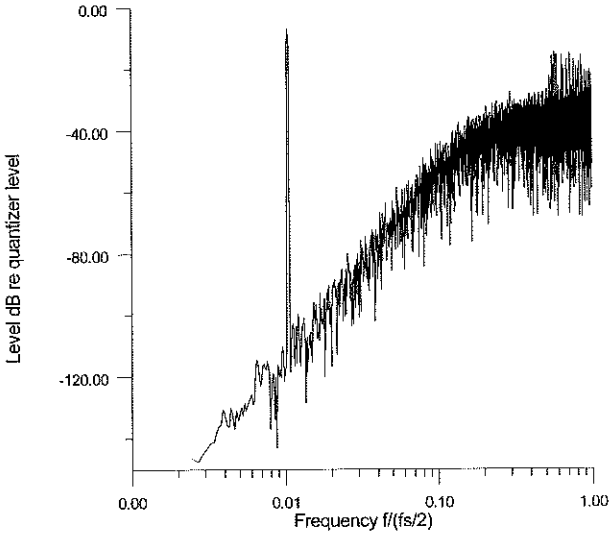

Figure 7.5: Output spectrum of the implemented 3^{rd} order modulator

7.3.1 Overall Design

The modulator has been implemented as a fully differential circuit. Apart from the obvious advantages as larger dynamic range, cancellation of charge injection and so on, the choice of amplifier type has been the major reason for choosing a differential solution. This will be shown later. The implementation is shown in Fig. 7.6. As the modulator is operated on a single supply the 1 bit D/A conversion can only achieve values Gnd and V_{ref}. So a digital control block has been added. This controls the switching of the feedback capacitances. If a feedback of $-V_{ref}$ is needed the feedback capacitance is switched to $-V_{ref}$ during phase 1 and then switched to Gnd during phase 2. If a feedback of V_{ref} is needed then the order is just the opposite. Delays of Z^{-1} have been introduced to realize the topology of Fig. 7.6. Furthermore, comparator plus digital control has a delay of Z^{-1}. The delays are implemented as analog delays but they could easily had been implemented as digital delays after the 1 bit quantization

Table 7.1: Coefficients of implemented Σ Δ modulator

a_1	b_1	b_2	b_3	G_1	G_2	G_3	h_1	h_2
1	*1*	*0.302*	*0.1965*	*0.254*	*1.333*	*3*	*0.25*	*0.25*

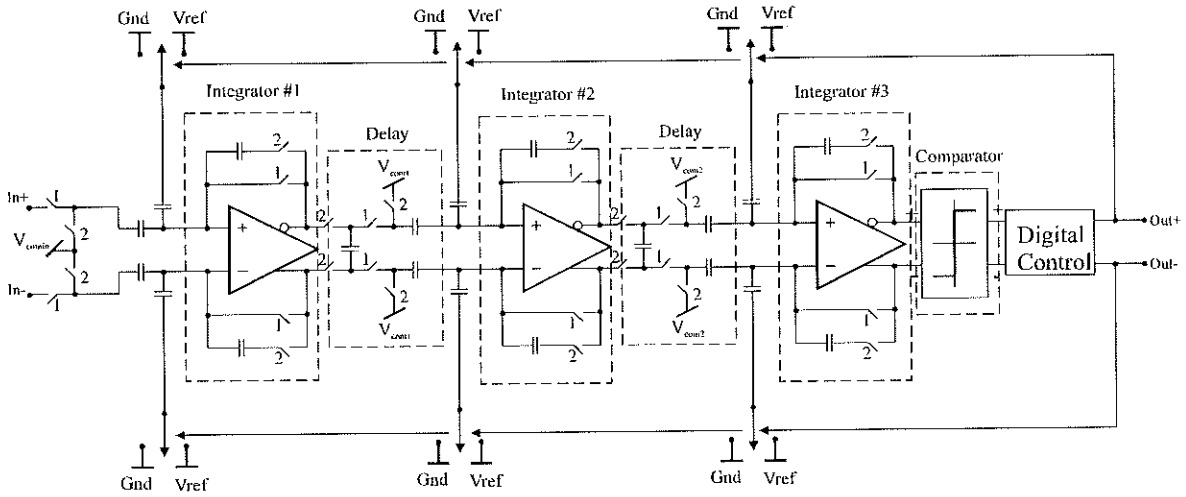

Figure 7.6: Implemented ΣΔ modulator topology

using very few digital blocks. This was though not recognized at the moment that the modulator was implemented.

Supply Voltage Optimization

The circuitry is operated on two different supply voltages [26]. The reason for this is that power efficient multiplication of the supply voltage requires an external coil. This was not desirable. So the power consuming parts of the circuitry was operated on 1.5V while the less power consuming circuitry parts was operated on the high voltage 3V - 5V. These are the digital circuitry parts and the switches. Especially the switches need a clock signal somewhat larger than the supply voltage in order to achieve sufficiently low on resistance. This comes from the fact that the on resistance of the switches are equal to :

$$R_{on} \simeq \frac{1}{\frac{W}{L} \cdot K_p \cdot (V_{gs} - V_T)} \tag{7.1}$$

So if we want to process signal with voltage levels close to V_{DD} then the clock signal should have an amplitude larger than $V_{DD} + V_T$.

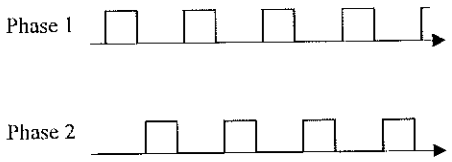

Figure 7.7: Clock phases of the ΣΔ modulator

Minimizing Total Power Consumption

Besides from designing the NTF for minimum power consumption and using supply voltage optimization there are other possibilities for minimizing the power consumption.
As only noise from the first integrator plus the reference voltage is of importance, integrator 2 and 3 noise can be sacrificed. This comes from fact that noise from integrators 2 and 3 are exposed to a high pass filter function at the output of the modulator, as described in chapter four (it can be seen by calculating the filter function from an internal node to the output of the modulator). In this design the capacitances of the second and third integrator were halved. It is actually the minimum capacitance value that sets the maximum power sawing, i.e. as long as the capacitances can be scaled, to obtain the wanted modulator coefficients, then power can be saved.
It is of great importance that the first integrator and the reference voltage is low noise and suppress disturbances from the power supply. Any disturbances from these two blocks, e.g. noise or power supply noise will be added at the same level as the signal. This has the consequence that the major part of the power consumption will be the power consumption of these two blocks.
The digital part of the modulator does not consume any power of significance.

7.3.2 Amplifiers

The first priority of the modulator is ultra low power consumption. Because of this, it is important that the amplifiers used to implement the integrators, use a minimum of static current to settle within the available time slot. In ΣΔ modulators the feedback coefficient of the amplifiers/integrators is commonly close to one. This can also be interpreted as the feedback capacitance C_f of Fig. 7.8 being much larger than the signal capacitance C_s. As seen from chapter two single stage amplifiers are much more efficient than multi stage amplifiers under these conditions, or as stated by Eric Vittoz [8] :" Therefore any compensation capacitor other than the load itself should be avoided ". This implies that the amplifier type used, should be single stage OTA's. In 7.8. such a configuration is shown. In the configuration of 7.8, correlated double sampling (CDS) has been added by using a reset phase (phase 1) and a amplification phase (phase 2). The two phases are non-overlapping, with duty cycle of 50%. The clock phases can be seen in Fig. 7.7. The drawback of this clocking scheme is that the amplifier only is available during phase 2. Settling in the two phases is solely determined by the transconductance of the OTA and the surrounding capacitive network. We will assume that the amplifier is class AB without slew rate limitations. The C_S , C_P , C_f and C_{load} are gain , parasitic , integration and load capacitance.

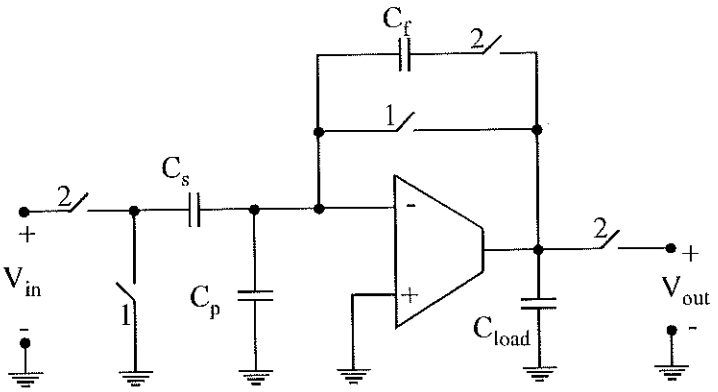

Figure 7.8: Implemented ΣΔ modulator topology

Amplifier Settling

We will now calculate the settling time during phase 1 and 2 and the bias current needed. During phase 1, the time needed for settling Ts within an error band d is :

$$T_{S1} = \frac{C_s + C_p + C_{load}}{g_m} \cdot ln(\frac{1}{d}) \tag{7.2}$$

And for phase 2 :

$$T_{S2} = \frac{C_{leff}}{g_m} \cdot ln(\frac{1 + \frac{C_f}{C_{leff}}}{d}) \tag{7.3}$$

Where C_{leff} equals $C_s + C_p + (C_f + C_s + C_p) \cdot \frac{C_{load}}{C_f}$.

These equations are deducted in app. B.

Current Consumption

Normally one chooses the capacitance values from noise specification. And from this one sees that T_s depends solely on the transconductance g_m of the OTA. So it is important that the g_m is as large as possible for a given bias current. As seen from chapter two an inverter with transistors operating in weak inversion is the optimum choice. This amplifier type has the largest transconductance, lowest noise resistance and it is inherently a class A/B circuit. The minimum bias current I_{bias} for an inverter is in phase 1 :

$$I_{bias1} = \frac{n \cdot V_t}{2 \cdot T_s} \cdot (C_s + C_p + C_{load}) \cdot ln(\frac{1}{d}) \tag{7.4}$$

And for phase 2 :

$$T_{bias2} = \frac{n \cdot V_t}{2 \cdot T_s} \cdot C_{leff} \cdot ln(\frac{1 + \frac{C_f}{C_{leff}}}{d}) \tag{7.5}$$

Where $n \cdot V_t$ is the weak inversion slope factor and V_t equals 26mV.

7.3.3 The Switched Inverter

In order to achieve the largest possible g_m for a given current the amplifier has been implemented as a switched inverter [8], see Fig. 7.9. The switching scheme resembles the one of Fig. 7.7. All transistors are operated in weak inversion for maximum $\frac{g_m}{I_{bias}}$. In order to enlarge the low frequency gain, cascode transistors M2 and M3 has been added. The operation is as follows. During phase 1 the amplifier is biased and is not connected to the input signal. Transistor M5 biases the inverter during the biasing phase. Phase 2 is the amplification phase where it is connected as the amplifier of Fig. 7.8. Furthermore, an extra biasing capacitance has been added. The capacitor C_{fbias} sets the quiescent voltage level at the output. I.e. the value that the signal swings around. This is optimally set to $\frac{V_{DD}}{2}$. Unfortunately this capacitance also limits the low frequency gain of the amplifier if it is operated as an integrator as the one of Fig. 7.9.

As C_f is much larger than all other capacitors one sees from equations 7.4 and 7.5 that the bias current needed is approximately the same in phase 1 and 2. The switched inverter amplifier has the ability to operate at voltages just above the CMOS threshold voltage. As the switched inverter is a class AB circuit it has no slew rate limitations. The switched inverter is described in [21], [16] and [8].

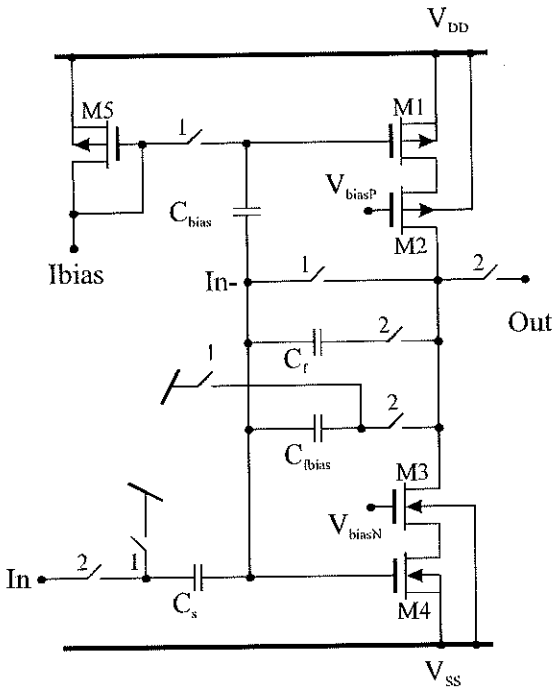

Figure 7.9: Switched inverter amplifier

7.3.4 Switched Inverter Amplifier Noise

In sampled analogue systems the white noise from switches and amplifiers is under-sampled and all of the available noise power is folded within -fs/2 and +fs/2. Low frequency 1/f noise from transistors is not considered a problem as this is removed by CDS. Furthermore, noise from switches is generally of minor importance compared to

amplifier noise [16]. During phase 1 the noise is sampled onto capacitors Cs and Cp. In the following phase this noise is amplified to the output. The input referred noise contribution of phase 1 is :

$$V_{n1}^2 = \gamma \cdot \frac{kT}{C_s} \cdot \frac{(C_s + C_p + \frac{C_f \cdot C_{load}}{C_f + C_{load}})^2}{C_s \cdot (C_s + C_p)} \tag{7.6}$$

Where γ, k and T is n/2 (in case of a switched inverter amplifier), Boltzmans constant and temperature in Kelvin. In order to calculate the noise in the base band one has to divide by OSR. During phase 2 the equivalent input referred white noise has the rms. value of :

$$V_{n2}^2 = V_{n1}^2 \cdot \frac{C_s + C_p}{C_{leff}} \tag{7.7}$$

Again one has to divide by OSR. In our case C_f is much larger than all of the other capacitors. So the two contributions are approximately equal. The theory of sampled noise is described in [46], [47] and [8]. Noise of the switched inverter is described in [16].

7.3.5 Integrators

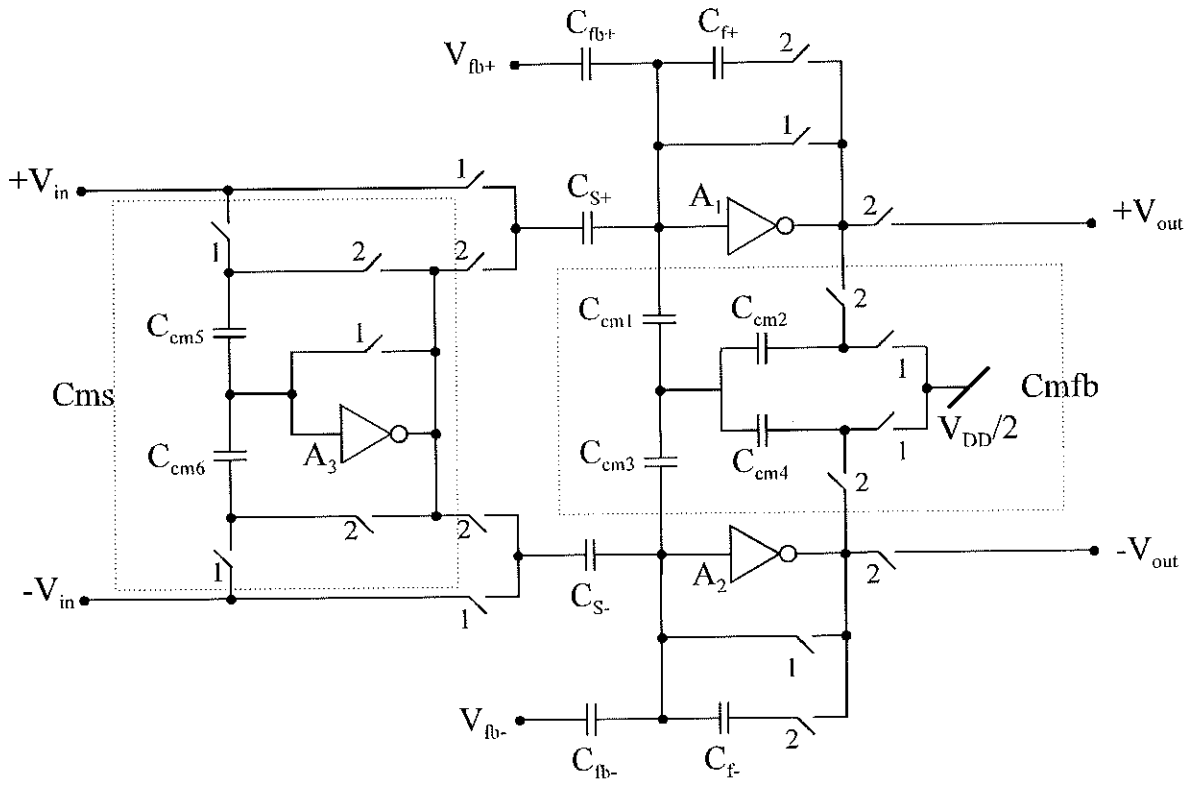

Figure 7.10: Differential switched inverter amplifier

The largest problem associated with the switched inverter amplifier is the poor high frequency power supply rejection ratio PSRR. As the source of M1 is directly connected to V_{DD} the PSSR is only 6dB, referring to Fig. 7.9. CDS enhances the PSSR at low frequencies but unfortunately it also submerges frequency components around fs/2 into the base band. A solution to this problem is to implement integrators as pseudo differential amplifiers with common mode feedback. Principle schematic of the integrators is showed in Fig. 7.10. Switching phases resembles the ones of Fig. 7.7. In Fig. 7.10 amplifiers A_1-A_3 are replaced by the core of the switched inverter of Fig. 7.9 The differential switched inverter consists of three blocks. A block which performs cancellation of the common mode part of the input signal is named Cms. The block that implements the common mode feedback of the integrator is named Cmfb. The remaining parts are two switched inverters. These are implemented as the one of Fig. 7.9. We will know explain the operation of the differential switched inverter and the separate blocks.

Cmfb

The differential switched inverter is implemented with two inverters in a pseudo differential coupling with common mode feedback. The common mode feedback is implemented with the block named Cmfb. It consists of four switched capacitors. For differential input signals the pseudo differential switched inverter of Fig. 7.10 is an integrator with a gain of $\frac{C_{s+}}{C_{f+}}$. For common mode signals the circuit acts as a lossy integrator with low frequency gain of $C_{s+} \cdot (\frac{1}{C_{m1}} + \frac{1}{C_{m1}})$. As the maximal suppression ultimately is determined by matching of components then the two half parts of the integrator should match. C_{gain1} should match C_{gain2} and so on. As noise from the power supply is a common mode signal, it will be removed completely, in case of complete matching.
In Fig. 7.10 the common mode level of the integrator is also set by Cmfb to $V_{DD}/2$. In case of complete matching this will not affect the differential integration. This feature has not been implemented on chip.

CmS

To further reduce the amplification of common mode signals the block named Cms is introduced. It performs a sampling of the common mode part of the input signal. On phase 1 the input signal, differential and common mode part is sampled on the two capacitors C_{cm5} and C_{cm6}. And on phase 2 only the common mode part is present at the output of A_3. As the input capacitors C_{S+} and C_{S-} is connected to the input signal at phase 1 and to the common mode part of the input signal at phase 2 then the input capacitors C_{S+} and C_{S-} is only charged with the differential part of the input signal.
As noise from the block Cms is common mode then it is ideally left out. Cms does not attenuate common mode disturbances introduced via the power supply. These are only suppressed by the Cmfb block.

Choice of Capacitance Values and Bias Currents

We will know discuss how to design the blocks of the $\Sigma\Delta$ modulator and how to design for a given signal to noise ratio with minimum power consumption. i.e. minimum bias current. The capacitances used to realize coefficients a1 and b1 is chosen to 4 pF. This gives us a total calculated integrated white noise from integrator 1 and voltage reference of approx. 10mV RMS.

The bias current needed for integrator 1 and the voltage reference is 25μA and 50μA respectively. This assures that the first integrator and the voltage reference can settle within 0.39μ sec. This corresponds to the width of phase 1 and phase 2 where they are logic "high". The bias current requirements for integrator 2 and 3 are more relaxed as the noise from these are of minor importance. Therefore values of the capacitances in integrator 2 and 3 can be chosen smaller without affecting noise performance. Bias currents are set to 12.5μA in both.

7.3.6 Comparator Design

The comparator is a design originally proposed by Krummenacher [26]. It implements the well known latched comparator, using switched inverters instead of the standard type inverters. This has the advantage that the minimum supply voltage is lowered to just above the CMOS threshold voltage. The switching scheme resembles the one of Fig. 7.7.

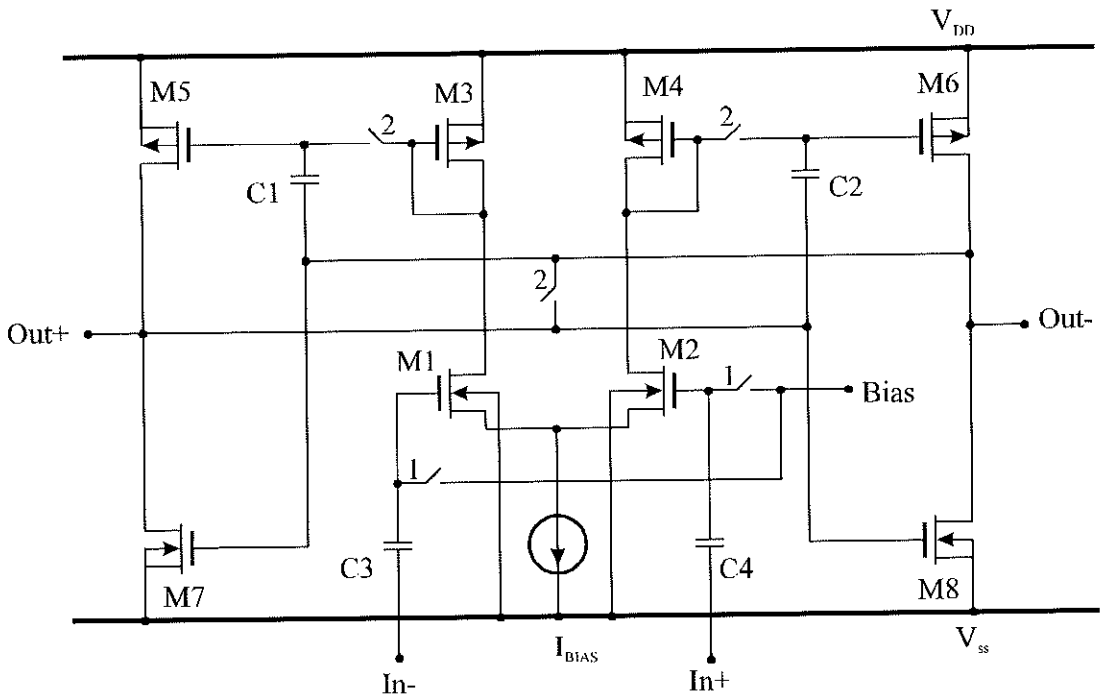

Figure 7.11: Low voltage latched comparator

During phase 1 the common mode voltage of the input of the differential pair is set (M1 and M2). During phase 2 the signal is applied and the comparator is reset. In this phase an imbalance in the comparator is introduced. The current in one of

the switched inverters is larger than in the other. When the comparator is released in phase 1 and the switches opens, then the comparator flips to one of the sides.

7.3.7 Voltage Reference

As the noise from the voltage reference is sampled directly at the input of the first integrator it is important that it is low noise , see chapter four. The reference voltage will contribute with both white noise and low frequency 1/f noise. In the integrators the low frequency 1/f noise is removed by correlated double sampling. This technique can not be used in the voltage reference, because this would remove the reference itself. A lateral parasitic bipolar transistor [48] has been utilized in a diode coupling biased by a current mirror. This solution was chosen for its simplicity, fast settling and good PSSR. A class A/B solution was also tested but it was either too slow or had bad PSSR.

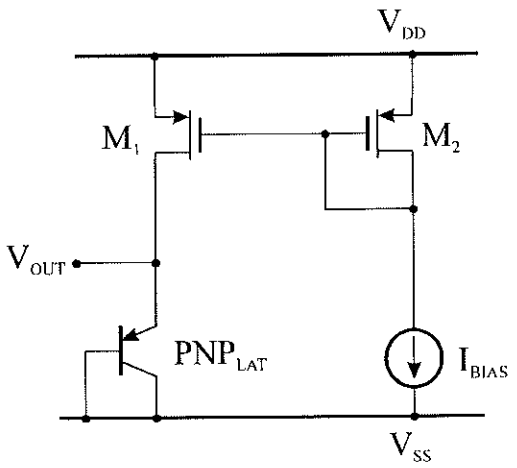

Figure 7.12: Voltage reference utilizing parasitic bipolar transistor

7.3.8 Clock Generator, Voltage Doubler, Level Shifter and Finite State Machine

The last blocks are the two phase non overlapping clock generator, a voltage doubler, a level shifter and a finite state machine. These are seen in Fig. 7.13 to 7.16. The clock generator is a standard two phase clock generator, see [49].

The finite state machine assures that the feedback can subtract or add charge to the integrators, depending on the sign of the output of the comparator. If charge has to be added then the feedback capacitance is switched from Gnd to V_{bias} going from phase one to phase two.

Due to the fact that the circuitry is powered on two different supply voltages then a level shifting function has to be added. It has been taken from [26] and it is a dynamic level shifter. It interfaces logic level high of 1.5v and 3v.

The voltage doubler is implemented with two capacitors and some few switches. At phase one capacitor C_1 is charged to V_{DD}. And on phase two the charge is shared with capacitor C_2. As C_1 in phase two is connected to both V_{DD} and C_2 then C_2

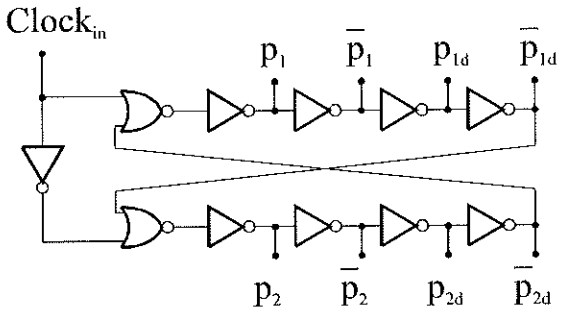

Figure 7.13: Two phase non overlapping clock generator

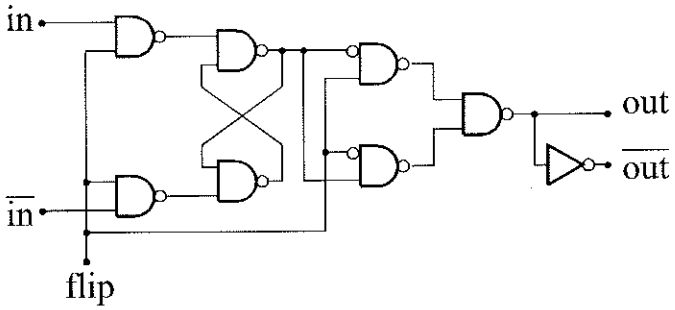

Figure 7.14: Finite state machine

will gradually be charged to a voltage equal to $2 \cdot V_{DD}$. If no external components are allowed then the efficiency of this circuitry will be low. But as the total current drawn from the voltage doubler is small then the total power consumption is nearly not affected. This has not been implemented on chip.

7.4 Simulation Results

Below, in 7.2 is summarized the simulated specifications for the modulator. The simulation results are obtained by simulating the analog circuitry in SPICE and the ideal modulator structure using MATLAB. The noise of the analogue circuitry is simulated using ac analysis in SPICE. In this way the total input referred noise power can be estimated. The noise power in the base band can then be found by dividing by OSR. The result can be seen in table 1. In practice the noise tends be to be higher than expected. This way of evaluating the noise performance do not take the canceling of 1/f noise into account. Also second order effects such as charge injection, coupling of noise through the substrate, PSSR, non-infinite amplifier gain and non-linear settling are not considered is these simulations of table 1. They are either too time consuming, can not be modeled in SPICE or are in this design very dependent on matching. A transient analysis in SPICE has been used to assure that the circuitry implemented corresponds to the modulator topology of Fig. 7.1. Such a simulation does not give any clue of what the SNR of the modulator might be. This is because the transient analysis in SPICE does not take noise from switches and transistors into account. All second order effects tend to increase the noise. Much attention has been offered in the design and layout phase in order to minimize these extra noise sources.
The modulator has been simulated in PSPICE to verify the overall functionality. This

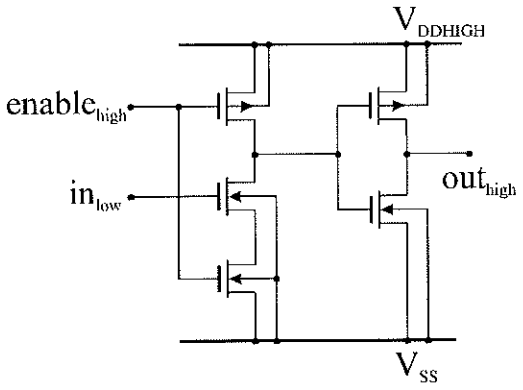

Figure 7.15: Dynamic level shifter

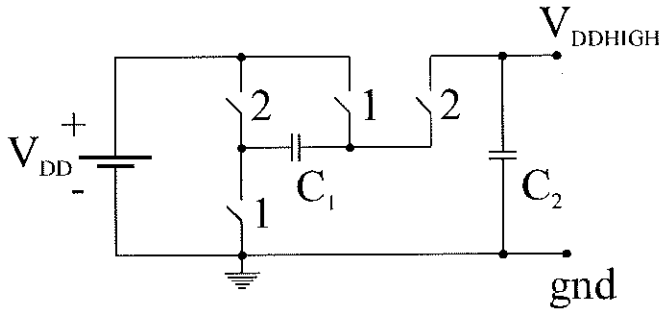

Figure 7.16: Voltage doubler

can be seen in Fig. 7.17. Here the differential bit stream, together with the differential input signal is shown. This clearly shows that the modulator performs a coding of the input signal.

7.5 Measurements

The chip has been realized. It was verified that the DC levels of bias transistors was correct, according to simulations, but the expected functionality could not be verified. In Fig. 7.18 a measurement showing the spectrum of the bit stream when the modulator is processing a sine wave is presented. It is seen that the modulator shapes the quantizer noise, but it is not shaped as expected. It is not clear at the moment what part of the circuitry that does not function correctly.

7.6 Conclusion

A 3^{rd} order switched capacitor Σ Δ modulator is presented. Overall chip size is 3.3mm versus 3.3mm. The modulator has been designed to have a maximum SNR of 87dB with a signal bandwidth of 5 kHz. The over sampling ratio is 128. The noise transfer-function is a Butterworth high pass filter. Design procedure for finding the modulator coefficients are given. Furthermore a new fully differential switched amplifier design is presented. The very low power consumption achieved is due to this very efficient type of amplifier and the design strategy presented in this paper. Analytical expression

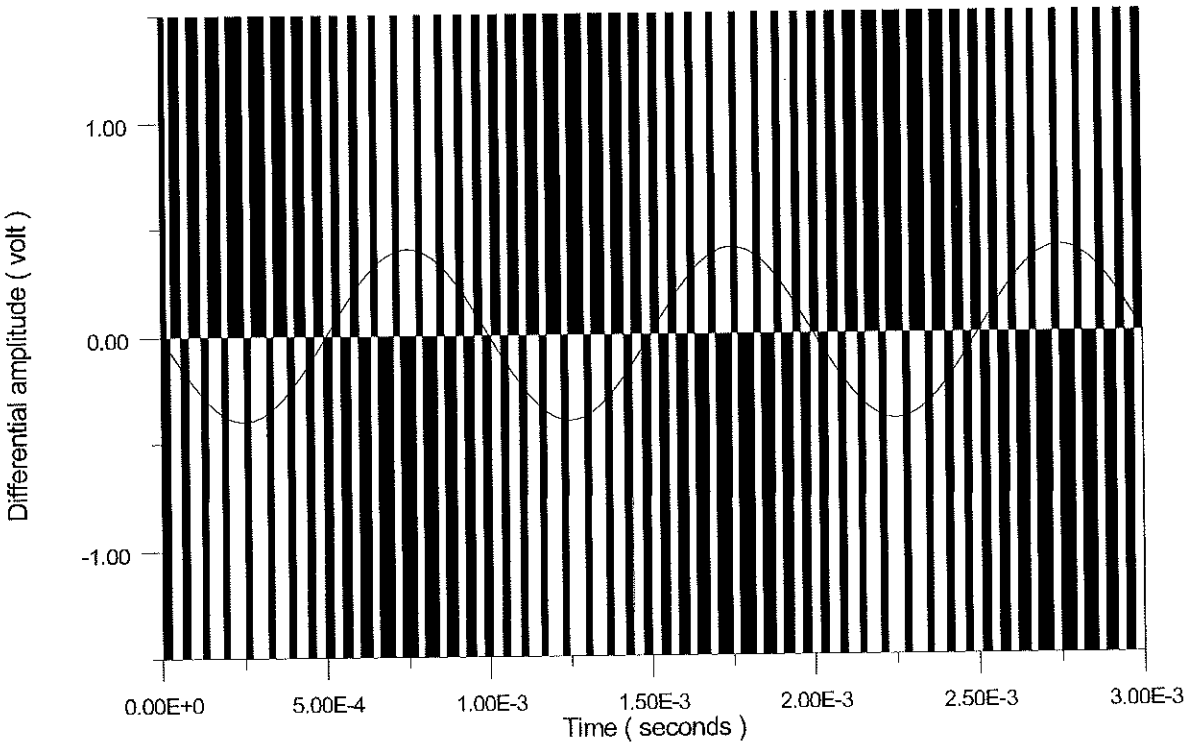

Figure 7.17: Simulated (SPICE) output of the modulator, when processing 1khz sine wave

Table 7.2: Simulated specifications of implemented $\Sigma\ \Delta$ modulator

Maximum differential input signal MSA	$0.48V_{RMS}$
Analogue RMS noise voltage 0-10kHz	$20.5\mu V_{RMS}$
Total maximal SNR	$87dB\ re\ MSA \simeq 21\mu V_{RMS}$
Current Consumption	$100\mu A$
Supply Voltage Range	*1V-1.5V and 5V(switches + digital part)*

of bias requirements and noise performance of amplifiers is presented too. The total power consumption is as low as 150μW. The modulator operates on power supply of 1.5V and 5V for analogue and digital part + switches respectively.

The implemented chip did not behave as expected. It is not yet clear if a design error or a layout or error is the cause. The latter is though the most likely, as a SPICE simulation of the implemented modulator performed nicely and a full LVS was not performed.

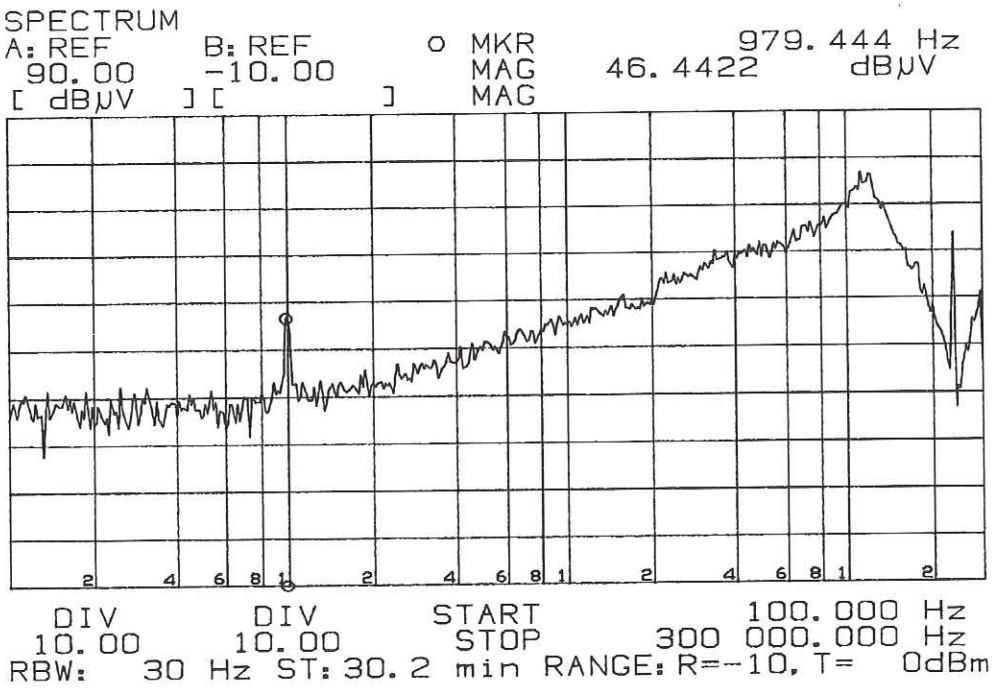

Figure 7.18: Spectrum of the modulator processing a sine wave

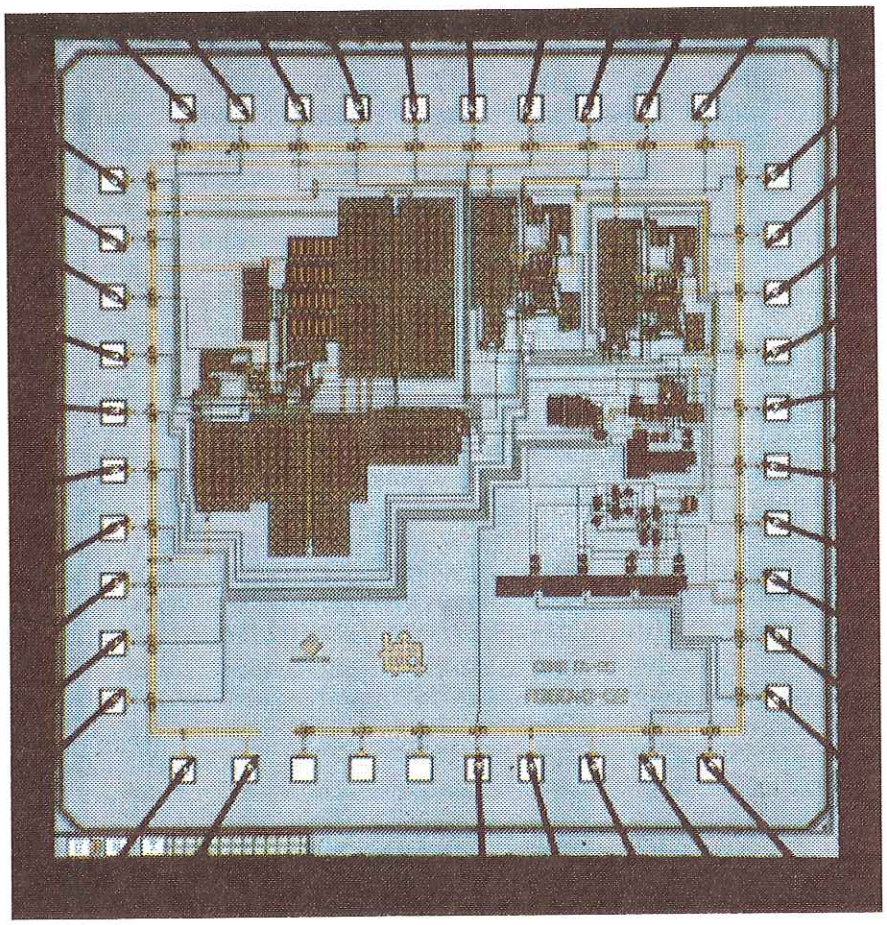

Figure 7.19: Chip microphotograph

Chapter 8

Conclusions

In this thesis the focus is on low power / low voltage interface circuits in CMOS micro electronic technology for capacitive microphones.

It has been shown that CMOS technology is the best choice for analog signal processing circuitry. Future CMOS VLSI technologies will posses the well known advantages of bipolar technology as low 1/f noise and high bandwidth. Furthermore CMOS has the, for low power low voltage designs, very useful feature of a very large input impedance.

It is shown that the single stage OTA is the best choice of amplifier building blocks for low power analog signal processing circuitry. Especially amplifiers with a feedback factor close to one is best designed as single stage OTAs. Furthermore, it is shown that the inverter is the optimum choice for a single stage OTA.

Design methodologies for low voltage design is presented. Both time continuos designs and switched designs are presented. The switched designs makes it possible to add essentially all features of designs operated on high power supply voltages.
The expenses are switching schemes and extra complexity. The switched designs can only be implemented in CMOS technology.

$\Sigma\Delta$ modulators are compatible with low power design. It is shown how to design low power $\Sigma\Delta$ modulators.

It is also shown how a detection circuitry can be designed for a capacitive microphone. Furthermore, we have shown that a $\Sigma\Delta$ modulator embedding a capacitive microphone in a feedback loop, using electrostatic force feedback, is very advantageous. The advantages are improved linearity, reduced parameter spreading ,direct digital conversion and easy stabilization of the feedback loop.

A CMOS amplifier matching a capacitive microphone is presented. The circuitry has been implemented in a standard $0.7\mu m$ CMOS technology. The amplifier reaches a SNR of 94dB at a power supply voltage of 1.5V with a current consumption of $40\mu A$. Operation of the amplifier with full rail to rail output swing is possible at a supply

voltage of 1V. This CMOS amplifier performs better than the traditional JFET amplifier used today. The overall chip area is 0.7mm·1.2mm.

A low power / low voltage $\Sigma\Delta$ modulator intended for use in a force feedback loop with a micro mechanical capacitive microphone is presented. the modulator is operated on a 1.5 power supply voltage with a total current drain of $100\mu A$. The very low power consumption was mainly due to the use of differential switched amplifiers used in the integrators. The simulated SNR was 86dB. Overall chip size was 3mm · 3mm.

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Part III

Appendices

Appendix A

Settling of Second Order Systems

In this appendix settling of the second order system with feedback is treated.

A.1 The Second Order System with Feedback

A great number of analog signal processing circuits can be categorized as being of second order. The types of analog signal processing circuits we will consider here are feedback systems with two poles in the feedback loop. Normally one of the poles is dominating over the other. i.e. it has a larger time constant. The second pole is the next pole of importance or it can be the total effect of all non dominating poles. This is of great importance as most systems then can be modeled as second order systems. We will model the open loop gain of a second order system with feedback by :

$$A(s) = \frac{1}{s\tau_1(s\tau_2 + 1)} \tag{A.1}$$

Where τ_1 and τ_2 are the time constants of the first and second pole.
In figure Fig. A.1 a principle of a second order system with feedback is shown. If the

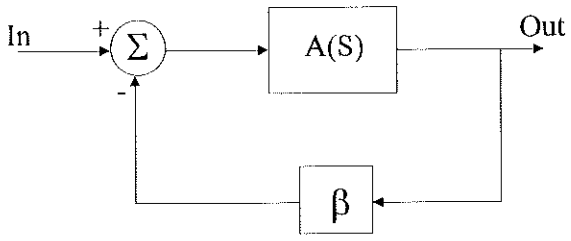

Figure A.1: Second order system with feedback.

feedback is β then the closed loop transfer-function is:

$$\frac{out}{in} = \frac{\beta}{s\tau_1(s\tau_2 + 1) + \beta} = \frac{1}{\beta} \cdot \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{A.2}$$

Where $\omega_o = \sqrt{\frac{\beta}{2 \cdot \tau_1 \cdot \tau_2}}$, $\frac{\omega_o}{Q} = \frac{1}{2 \cdot \tau_2}$ and $Q = \sqrt{\frac{\beta}{\tau_1 \tau_2}}$. The step-response can then be calculated. The step-response has three different solutions depending of the roots of the nominator of the equation. These are over damped, critically damped and under

damped. And they corresponds to $Q < 0.5$, Q = 0.5 and $Q > 0.5$. We will now treat them one by another. All solutions has been multiplied by β. A step-response of an under damped second order system can be seen in Fig. A.2.

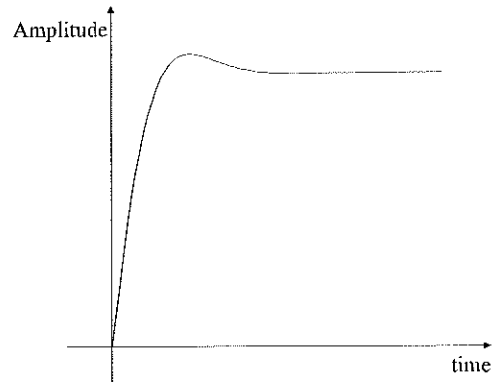

Figure A.2: Step-response of an underdamped second order system.

A.2 Over Damped Second Order System

For a over damped second order system ($Q < 0.5$) the step-response is :

$$1 - \frac{1}{2\sqrt{1-4Q^2}} e^{-\frac{\omega_o}{2Q}t}((1+\sqrt{1-4Q^2})e^{\frac{\sqrt{1-4Q^2}}{2Q}\omega_o t} - (1-\sqrt{1-4Q^2})e^{\frac{\sqrt{1-4Q^2}}{2Q}\omega_o t}) \quad \text{(A.3)}$$

Which for small Q's (or $\tau_1 \gg 2\beta\tau_2$)can be approximated by :

$$1 - e^{-\omega_o \cdot Q \cdot t} \quad \text{(A.4)}$$

Where $\omega_o \cdot Q = \frac{\beta}{\tau_1}$

A.3 Critically Damped Second Order System

The critically damped system (Q = 0.5) step-response is :

$$1 - (1 + \omega_o \cdot t)e^{-\omega_o \cdot t} \quad \text{(A.5)}$$

A.4 Under Damped Second Order System

And finally the step-response of a under damped ($Q < 0.5$) second order system is :

$$1 - \frac{1}{\sqrt{1-\frac{1}{4Q^2}}} e^{-\frac{\omega_o}{2Q}\cdot t} \cdot sin(\omega_o \sqrt{1-\frac{1}{4Q^2}} \cdot t + \Phi) \quad \text{(A.6)}$$

Where :

$$\Phi = tan^{-1}(\sqrt{4Q^2 - 1}) \tag{A.7}$$

The settling can for large Q's (or $\tau_1 \ll 2\beta\tau 2$) be approximated by :

$$1 - e^{-\frac{\omega_o}{2Q}t} \tag{A.8}$$

Where $\frac{\omega_o}{2Q} = \frac{1}{2\tau_2}$

A.5 Estimation of a Unified Time constant

The equation A.3, A.5 and A.6 are for practical use too complicated. Instead an approximation of the settling response in all regions can be made. We se from equation A.4 and A.8 that the settling always takes the form :

$$1 - e^{-\frac{t}{\tau_s}} \tag{A.9}$$

For the case of large Q ($\tau_1 \gg 4\beta\tau_2$) τ_s equals $\frac{1}{2\tau_2}$ and for very small Q ($\tau_1 \ll 4\beta\tau_2$) equals $\frac{\beta}{\tau_1}$ The time constant for the exponentially settling can thus be approximated by [50]:

$$\tau_s \simeq 2\tau_2 + \frac{\tau_1}{\beta} \tag{A.10}$$

The approximated settling time is then :

$$T_s \simeq (2\tau_2 + \frac{\tau_1}{\beta})ln\frac{1}{\varepsilon} \tag{A.11}$$

Appendix B

Settling of SC CDS Amplifier

B.1 Switched Capacitor Amplifier With CDS

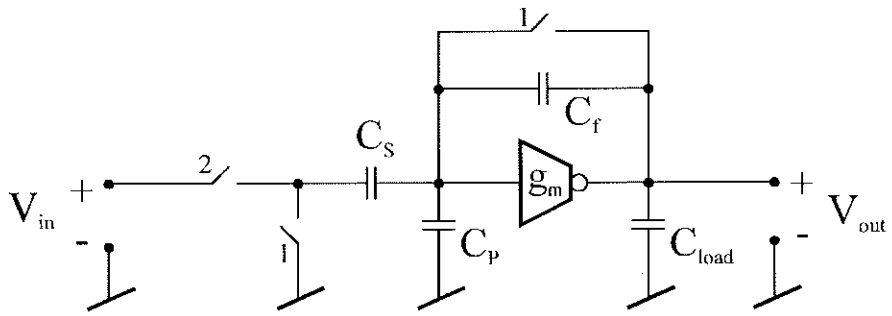

Figure B.1: Switched capacitor amplifier with CDS

In this section we will analyze an switched capacitor OTA amplifier. The OTA utilizes correlated double sampling. The circuitry can be seen in Fig. B.1. It consists of an OTA amplifier with transconductance g_m. The capacitance's C_S, C_f,C_P and C_{load} represents source capacitance, gain capacitance, parasitic capacitance and load capacitance. To implement correlated double sampling a two phase non overlapping switching scheme has been applied. We will now analyze the settling behavior in the two phases. We will assume that the time constants of the switches and capacitance are much smaller than the ones of the OTA and the capacitance's, i.e. the switches can be regarded as short circuits when turned on.

B.1.1 Settling Behavior During Phase 1

The OTA is during phase 1 coupled as shown in Fig. B.2. Before t = 0 the circuit is at rest and the voltage at the output is zero. A step function at the input of the amplifier at t =0+ will cause the output voltage to jump. After t = 0+ the output will decay slowly towards zero. This can be seen in Fig. B.3. The settling behavior can be described mathematically as :

$$V_o(t) = \mu(t) \cdot \frac{C_S}{C_S + C_P + C_f + C_{load}} \exp^{-\frac{g_m}{C_S+C_P+C_f+C_{load}} \cdot t} \tag{B.1}$$

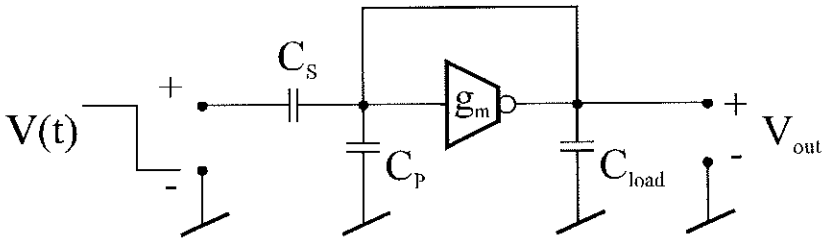

Figure B.2: Amplifier during phase 1

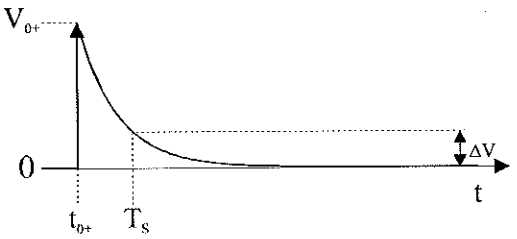

Figure B.3: Settling of amplifier during phase 1

From this the time T_S to settle within $\varepsilon = \frac{\Delta V}{V_\infty}$ can be calculated to :

$$T_S = \frac{C_S + C_P + C_{load}}{g_m} \ln \frac{1}{\varepsilon} \tag{B.2}$$

B.1.2 Settling Behavior During Phase 2

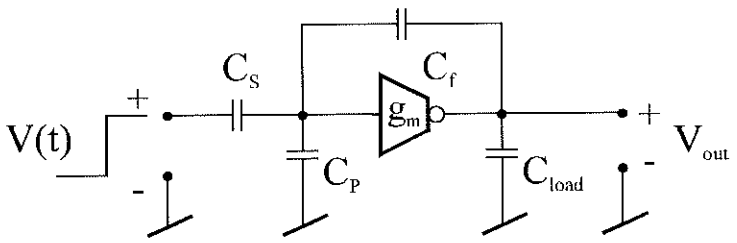

Figure B.4: Amplifier during phase 2

During phase 2 the amplifier is coupled as the one of Fig. B.4.Before t = 0 the circuit is at rest and the output voltage is equal to zero. A step at the input at t = 0 will cause the output of the amplifier to jump to a voltage of V_{0+}. After t = 0+ the output decays slowly towards the final value of V_∞. These two voltage's equals :

$$V_o(t = 0+) = \frac{C_S}{C_{leff}} \quad and \quad V_o(t = \infty) = -\frac{C_S}{C_f} \tag{B.3}$$

Where $C_{leff} = C_S + C_P + (C_f + C_S + C_P) \cdot \frac{C_{load}}{C_f}$
As it is seen the output first jumps to the opposite direction of the final value. This is due to the feed-forward path via C_f. Or it can be interpreted as a left half plane zero in the Laplace domain. This slows down the settling a bit.

The settling can be described mathematically as :

$$V_o(t) = -\frac{C_S}{C_f} \cdot (1 - (1 + \frac{C_f}{C_{leff}}) \exp^{\frac{g_m}{C_{leff}} \cdot t}) \tag{B.4}$$

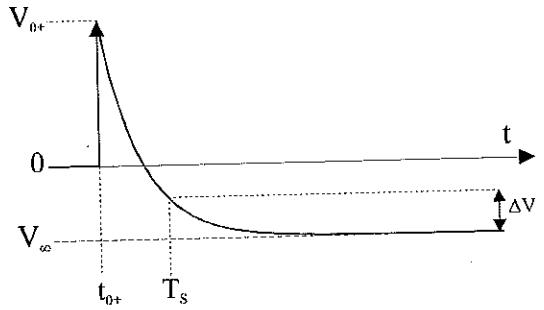

Figure B.5: Settling of amplifier during phase 2

From this the time T_S to settle within $\varepsilon = \frac{\Delta V}{V_\infty}$ can be calculated to :

$$T_S = \frac{C_{leff}}{g_m} \ln \frac{1 + \frac{C_f}{C_{leff}}}{\varepsilon} \tag{B.5}$$

Appendix C

Noise in Analog Signal Processing Circuitry

C.1 Bandwidth Limited White Noise

The term bandwidth limited white noise is an contradiction. White noise is by nature not bandwidth limited. By definition it has a spectral density of [51]:

$$S_v(f) = Constant \tag{C.1}$$

White noise is a mathematically ideality. Calculating the power of white noise one will notice that it is infinite. In the real world this is obvious not true. The reason why this does not happen is that in the real world a bandwidth limitation is always present. Thus limiting the power. This is the origin of bandwidth limited white noise. We will now go through a very basic example.

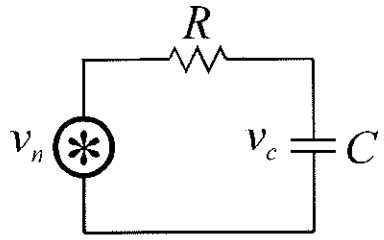

Figure C.1: Noise from a RC circuit

Example C.1.1
In Fig. C.1 the simplest circuitry with bandwidth limited white noise is shown. It consists of a noisy resistor. Its equivalent spectral noise voltage density and a capacitor. We will now calculate the mean squared rms. voltage across the capacitor. It can be calculated as :

$$S_v = \int_0^\infty S_v(f) \cdot |H(f)|^2 df = \frac{kT}{C} \tag{C.2}$$

Where $|H(f)|^2$ is the amplitude value of the transfer function from $S_v(f)$ to $V_c(f)$. As it is seen, it only depends of the capacitor value. It should be noticed that the integration is done from 0Hz to $+\infty$ This is custom among circuit designers whereas

the tradition, in the field of signal analysis, is to integrate from $-\infty$ to $+\infty$ and to use double sided Fourier etc. The white noise of a resistor is, in case of one sided (0Hz to $+\infty$) integration, equal to $V^2_{noise} = 4KTR$.

As the white noise is a stationary stochastic signal it is convenient to describe it with its auto-correlation function [51]:

$$R_{vn} = 2kTR \cdot \delta(\tau) \tag{C.3}$$

The auto-correlation function expresses the correlation between to samples of the signal at two distinct times. If it is zero there is no correlation. As it is seen from equation C.3 there is no correlation between two samples taken at two distinct times (R_{vn} equals zero outside $\tau = 0$). As we will se later this is a mathematical ideality. If we take the example of bandwidth limited white noise, then the auto-correlation function of the voltage across the capacitor can be found as the convolution between the white noise auto-correlation function and the auto correlation function of the RC filter :

$$R_{vC}(\tau) = R_{vn} \otimes R_{RC}(\tau) = \frac{kT}{C} \cdot \exp^{-\frac{|\tau|}{RC}} \tag{C.4}$$

We now see that adding a bandwidth limitation actually adds some correlation between two samples. I.e. the capacitor remembers the previous value of the noise signal. From equation C.4 it is also seen that as long as $\tau \gg RC$ then there is little correlation. And this is actually the case in most analog sampled systems. The mean squared value or the rms value across the capacitor can also be calculated setting τ equal to zero in equation C.4. Again it is seen to be $\frac{kT}{C}$ We will now discuss what effect sampling has on white noise spectra. ■

C.2 Sampling of White Noise

We saw in the previous section that as long as two samples of a white noise source were taken with a time difference τ which is much larger than $\frac{2\pi}{BW}$, where BW is the bandwidth of the noise signal, then each pair of samples can be considered as being un-correlated. I.e. the noise can be considered being white. In analog sampled systems it is characteristic that the sample time interval δT' is much larger than $\frac{2\pi}{BW}$. This is to assure that the analog sampling system can settle before the next sampling is performed. We can now consider each pair of sample to be un-correlated. Sampling of the white noise signal is equivalent to sampling its auto-correlation function :

$$S_{nb}(f) = S_n \cdot f_s \cdot \sum_{n=-\infty}^{+\infty} |B(f - nf_s)|^2 \tag{C.5}$$

Where B(f) is the bandwidth limiting filter. Equation C.5 tells us that replica of the original noise signal will be spread around multiples of the sampling frequency f_s. In Fig. C.2 the sampling of signal with a bandwidth equal to the sampling frequency is seen. We have assumed that the signal is bandwidth limited by a brick wall filter. As it is seen all of the available noise power will be situated within $-f_s/2$ and $+f_s/2$. This can also be seen from equation C.5. This is a very important result.

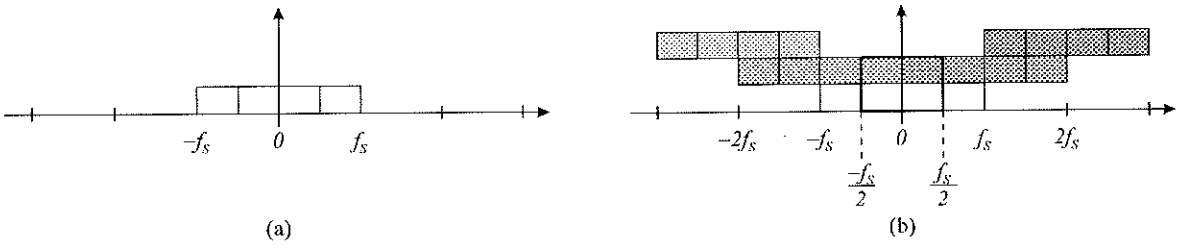

Figure C.2: Under-sampling

C.3 Sampled & Held White Noise

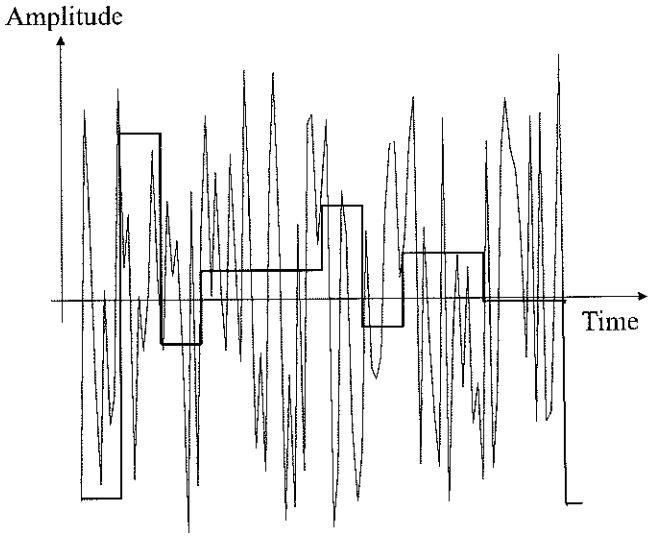

Figure C.3: sampled and held noise

In Fig. C.3 white noise and its sampled and held value [8] is shown. It is easy to see what happens in the time domain but what happens in the frequency domain ?

The sampling of white noise leaves a white noise spectrum. The hold function is mathematically equivalent of folding the sampled signal with a square wave :

$$h(t) = (f(t) \cdot \sum_{n=-\infty}^{+\infty} \delta(t)) \otimes g(t) \tag{C.6}$$

Where f(t), g(t) and h(t) are the noise signal, square wave and sampled and held noise signal. If we Fourier transform this then the result is a signal with a frequency response equal to that of a sinc function [8]. This can be seen in Fig. C.4

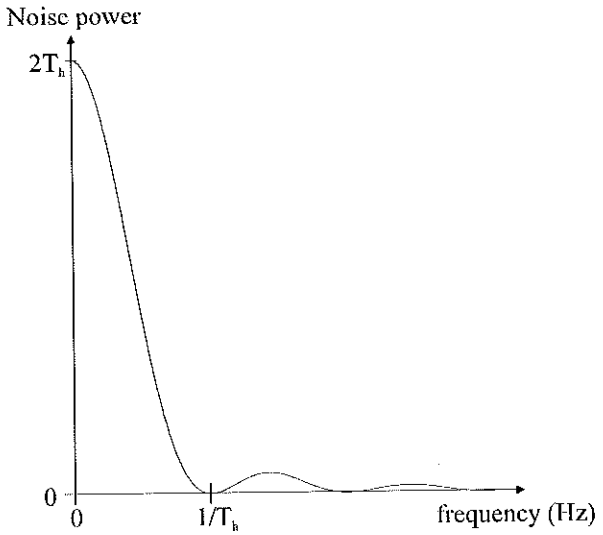

Figure C.4: Frequency response of hold function (Sinc function)

C.4 Correlated Double Sampling (CDS)

Correlated double sampling is the operation of subtracting the previous value from the present. Normally this is done at a sampling frequency doubled compared to the sampling of the signal. The signal is only sampled once and is thus not exposed to the double sampling. It is only unwanted disturbances that are exposed to CDS. We will now go through a very basic example of correlated double sampling.

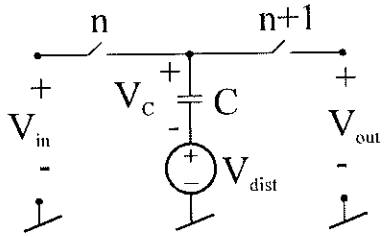

Figure C.5: Basic example of CDS

Example C.4.1
In Fig. C.5 a very basic example of correlated double sampling is shown. It is a two phase switched circuitry. At the first phase (n) the input signal V_{in} is sampled and at the same time the voltage disturbance is sampled at the other side of the capacitor. At phase n+1 it is held at the output of the circuit. This can be expressed as :

$$V_{out}(n+1) = V_{dist}(n+1) + V_C(n) = V_{in}(n) + (V_{dist}(n+1) - V_{dist}(n)) \qquad \text{(C.7)}$$

Or expressed in the Z domain :

$$V_{out}(Z) = V_{in}(Z) \cdot Z^{-1} + V_{dist}(Z)(1 - Z^{-1}) \qquad \text{(C.8)}$$

We can see that the signal is delayed one sample period and that the disturbance signal V_{dist} is exposed to the function $H(Z) = 1 - Z^{-1}$. If we evaluate this in the frequency domain we get :

$$|H(f)|^2 = |\exp^{-j\frac{\pi f}{f_s}}| \cdot |\exp^{j\frac{\pi f}{f_s}} - \exp^{-j\frac{\pi f}{f_s}}| = |2sin(\frac{\pi f}{f_s})|^2 \quad (C.9)$$

■

C.4.1 White Noise Exposed to Correlated Double Sampling

We will now discuss what happens with white noise that is exposed to correlated double sampling CDS. If we assume that the noise is white, i.e. the bandwidth of the noise is much larger than the sampling frequency then we can assume that two samples will be un-correlated. That is, their noise power can directly be added. The effect of subtracting two adjacent samples from each other is actually to add their powers.

C.4.2 1/f Noise Exposed to Correlated Double Sampling

As two samples of a 1/f noise signal are strongly correlated then CDS will be very effective. We will now try to calculate how effective. We will calculate the part of the 1/f noise power exposed to CDS situated within the signal band $[-f_b; +f_b]$. We will assume that the signal is sampled at a much higher than the signal band frequency. I.e. the over-sampling ratio is large. The 1/f noise has the spectral power density of $P_{1/f}(f) = \frac{K}{f}$

The noise power of the CDS exposed 1/f noise is :

$$P_{1/fCDS} = 4K \cdot \int_{-f_b}^{+f_b} \frac{sin^2(\frac{\pi f}{f_s})}{f} df \quad (C.10)$$

An symbolic integration and following Taylor expansion gives

$$P_{1/fCDS} \simeq \frac{K}{2} \cdot (\frac{\pi}{OSR})^2 \quad (C.11)$$

Where $OSR = \frac{f_s}{f_b}$ We see that a large over-sampling ratio suppresses the unwanted low frequency 1/f noise.

C.5 Noise From Switches and Amplifiers

In actual implementation of sampled CMOS signal processing circuits there are two sources of noise. The first is switches and the second is amplifiers. We will now discuss the two noise sources.

C.5.1 Switches

A switch is actually a noisy resistor which in conjunction with a capacitor forms a bandwidth limited white noise source [46] [47]. If the capacitor value is C then the total noise power is $\frac{kT}{C}$. The circuitry of Fig. C.5 can be used again to illustrate this. During the 'on' state of the switches the noise is sampled on the capacitor. Because of heavy under-sampling all of the noise power will be situated within $-f_s/2$ to $-f_s/2$

[8]. The reason for under-sampling is that the circuit has to be able to settle within each sampling period. I.e. the bandwidth of the switch and the capacitor is much larger than the sampling frequency. The off state of the switches is not considered to contribute to the noise on the capacitor. This is due to the fact that it can be considered as very slowly varying signal [46] [47]. Nearly as a DC signal.

C.5.2 Amplifiers

Again we must assume that the bandwidth of an amplifier used in a sampled system will be much larger than the sampling frequency. Otherwise the amplifier will not be able to settle within the sampling period. This means that calculating the total noise power at the output of the amplifier will give us the total noise within the frequency band $-f_s/2$ to $+f_s/2$. We will now use an example of an OTA amplifier.

Example C.5.1
An example of an OTA amplifier during one phase of a switched system is shown in Fig. C.6. Switches have been left out as their noise can be calculated separately and normally can be neglected. Noise from the amplifier is represented by V_{noise}

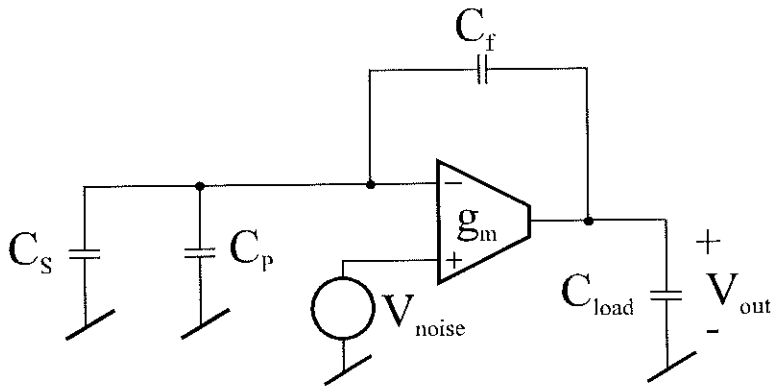

Figure C.6: OTA amplifier with noise source during one phase

Calculating the noise power at the output one gets :

$$V^2_{noutput} = V^2_{noise} \cdot \int_{-\infty}^{\infty} |A_{+out}(f)|^2 df \tag{C.12}$$

Where $A_{+out}(f)$ *is the transfer-function from the noise source to the output. The noise power can be calculated to [8]:*

$$V^2_{noutput} = kT\gamma \frac{1}{C_{eff} \cdot \beta} \tag{C.13}$$

Where γ,β *and* ,C_{eff} *equals the ratio between noise resistance and trans-conductance [8], feedback coefficient* $\beta = \frac{C_f}{C_S+C_P+C_{load}}$ *and* $C_{eff} = C_{load} + \frac{C_f \cdot (C_S+C_P)}{C_f+C_S+C_P}$ ■

Appendix D

Optimal Gate Area of CMOS Input Stages Matching a Capacitive Source

When designing input stages optimized for capacitive sources there are two aspects one has to consider to achieve the largest possible signal to noise ratio. First there is the noise of the input stage itself. It is obvious that for a given signal swing the noise should be as small as possible to achieve the largest SNR. Normally a low noise input stage is accompanied by a large input capacitance, thus loading the capacitive source.

So the second aspect is the input capacitance. It will be shown that optimum of input capacitance's for achieving largest possible SNR exists [39].

Fig. D.1 shows a CMOS differential input stage matching a capacitive source. The capacitive source is represented by V_{Source} and C_{Source}. A parasitic capacitive load is represented by C_P. The input stage consists of transistors M_1 and M_2. It is biased by a current source I_{BIAS}. Both white noise and low frequency 1/f noise of the differential stage is represented by the noise voltage source V_{noise}.

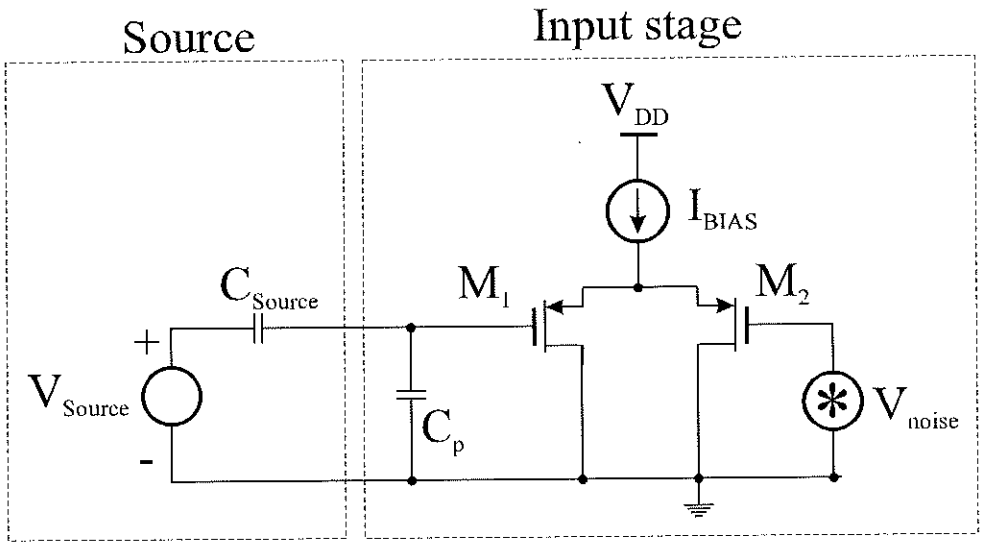

Figure D.1: Differential input stage matching a capacitive source

In the following optimal signal to noise ratios and optimal dimensioning of input stages is done both for differential stages and for common source and source followers. The parameter a equals 1 in case of a common source stage or a source follower. In case of a differential stage a equals 2.

D.1 Input Stage White Noise

In this subsection we will first give equations for input capacitance, white noise and trans-conductance of CMOS input stages. Then we will calculate the optimal aspect ratio $\frac{W}{L}$.

D.1.1 Strong Inversion Operation

It is a well known fact that thermal white noise of a CMOS transistor in strong inversion equals :

$$I^2_{noise\ drain}(f) = 4kT\frac{2}{3}K_P\frac{W}{L}(V_{gs} - V_T) \tag{D.1}$$

At the same time the input capacitance of the input stage is :

$$C_{in} = \frac{2}{3a}WLC_{ox}\alpha \tag{D.2}$$

Where $\alpha = 1 + \frac{3L_d}{2L}(1 + a)$ and a equals 2 for a differential stage and 1 for source follower and common source stage. The input capacitance C_{in} accounts for gate source capacitance and overlap capacitance's. If one wishes to take gate bulk capacitance into account then α can be modified to $\alpha = 1 + \frac{3L_d}{2L}(1 + a) + \frac{n-1}{2n} \cdot a$ [40].

From this and Fig. D.1 the input referred equivalent noise can be calculated as :

$$V^2_{equi\ therm}(f) = 4kT\frac{2a}{3}\frac{L}{\sqrt{2I_DK_PWL}}(1 + \frac{2}{3}\frac{WLC_{ox}\alpha + \frac{3a}{2}(C_P + C_f)}{aC_{source}})^2 \tag{D.3}$$

It is seen that a optimum exists. This comes from the fact that increasing the aspect ratio will lower the noise but also increase the gate area and thus the damping of the signal due to capacitive loading. The optimum is located at :

$$WL = a\frac{C_P + C_{mic}}{2C_{ox}\alpha} \tag{D.4}$$

Or it can be interpreted as :

$$C_{in} = \frac{a}{3} \cdot (C_P + C_{mic}) \tag{D.5}$$

And the value associated with the minimum is :

$$V^2_{equi\ therm}(f) = 4kT\frac{2a}{3}\frac{L}{\sqrt{aI_dK_P}}\sqrt{\frac{C_{ox}\alpha}{C_P + C_{mic}}}(\frac{4}{3}\frac{C_{mic} + C_P}{C_{mic}})^2 \tag{D.6}$$

So the channel length should be as small as possible. This indicates that a small line width technology should be used. As we see a differential stage is twice as noisy , considering the thermal noise, as a single transistor stage.

D.1.2 Weak Inversion Operation

In weak inversion the input capacitance C_{in} is :

$$C_{in} = \frac{n-1}{a \cdot n} W L C_{ox} \cdot (1 + \alpha) \tag{D.7}$$

Here the input capacitance C_{in} corresponds to the gate bulk capacitance. In true weak inversion this is the dominating part. Now α equals $\frac{a \cdot n}{n-1} \cdot \frac{L_d}{L}$ At the same time the noise voltage of a MOS transistor operated in weak inversion is [8] [40]:

$$V^2_{noise\ weak\ inv\ therm}(f) = 4kT\frac{n}{2}\frac{nV_t}{I_D} \tag{D.8}$$

Again the input referred equivalent noise can be calculated as :

$$V^2_{equi\ weak\ inv\ therm}(f) = 4kT\frac{n \cdot a}{2}\frac{nV_t}{I_D}(1 + \frac{\frac{n-1}{n \cdot a} W L C_{ox} + (C_P + C_f)}{C_{mic}})^2 \tag{D.9}$$

As it is seen here the input referred nose is minimal when the gate area WL of the input transistors are minimal. At the same time the condition of weak inversion operation can be written as :

$$W \geq L_{min} \cdot \frac{2n \cdot K_p \cdot V_t^2}{I_D} \tag{D.10}$$

Where L_{min} is the minimal gate length. And the width W is the minimal gate width that assures weak inversion operation. I.e. the minimal gate area that assures weak inversion operation. So the gate area should be as small as possible but still weak inversion should be assured for the given current. Weak inversion operation assures the best signal to noise ratio considering channel white noise.

D.2 Input Stage Low Frequency 1/f Noise

In this subsection we will first give equations for input capacitance, 1/f noise and trans-conductance of CMOS input stages. Then we will calculate the optimal aspect ratio $\frac{W}{L}$.

D.2.1 Strong Inversion Operation

It is a well known fact that low frequency 1/f noise of a CMOS transistor in strong inversion equals :

$$I^2_{noise\ drain\ 1/f}(f) = \frac{1}{f}\frac{K_f \cdot I^{AF}_{drain}}{L^2 C_{ox}} \tag{D.11}$$

From this and Fig. D.1 the input referred equivalent noise can be calculated as :

$$V^2_{equi\ 1/f}(f) = \frac{a}{2}\frac{1}{f}\frac{K_f}{K_p W L C_{ox}}(1 + \frac{2}{3}\frac{W L C_{ox}\alpha + \frac{3a}{2}(C_P + C_f)}{a C_{source}})^2 \tag{D.12}$$

Where $\alpha = 1 + \frac{3L_d}{2L}(1 + a)$ and a equals 2 for a differential stage and 1 for source follower and common source stage. Here α can also be modified to take the gate bulk capacitance into account. Again it is seen a optimum exists. This comes from the fact that increasing the aspect ratio will lower the noise but also increase the gate area and thus the damping of the signal due to capacitive loading. The optimum is located at :

$$WL = a\frac{3}{2}\frac{C_P + C_f + C_{mic}}{C_{ox}\alpha} \tag{D.13}$$

Or it can be interpreted as :

$$C_{in} = (C_P + C_f + C_{mic}) \tag{D.14}$$

And the value associated with the minimum is :

$$V^2_{equi\ 1/f}(f) = \frac{4}{3}\frac{1}{f}\frac{K_f\alpha}{K_p}\frac{(C_{mic} + C_p + C_f)}{C^2_{mic}} \tag{D.15}$$

As it is seen the minimal 1/f noise of a given technology only depends on $\frac{K_f\alpha}{K_p}$ and the capacitance values. Furthermore, it is seen that a differential stage is equal as noisy as both a source follower or a common source stage.

D.2.2 Weak Inversion Operation

The input capacitance in weak inversion is again :

$$C_{in} = \frac{n-1}{a \cdot n} WLC_{ox} \cdot (1 + \alpha) \tag{D.16}$$

And α equals $\frac{a \cdot n}{n-1} \cdot \frac{L_d}{L}$. In case of a PMOS transistor the 1/f noise is believed to be due to mobility fluctuations [52] [53]. This means that the 1/f noise voltage source in weak inversion is :

$$\frac{K_f \cdot I_D^{AF} \cdot (nV_t)^2}{f \cdot L^2 \cdot K_p \cdot I_D^2} \tag{D.17}$$

The input referred low frequency 1/f noise is now :

$$V^2_{equi\ weak\ inv\ 1/f}(f) = \frac{K_f \cdot I_D^{AF} \cdot (nV_t)^2}{f \cdot L^2 \cdot K_p \cdot I_D^2}\left(1 + \frac{\frac{n-1}{n \cdot a} WLC_{ox} + (C_P + C_f)}{C_{mic}}\right)^2 \tag{D.18}$$

As we see from this equation decreasing the gate length will increase the equivalent input referred 1/f noise. If the gate length increases far beyond $\frac{C_P + C_f}{W \cdot C_{ox}} \cdot \frac{n \cdot a}{n-1}$ then equation D.18 reduces to :

$$V^2_{equi\ weak\ inv\ 1/f}(f) = \frac{K_f \cdot I_D^{AF} \cdot (nV_t)^2}{f \cdot L^2 \cdot K_p \cdot I_D^2}\left(\frac{\frac{n-1}{n \cdot a} WLC_{ox}}{C_{mic}}\right)^2 \tag{D.19}$$

From this we see that minimal 1/f noise in weak inversion means large gate length and small gate width, i.e. low frequency 1/f noise is smallest in strong inversion.

D.3 Overview

In table D.1 the optimal input capacitance's for 1/f noise and white noise for both weak inversion operation and strong inversion operation. These apply for differential stages for a equal to 2 and common source stages and source followers for a equal to 1. We have previously seen that for low frequency 1/f noise it is optimal to use strong

Table D.1: Optimal input capacitance of input stage matching a capacitive source

Input capacitance	*Weak inversion operation*	*Strong inversion operation*
1/f noise	$C_{in} \ll (C_P + C_{Source})$	$C_{in} = C_P + C_{Source}$
Channel white noise	$C_{in} \ll (C_P + C_{Source})$	$C_{in} = \frac{a}{3}(C_P + C_{mic})$

inversion operation(see also [52] and [53])as this gives us the best SNR. And for channel white noise it is best to use weak inversion operation [10]. If the 1/f noise is dominating then the optimum for 1/f noise in strong inversion should be chosen. If it is the channel white noise that dominates then the smallest possible gate area assuring weak inversion operation should be chosen. The third and troublesome possibility is that both 1/f noise and channel white noise has to be taken into consideration. In this numericall optimization has to be used. A qualified guess in this situation would be to use the 1/f noise optimum gate area and to chose an aspect ratio assuring moderate inversion operation as the input capacitance has its minimum there see [10]. Table D.2 summarizes the noise levels of the inversion modes.

Table D.2: Noise levels in different inversion modes.

Noise level	*Weak inversion operation*	*Strong inversion operation*
1/f noise	*High*	*Low*
Channel white noise	*Low*	*High*

Appendix E

Analog Signal Processing and Future CMOS Technology

In this appendix we will calculate some of the most important features of future short channel CMOS technologies considering analog signal processing [1].

E.1 Weak Inversion Current Limit

As weak inversion operation is of great importance when designing high performance analog circuitry, it is interesting to investigate how future short channel CMOS technologies will impact this. To evaluate this we notice that the weak inversion current limit is [10] :

$$I_D = 2n \cdot C_{ox}\mu \cdot \frac{W}{L}V_t^2 \tag{E.1}$$

The input capacitance in weak inversion is mainly due to the gate bulk capacitance [40]:

$$C_{gb} = \frac{n-1}{n} \cdot W \cdot L \cdot C_{ox} \tag{E.2}$$

The weak inversion current limit of a transistor operated in weak inversion with a given input capacitance of C_{in} can then be calculated to :

$$I_D = 2\frac{n^2}{n-1} \cdot C_{in} \cdot \mu \cdot \frac{1}{L^2}V_t^2 \tag{E.3}$$

This shows us that if all other parameters than L is constant then scaling of the technology will have an dramatic impact on the weak inversion current limit [1].

E.2 Maximum Gain Band Width GBW in Weak Inversion

We will calculate the maximal GBW of a given technology when operated in weak inversion. In Fig. E.1 the simplest possible gain stage is shown. The transistor has a aspect ratio of $\frac{W}{L}$. As the technology is minimized then the drain capacitance will

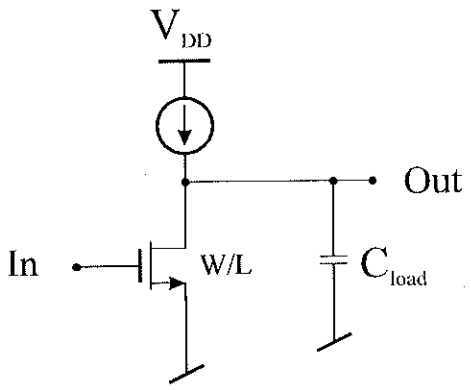

Figure E.1: Single transistor MOS amplifier

ultimately determine the capacitive load of the amplifier. The reason for this is that the contact to the drain normally doesn't scale as much as the channel length [9]. Therefore :

$$C_{load} = C_{drain} = X_{drain} \cdot W \cdot C_J \tag{E.4}$$

Where X_{drain} is the length of the drain region parallel to current flow and C_J is the junction capacitance per area for a drain-bulk voltage of 0 volts.

The gain band width can now be calculated to :

$$GBW = \frac{g_m \cdot R_o}{2\pi R_o \cdot C_{load}} \tag{E.5}$$

Now we define the weak inversion current limit to :

$$weaklim = \frac{2n\frac{W}{L}\mu C_{ox} V_t^2}{I_D} \tag{E.6}$$

Then the maximal GBW in weak inversion can be expressed as [9]:

$$GBW = \frac{2\mu C_{ox} V_t}{2\pi \cdot L \cdot X_{drain} \cdot C_J \cdot weaklim} \tag{E.7}$$

E.3 Charge Injection

We will now calculate what effect scaling has on charge injection.

In Fig. E.2 a sampling circuitry consisting of a MOS switch and a capacitor is shown. When the switch is turned on then the voltage across the capacitor is equal to the input voltage. When the transistor is shut off then the channel has to be discharged. We will as an worst case estimate assume that all of the charge in the channel will flow to the capacitor and charge this. The charge in the channel is [54]:

$$q = \frac{L^2}{\mu \cdot R_{on}} \tag{E.8}$$

Where L is the channel length, μ is the mobility and R_{on} is the on resistance of the switch. If the sampling circuitry shall be able to settle within a settling time of T_S

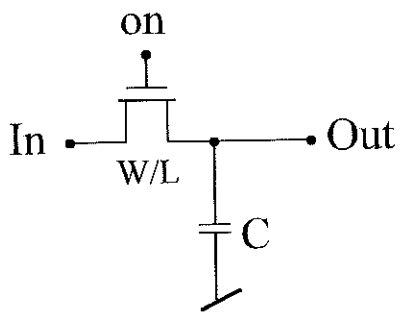

Figure E.2: MOS switch and capacitor

then R_{on} must maximally be :

$$R_{on} \leq \frac{T_S}{2C \ln \frac{1}{\varepsilon}} \tag{E.9}$$

Where ε is the settling error. If we use the maximal value and combine it with equation E.8 then it can be calculated that the disturbance of the sampled voltage will be :

$$\Delta V_{charge} = \frac{2L^2 \ln \frac{1}{\varepsilon}}{\mu T_S} \tag{E.10}$$

What can be seen from this is that scaling of the technology will inherently lead to a situation where charge injection is of no importance.

Part IV

Publications

The following papers have been published as a part of my Ph.D. study.

1. A Very Low-Noise/Low-Power Preamplifier for Capacitive Microphones

Presented at:
The thirteenth Norchip Conference NORCHIP'95
Copenhagen Denmark
November 7-8.

2. A Low-Noise/Low-Power Preamplifier for Capacitive Microphones

Presented at:
The International Conference on Circuits and Systems
ISCAS'96
Atlanta May 12-15

3. A High Resolution Switched Capacitor 1Bit $\Sigma\Delta$ Modulator for Low-Voltage/Low-Power Applications

Presented at:
The fourteenth Norchip Conference NORCHIP'96
Helsinki-Finland
November 4-5.

A very Low-Noise/Low-Power Preamplifier for Capacitive Microphones

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ABSTRACT

A design for a microphone preamplifier for hearing aid applications is presented. The amplifier operates at a supply of 1-1.5V, the current drain is 30μA. The maximum sound level allowed is more than 117 dB SPL (Sound Pressure Level), with a typical noise level of 23 dB SPL. The amplifier is optimised for a capacitive microphone with a very low capacitance (1.2pF) . The amplifier is fully integrated in a 0.7μm n-well CMOS technology . Design details concerning noise performance is analytically described.

I. INTRODUCTION

Current capacitive microphones for hearing aids use an electret design for the microphone. Electret microphone represent a capacitive source for the preamplifier. A Due to the low frequencies involved, the fact that microphones is miniaturerized and source capacitance is diminishing, a need for preamplifiers with a very low noise current is needed. Thus achieving acceptable signal to noise ratios. In traditional designs, a junction FET in a source follower configuration is used to buffer the signal from the microphone. Due to gate leakage current and the relatively low value of the bias resistor (1-10GΩ) the noise from a junction FET source follower can not be decreased. The value of the bias resistor can not be enlarged, because the leakage current imposes an upper bound. Other disadvantages of a junction FET source follower are, poor PSSR and low output swing. In order to lower the noise current of the preamplifier, MOSFETS which show a negligible gate leakage current, can be used. Two zero biased diodes can then be used as bias resistors, obtaining very large equivalent bias resistance and at the same time serve as protection diodes. Based on this, a fully integrated preamplifier can then be designed to obtain a superior PSSR and full output swing. Traditional design obtain noise level of 27 dB SPL and maximum sound level of 110 dB SPL. PSSR in traditional designs is no more than 30dB.

Others have designed integrated preamplifiers for electret microphones [6,8]. So far no solution has been presented that could compete with the ordinary junction FET source follower addressing SNR.

II. AMPLIFIER TOPOLOGY

An electret microphone consists of a capacitor which is charged by a permanent electric field. One off the capacitors plates acts as a diaphragm.The microphone can be represented as a voltage generator V_{mic} and a capacitor C_{mic} in series. The amplitude of the voltage generator is proportional to the incoming sound pressure. The proportionality constant, normally denoted the sensitivity, is usually in the range 5mV/Pa-20mV/Pa.

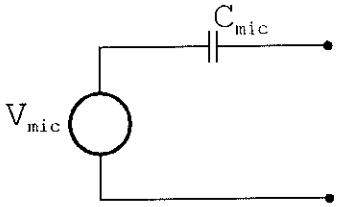

Fig. 1. Equivalent circuit for an electret microphone.

The amplifier topology in the actual design is a Differential Difference Amplifier (DDA) [5,9]. The amplifier topology is showed in Fig. 2 where C_{mic} is the capacitance of the microphone, C_p is the parasitic bonding capacitance and C_f is the feedback capacitance. The small signal resistance of the parallel diodes is denoted R_{diodes}. V_{ref} is used to set the DC voltage level at the output. A block diagram of the DDA is showed in Fig. 3.

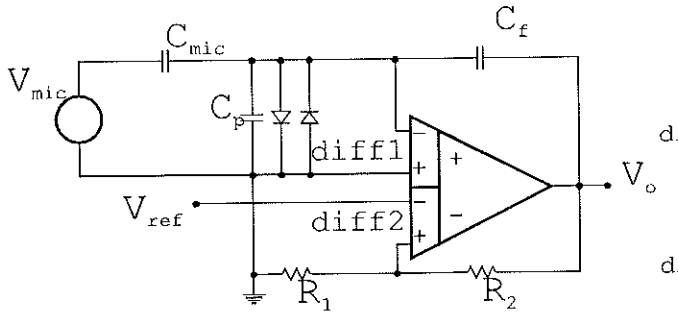

Fig. 2. Amplifier topology utilising DDA.

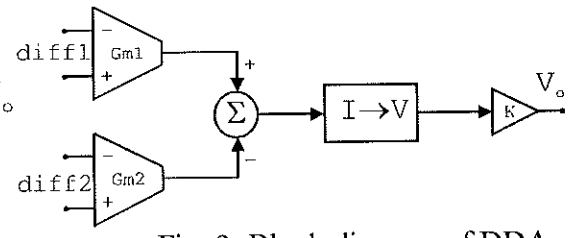

Fig. 3. Block diagram of DDA.

The DDA consist of two V→I converters (diff1 and diff2), a I→V converter and a gain k. Transconductances of diff1 an diff2 is denoted Gm1 and Gm2.
Below the unity gain frequency of the DDA, the transfer function from V_{mic} to V_o can be calculated to :

$$A_{mic}(s) = \frac{V_o}{V_{mic}} = -\frac{C_{mic}}{C_f}\frac{1}{1+\eta}\frac{s}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (1)$$

And from V_{ref} to V_o :

$$A_{ref}(s) = \frac{V_o}{V_{ref}} = (1+\frac{R_2}{R_1})\frac{\eta}{1+\eta}\frac{s+\omega_o}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (2)$$

Where

$$\omega_o = \frac{1}{R_{diodes}(C_{mic}+C_f+C_p)} \quad \text{and} \quad \eta = \frac{1+\frac{C_{mic}}{C_f}}{1+\frac{R_2}{R_1}}\cdot\frac{Gm2}{Gm1}$$

We see that it is desirable if $\eta \ll 1$. Then $A_{in}(s)$ will be equal to the gain from a charge amplifier. And the gain $A_{ref}(s)$, will be very small above ω_o. $\eta \ll 1$ can be obtained by $C_{mic}/C_f \ll R_2/R_1$ and Gm2 « Gm1.

III. Low-Noise Design of Input Stage

A. Configuration

The input stage chosen is a standard differential stage. The input stage corresponds to diff1 in the DDA. A differential stage is not the optimum choice for a low-noise design [2] but in this case it is convenient because the DC common mode voltage value, at the input diff1, can be set arbitrarily. In our case it is grounded. This would not have been possible with any other type of input stage.

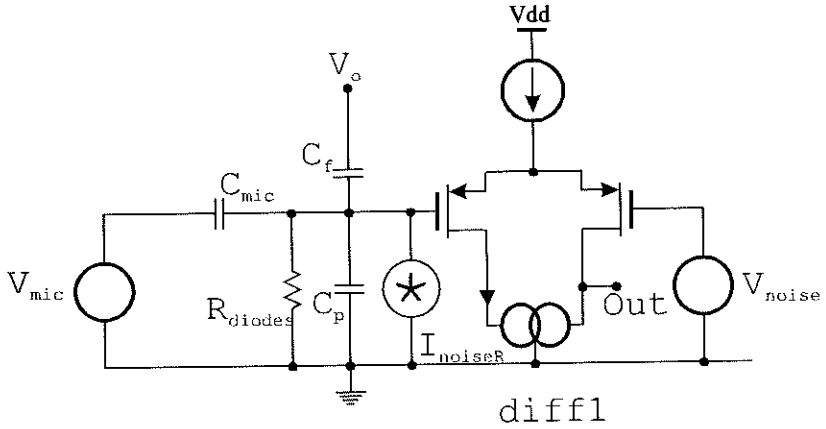

Fig. 4. Input stage configuration.

The noise from the input stage is represented by the noise voltage V_{noise} . This represents thermal noise and 1/f noise from the input stage. The white noise generated in the bias diodes is represented by I_{noiseR}. We will in the following only consider frequencies above $1/2\pi C_{mic}$. In order to calculate the SNR we will refer the noise to the input. this can be calculated to :

$$V_{neqi}^2 = I_{noiseR}^2 \frac{1}{(\omega C_{mic})^2} + V_{noise}^2 \left(\frac{C_{mic} + C_p + C_f}{C_{mic}} \right)^2 \qquad (3)$$

In our case this noise voltage should be weighted by the A weighting function in order to obtain the SNR(A). The A weighting function is showed in Fig. 5. Input transistors are assumed to operate in weak inversion, possibly moderate inversion as resent measurements show that noise in PMOS transistors is due to mobility fluctuations and not carrier number fluctuations [1,7]. Therefore they should preferably be biased in strong inversion. If possible.

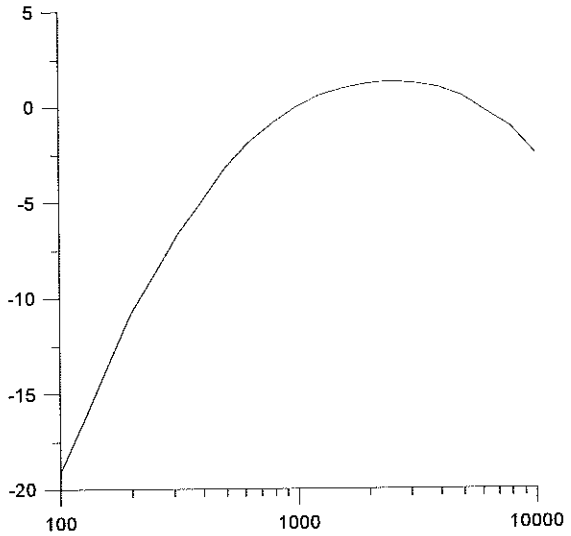

Fig. 5. A-Weighting Curve (dB).

B. Minimisation of Input Transistor Noise

First we define the following :

C_{ox} : Thin oxide capacitance pr. square.
I_d : MOST (MOS transistor) drain current.
K : Boltzmans constant $1.38 \cdot 10^{-23}$.
K_f : MOST 1/f noise parameter.
K_p : Transconductance parameter MOST.
L : MOST channel length.
L_d : Underdiffusion length.
T : Temperature in Kelvin.
V_t : 26mV.
W : MOST channel length.

The noise of the input stage can be divided into three noise sources. White noise from Bias diodes, white noise of input transistors and 1/f noise of input transistors. If we refer these to the input then they can be calculated as :

White noise from Bias diodes :

$$V^2_{neqiBiasres} = \frac{4KT}{R_{diodes}} \frac{1}{(\omega C_{mic}))^2} \tag{4}$$

As we see the noise from the bias resistor is moved to lower frequencies as the resistor gets larger. So it is advantageous that the bias resistor is as large as possible. The question is then, how large resistors can we implement onchip ? The best way of implementing very large resistors on chip is to implement them as junction diodes. Two zero biased diodes will be as noisy as resistor with the Value of :

$$R_{diodes} = V_t/(2I_{leak}) \tag{5}$$

Where V_t = 26mV and I_{leak} = 10fA for a minimum diode. This gives us R_{diodes} = 1.3TΩ.

Transistor generated thermal noise:

For the input referred transistor generated thermal noise, there exist an optimal gate area. This gate area gives minimal transistor generated thermal noise . It is located at :

$$WL = \frac{C_p + C_{mic} + C_f}{C_{ox}\alpha} \text{ , Where } \alpha = 1 + 9L_d/2L. \quad (6)$$

And the minimal input referred transistor generated thermal noise is :

$$V^2_{neqitherm\min} = 4KT\frac{4}{3}\frac{L}{\sqrt{2I_dK_p}}\sqrt{\frac{C_{ox}\alpha}{C_p + C_{mic} + C_f}}\left(\frac{4}{3}\frac{C_{mic} + C_p + C_f}{C_{mic}}\right)^2 \quad (7)$$

Transistor generated 1/f noise:

Again there exists a minimum. This is located at :

$$WL = 3\frac{C_p + C_{source} + C_f}{C_{ox}\alpha} \quad (8)$$

And the value associated with this minimum is :

$$V^2_{neqi1/f} = \frac{4}{3}\frac{1}{f}\frac{K_f\alpha}{K_p}\frac{(C_{mic} + C_p + C_f)}{C^2_{mic}} \quad (9)$$

Optimising for lowest noise :

As we see from equation 6 and 8, there exists to different optimal gate areas, where the thermal respectively the 1/f noise is minimal. The gate area for minimal 1/f noise is three times larger than the gate area for minimal thermal noise. The noisecorner frequency of the input transistors determines which gate area should be chosen. In this design, the noise corner is placed at a fairly low frequency inside the A weighting curve. So I have chosen gate area for minimal thermal noise. Normally one would have to use numerically optimisation using SPICE. But as SPICE MOST models underestimates thermal noise in moderate inversion this solution is not accurate. The solution is to use the EKV (Enz-Krummenacher-Vitoz) MOST model [3].

A technology with a small line width (0.7μm) has been chosen as the transistor generated white noise decreases as the minimum channel length decreases. The 1/f noise also benefits from a small line width technology, as K_p increases. Furthermore small line width technologies normally have better 1/f noise parameters.

PMOST transistors has been chosen as input transistors at they exhibit much lower 1/f noise than NMOS transistors. This is due to the fact that the dominating noise mechanism in PMOS transistors is mobility fluctuations and carrier number fluctuations in NMOS transistors.

C. Minimisation of Total Noise

The total noise from the amplifier consist of contributions from the input transistors and from all other transistors. Having minimised noise from input transistor one should assure that contributions from all other transistors is negligible to those of the input transistors. This is easily done, keeping in mind, that the transconductance g_m of the input transistors should be larger than all other transistors. Input transistors should be shorter than all other transistors.

IV. Overall Design

The schematic of the amplifier is showed in Fig. 6 below.

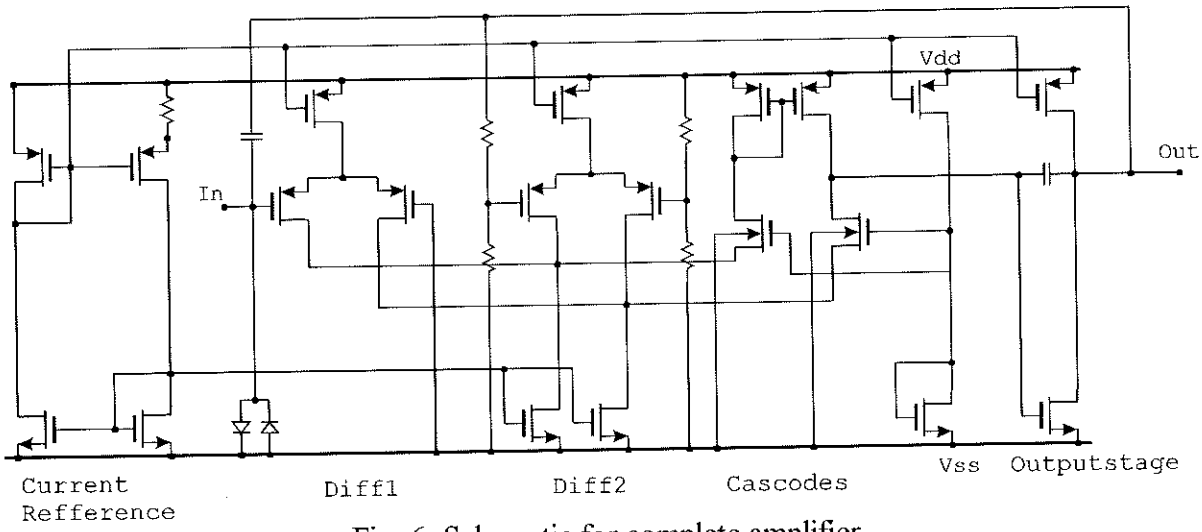

Fig. 6. Schematic for complete amplifier.

It consists of 5 sections. A current reference [4], inputstage (Diff1), bias input stage (Diff2), folded cascode and last a single transistor output stage. This configuration has been chosen because of its ability to operate at very low voltages. The current reference is a standard current reference with the two PMOS transistors operating in weak inversion [4]. Inputstage Diff1 is operated a larger current than Diff2. This is to reduce noise and assure a total gain close to C_f/C_{mic}. The cascodes are operated close to V_{ss}. This is to assure that Diff1 can handle voltages as low as V_{ss} on its input. Outputstage is a single transistor bias by a current generator and Miller compensated by a capacitor. Bias input stage (Diff2) is connected to V_{dd} and Out. Resistors is chosen in such a way that the bias voltage at the output always is $V_{dd}/2$. Last the input is biased by two diodes of minimum size. This is two assure the best SNR. These diodes serve as protection diodes also.

V. Experimental Results

At present no experimental results can supplied. The amplifier has been submitted to chip fabrication and is expected to arrive medio November. A layout view of amplifier is showed in Fig. 7. The die consists of a fully integrated version plus a test version. A fully integrated ver-

sion is also being fabricated unbonded. This version is to supposed to be bonded to a commercial electret microphone.

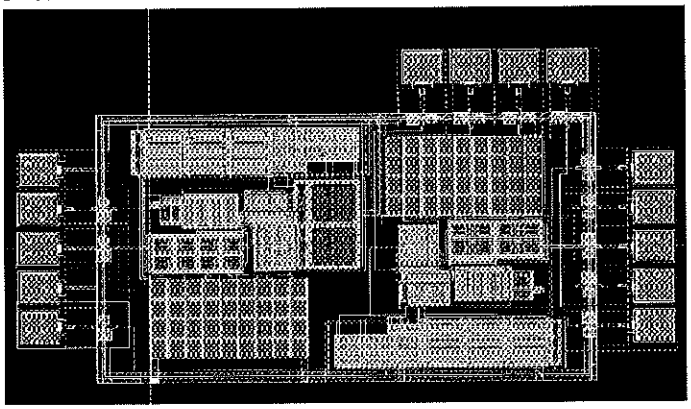

Fig. 7. layout view of amplifier plus test circuit.

As no experimental results are available we will have to rely solely on simulations. As SPICE MOST models overestimates the g_m of the transistors in moderate inversion. Simulation has been done keeping this in mind. But it can not at this moment be verified that the optimal gate area has been chosen. To obtain truly reliable simulations the best solution is to use the EKV model [3].

Fig. 8 shows a simulation of the gain A_{in} (top curve) and AC voltage across bias diodes (bottom curve) as a function of frequency. And Fig. 9 shows the PSRR .

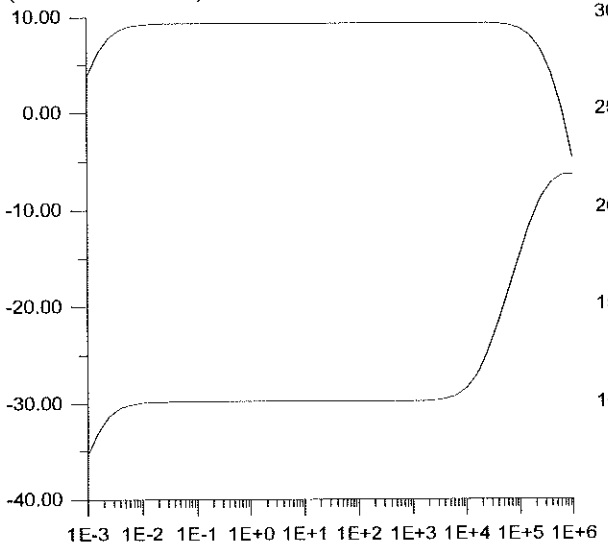

Fig. 8. Gain A_{in} (dB) as a function of frequency. And AC voltage (dB) across bias diodes.

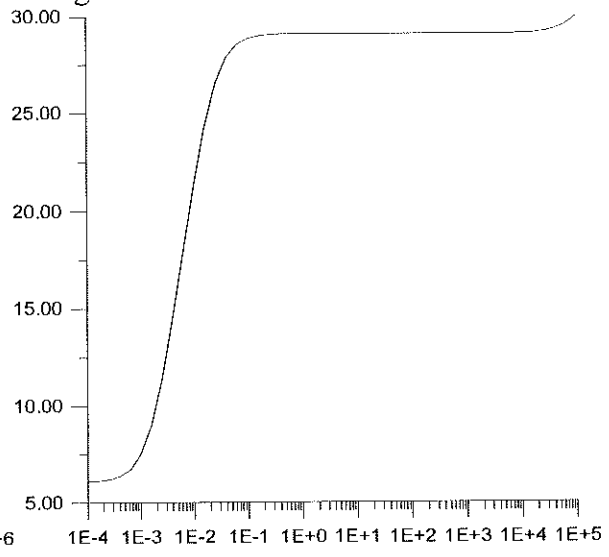

Fig. 9. PSRR (dB) as a function of frequency.

The gain A_{in} is as expected. An important feature off the amplifier configuration is that the bias diodes always is zero biased. This can be seen from Fig. 8, bottom curve. One sees that PSSR is equal to 6dB at low frequencies and then raises to 30dB in the audio range. The low frequency voltage at the output will always be equal to $V_{dd}/2$. If the supply voltage sinks, then the DC level at the output will follow thus assuring the best outputswing. This is very important in low voltage design. In the audio frequency band the gain A_{ref} is very low. So power supply variations are suppressed in this frequency band.

Below, in table 1. is summarised the simulated specifications for the amplifier

SNR(A) 10-10kHz	$4{,}75\mu V_{RMS}$ @ C_{mic} = 1.2pF and C_p = 1pF
PSRR 10mHz-	30dB
Current Consumption	30μA
Supply Voltage Range	1V-1.5V
Gain	9.3dB @ C_{mic} = 1.2pF and C_p = 1pF
Output Swing	$0.7V_{pp}$

Table 1. Simulated specifications of amplifier.

The PSSR might not seem impressive but it can easily be improved by cascoding. This will decrease the supply voltage range by 100mV-200mV. One would have to use a low threshold technology to preserve the supply voltage range.

VI. Conclusion

A preamplifier optimised for capacitive microphones with a very low source capacitance has been presented. It utilises a new design. A DDA is used to amplify the signal from the microphone. A special feature is an auxiliary input which is used to bias the output voltage level. This auxiliary input can be connected to V_{dd} thus assuring maximal outputsving under all conditions. This can be done without affecting the PSSR at audio frequencies. Or if desired the auxiliary input can be connected to a reference voltage. The preamplifier is implemented in a CMOS 0.7μm technology. Simulations shows that this solution is superior to the traditional junction FET solution concerning important parameters as SNR and outputsving. PSSR might not seem impressive but it can easily be improved by extra cascoding. This might require the use of a low threshold technology if the low voltage operation is to be preserved. Simulations are not yet experimentally verified. Expressions for optimal gatearea concerning noise are given. A chip has been sent to fabrication and is expected to arrive in November. Overall chip size is 1.7mm versus 1.1mm.

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A LOW-NOISE/LOW-POWER PREAMPLIFIER FOR CAPACITIVE MICROPHONES

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ABSTRACT

A design for a microphone preamplifier for application in hearing aids is presented. The amplifier operates at a supply of 1-1.5V, the current drain is 40μA. The maximum sound level allowed is more than 120 dB SPL (Sound Pressure Level), with a typical noise level of 25 dB(A) SPL (A-weighted). The amplifier is optimized for a capacitive microphone with a capacitance of 1.2pF. The amplifier is fully integrated in a 0.7μm n-well CMOS technology . Design details concerning noise performance are analytically described.

1. INTRODUCTION

Current capacitive microphones for hearing aids use an electret design for the microphone.An electret microphone represent a capa-citive source for the preamplifier. Due to the low frequencies involved, the fact that microphones is miniaturized and source capacitance is diminishing, a need for preamplifiers with a very low noise current is needed. Thus achieving acceptable signal to noise ratios. In traditional designs, a junction FET in a source follower configuration is used to buffer the signal from the micro-phone. Due to gate leakage current and the relatively low value of the bias resistor (1-10GΩ) the noise from a junction FET source follower can not be decreased. The value of the bias resistor can not be enlarged, because the leakage current imposes an upper bound. Other disadvantages of a junction FET source follower are, poor PSRR (Power Supply Rejection Ratio) and low output swing. In order to lower the noise current of the preamplifier, MOSFETS which show a negligible gate leakage current, can be used. Two zero biased diodes can then be used as bias resistors, obtaining very large equivalent bias resistance and at the same time serve as protection diodes. Based on this, a fully integrated preamplifier can then be designed to obtain a superior PSRR and full output swing. Traditional design obtain noise level of 27 dB SPL and maximum sound level of 110 dB SPL. PSRR in traditio-nal design is no more than 30dB.

Others have designed integrated preamplifiers for electret microphones [6,8]. So far no solution has been presented that could compete with the ordinary junction FET source follower addressing SNR (Signal to Noise Ratio).

2. AMPLIFIER TOPOLOGY

An electret microphone (Fig.1) consists of a capacitor which is charged by a permanent electric field. One off the capacitors plates acts as a diaphragm. The microphone can be represented as a voltage generator V_{mic} and a capacitor C_{mic} in series. The amplitude of the voltage generator is proportional to the incoming sound pressure. The proportionality constant, normally denoted the sensitivity, is usually in the range 5mV/Pa-20mV/Pa. The sensitivity used everyvere in this paper is 15.8mV/Pa.

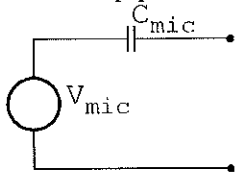


Fig. 1. Equivalent circuit for an electret microphone.

The amplifier topology used is a Differential Difference Amplifier (DDA) [5,9]. The amplifier topology is showed in Fig. 2 where C_{mic} is the capacitance of the microphone, C_p is the parasitic bonding capacitance and C_f is the feedback capacitance. The small signal resistance of the parallel diodes is denoted R_{diodes}. And last the V_{ref} is used to set the DC voltage level at the output. A block diagram of the DDA is showed in Fig. 3.

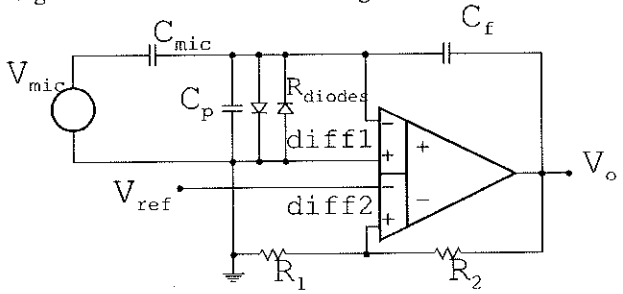


Fig. 2. Amplifier topology utilizing DDA.

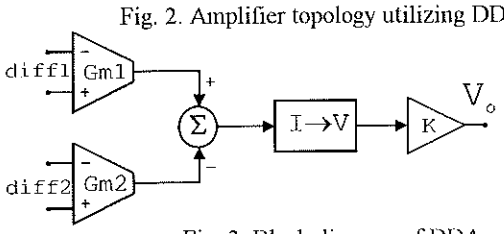


Fig. 3. Block diagram of DDA.

The DDA consist of two V→I converters (diff1 and diff2), a I→V converter and a gain k. Transconductances of diff1 an diff2 is denoted Gm1 and Gm2. Below the unity gain frequency of the DDA the transfer function from V_{mic} to V_o can be calculated to :

$$A_{in}(s) = \frac{V_o}{V_{in}} = -\frac{C_{mic}}{C_f}\frac{1}{1+\eta}\frac{s}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (1)$$

And from V_{ref} to V_o :

$$A_{ref}(s) = \frac{V_o}{V_{ref}} = (1+\frac{R_2}{R_1})\frac{\eta}{1+\eta}\frac{s+\omega_o}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (2)$$

Where

$$\omega_o = \frac{1}{R_{diodes}(C_{mic}+C_f+C_p)} \quad \text{and} \quad \eta = \frac{1+\frac{C_{mic}}{C_f}}{1+\frac{R_2}{R_1}}\cdot\frac{Gm2}{Gm1}$$

We see that it is desirable if $\eta \ll 1$. Then $A_{in}(s)$ equals the gain of a charge amplifier. And the gain $A_{ref}(s)$, will be very small above ω_o. $\eta \ll 1$ can be obtained by $C_{mic}/C_f \ll R_2/R_1$ and $Gm2 \ll Gm1$.

3. LOW-NOISE DESIGN OF INPUT STAGE

3.1. Configuration

The input stage chosen is a standard differential stage. The input stage corresponds to diff1 in the DDA. A differential stage is not the optimum choice for a low-noise design [2] but in this case it is convenient because the DC common mode voltage value, at the input diff1, can be set arbitrarily. In our case it is grounded. This would not have been possible with any other type of input stage.

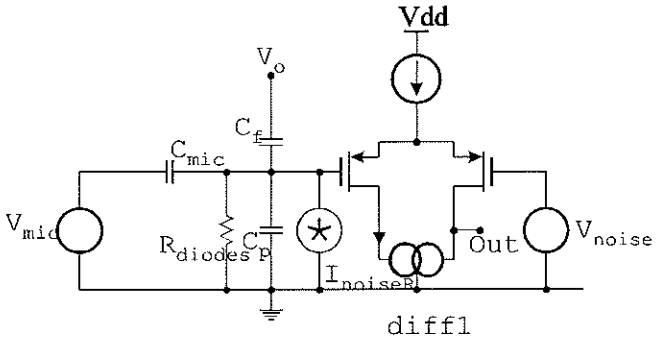


Fig. 4. Input stage configuration.

The noise from the input stage is represented by the noise voltage V_{noise} . This represents thermal noise and 1/f noise from the input stage. The bias resistor generated noise is represented by I_{noiseR}. We will in the following only consider frequencies above $1/2\pi C_{mic}$. In order to calculate the SNR we will refer the noise to the input. this can be calculated to :

$$V_{neqi}^2 = I_{noiseR}^2\frac{1}{(\omega\cdot C_{mic})^2} + V_{noise}^2\left(\frac{C_{mic}+C_p+C_f}{C_{mic}}\right)^2 \qquad (3)$$

In our case this noise voltage should be weighted by the A weighting function in order to obtain the SNR(A). The A weighting function is showed in Fig. 5. Input transistors are assumed to operate in weak inversion, possibly moderate inversion as resent measurements show that noise in PMOS transistors is due to mobility fluctuations and not carrier number fluctuations [1,7]. Therefore they should preferably be biased in strong inversion. If possible.

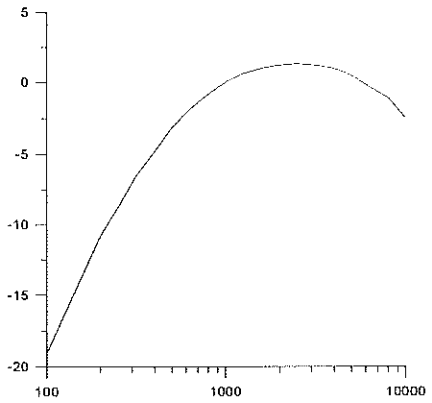


Fig. 5. A-Weighting Curve (-20dBre20μPa to +5dBre20μPa and 100Hz to 10kHz).

3.2. Minimisation of Input Transistor Noise

The noise from the input stage can be divided into three noise sources. Bias resistor white noise, white noise of input transistors and 1/f noise of input transistors. We will refer these to the input. First we define the following :

C_{ox} : Thin oxide capacitance pr. square.
I_d : MOST (MOS transistor) drain current.
K : Boltzmans constant $1.38\cdot10^{-23}$.
K_f : MOST 1/f noise parameter.
K_p : Transconductance parameter MOST.
L : MOST channel length.
L_d : Underdiffusion length.
T : Temperature in Kelvin.
V_t : KT/q = 26mV @ T=300°K.
W : MOST channel length.

3.2.1. Bias resistor generated noise

$$V_{neqiBiasres}^2 = \frac{4KT}{R_{diodes}}\frac{1}{(\omega\cdot C_{mic}))^2} \qquad (4)$$

As we see the noise from the bias resistor is moved to lower frequencies as the resistor gets larger. So it is advantageous that the bias resistor is as large as possible. The best way of implementing very large resistors onchip is to implement them as junction diodes. Two zero biased diodes will be as noisy as resistor with the Value of :

$$R_{diodes} = V_t/(2I_{leak}) \qquad (5)$$

Where I_{leak} = 10fA for a minimum diode. This gives us at theoretically value of R_{bias} = 1.3TΩ.

3.2.2. Transistor generated thermal noise

For the input referred transistor generated thermal noise, there exist an optimal gate area. This gate area gives minimal transistor generated thermal noise.

It is located at :

$$WL = \frac{C_p + C_{mic} + C_f}{C_{ox}\alpha} \text{ , Where } \alpha = 1 + 9L_d/2L. \quad (6)$$

And the minimal input referred transistor generated thermal noise is :

$$V^2_{neqitherm\,\min} = 4KT\frac{4}{3}\frac{L}{\sqrt{2I_dK_p}} \cdot \sqrt{\frac{C_{ox}\alpha}{C_p + C_{mic} + C_f}}\left(\frac{4}{3}\frac{C_{mic} + C_p + C_f}{C_{mic}}\right)^2 \quad (7)$$

3.2.3. Transistor generated 1/f noise

Again there exists a minimum. This is located at :

$$WL = 3\frac{C_p + C_{source} + C_f}{C_{ox}\alpha} \quad (8)$$

And the value associated with this minimum is :

$$V^2_{neqi1/f} = \frac{4}{3}\frac{1}{f}\frac{K_f\alpha}{K_p}\frac{(C_{mic} + C_p + C_f)}{C^2_{mic}} \quad (9)$$

3.3. Optimizing for lowest noise

As we see from equation 6 and 8, there exists two different optimal gate areas, where the thermal respectively the 1/f noise is minimal. The gate area for minimal 1/f noise is three times larger than the gate area for minimal thermal noise. The noise corner frequen-cy of the input transistors determines which gate area should be chosen. In this design, the noise corner is placed at a fairly low frequency. So I have chosen gate area for minimal thermal noise. Normally one would have to use numerically optimization using SPICE. But as SPICE MOST models underestimates thermal noise in moderate inversion this solution is not accurate. One solution is to use the EKV (Enz- Krummenacher-Vitoz) MOST model [3].

3.4. Minimisation of Total Noise

The total noise from the amplifier consist of contributions from the input transistors and from all other transistors. Having minimized noise from input transistor one should assure that contributions from all other transistors are negligible to those of the input transistors. This is easily done, keeping in mind, that the transconductance g_m of the input transistors should be larger than all other transistors. Input transistors gatelengths should be shorter than all other transistors.

4. OVERALL DESIGN

The schematic of the amplifier is showed in Fig. 6. It consists of 5 sections. A current reference [4], input stage (Diff1), bias input stage (Diff2), folded cascode and last a single transistor output stage. This configuration has been chosen because of its ability to operate at very low voltages. The current reference is a standard current reference with the two PMOS transistors operating in weak inversion [4]. Input stage Diff1 is operated at a larger current than Diff2. This is to reduce noise and assure a total gain close to C_f/C_{mic}. The cascodes are operated close to V_{ss}. This is to assure that Diff1 can handle voltages as low as V_{ss} on its input. Output stage is a single transistor biased by a current generator and millercompensated by a capacitor. Bias input stage (Diff2) is connected to V_{dd} and Out. Resistors are chosen in such a way that the bias voltage at the output always is $V_{dd}/2$. Last the input is biased by two diodes of minimum size. This is two assure the best SNR possible. These diodes serve as ESD protection diodes also.

5. EXPERIMENTAL RESULTS

The amplifier has been integrated with a 1.2pF capacitance simulating the microphone capacitance. Another version without the 1.2pF capacitance is being fabricated unbonded. This version is supposed to be bonded to a commercial electret microphone. At the moment only measurements on the version with a capacitance of 1.2pF has been performed.

5.1. Static Measurements

It has been verified that the amplifier can operate at a supply voltage of 1V-1.5V. The current drain was simulated to 30μA and measured to 36μA -40μA. The measured outputsving is approx. $0.5V_P$ at a supply voltage of 1.5V. This corresponds to a maximum input sound level of more than 120 dB SPL.

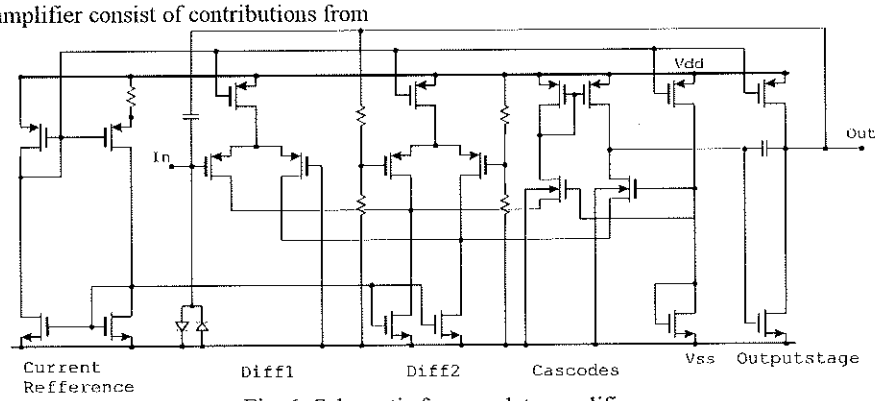
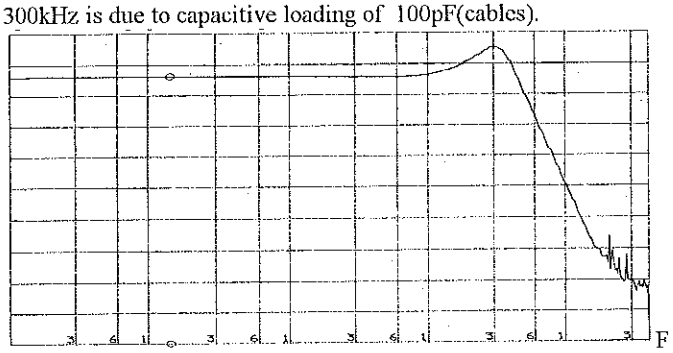


Fig. 6. Schematic for complete amplifier.

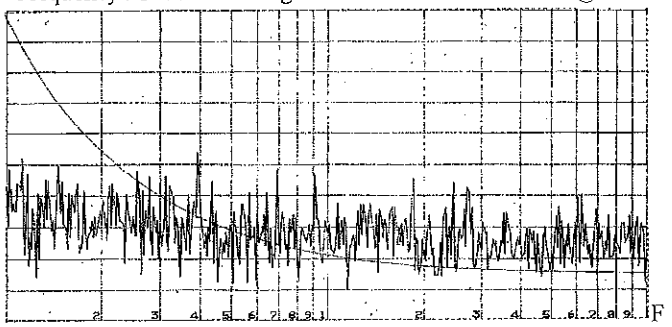
5.2. Dynamic Measurements

During the test of the amplifier it was noticed that when the amplifier was overloaded it saturated and returned to normal operation very slowly. This saturated state may last for several minutes. This can be explained as follows. When the amplifier is saturated, then the high impedant node at the input is charged. The only current discharging the node, is the leakage current of the bias diodes. As this current is very small, the discharging may take some time. Furthermore the dc gain from the high impedant node to the output is very large (approx. 300 times). This worsens the saturation problem. A solution is to enlarge the biasing diode leakage current a little, and to decrease the DC gain from the high impedant node to the output.

Gain has been measured to 2.96 ~ 9.42dB @ 1kHz.. This was simulated to 3.03 ~ 9.63dB @ 1kHz. Fig. 8 shows the measured gain A_{mic} as a function of the frequency. The peak located at 300kHz is due to capacitive loading of 100pF(cables).



ig. 8. Measured gain A_{mic} (dB) as a function of frequency. Frequency : 100Hz to 4MegHz. 5dB/div. Gain = 9.42dB @ 1khz.



ig. 9. Simulated and measured noise at the output of the ampli-fier. Frequency: 100Hz to 10kHz. Scale : 0nv to 800nv(Rms).

The noise at the output of the amplifier has been measured and simulated (fig. 9). This is worth a notice. The white noise level is approx. 6dB higher than simulated. It is at the moment not clarified why this disproportion exists. Some of the transistors are biased in moderate inversion and as SPICE overestimates the transconductance in this area, this might explain some of the difference between measurements and simulation. Simulation has to be done using the EKV MOST model [3]. This has not yet been done as this model level not is an integrated feature of SPICE.

The low frequency noise is much lower than expected. This is quite surprising. The noise corner is situated at a very low frequency (approx. 40Hz). This is though, only based on measurements from 10 samples of a single run. So while white noise is larger than expected the low frequency noise is smaller. The total noise level was simulated to 24B(A) SPL. And it was measured to 25dB(A).The frequency range was 100Hz to 10Khz.

6. CONCLUSION

A preamplifier optimized for capacitive microphones with a very low source capacitance has been presented. It utilizes a new design. A DDA is used to amplify the signal from the microphone. Expressions for optimal gatearea concerning noise are given. The preamplifier is implemented in a CMOS 0.7µm technology. Noise measurements differs from the simulations. White noise is larger and low frequency noise is smaller. This has not yet been explained. The total measured noise level is equivalent to 25dB(A) SPL. This compared with the maximum sound level allowed of more than 120 dB SPL gives us a dynamic range of 95dB at a supply voltage of 1.5V.

7. ACKNOWLEDGEMENTS

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A HIGH RESOLUTION SWITCHED CAPACITOR 1BIT ΣΔ MODULATOR FOR LOW-VOLTAGE/LOW-POWER APLICATIONS

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ABSTRACT

A high resolution 1bit ΣΔ modulator for low power/low voltage applications is presented. The modulator operates at a supply of 1-1.5V, the current drain is 100μA. The maximum resolution is 87dB equivalent to 14 bits of resolution. This is achieved with a signal-band of 5kHz, over-sampling ratio (OSR) of 128 and a sampling frequency of 1.28MHz. The very low power consumption is achieved by using a new type of efficient class AB amplifiers in a fully differential configuration. The modulator is implemented in a 0.7μm n-well CMOS technology. Optimisation details concerning modulator coefficients and bias requirement of amplifiers is described.

I. INTRODUCTION

Sigma Delta A/D converters has recently received much attention. These oversampled converter types solves many of the problems designers face designing A/D converters. As ΣΔ A/D converters are oversampled the need for antialiasing filters preceding the A/D converter is abandoned. This filtering is moved to the digital domain. The remaining analogue part is denoted the ΣΔ modulator. The digital filter is denoted the decimator and the to joined, ΣΔ A/D converter. In this paper a ΣΔ modulator is described. Why is ΣΔ A/D converters so interesting to VLSI designers ? As the digital domain is desirable for high resolution low power signal processing [9] it is obvious why as large a part of the signal processing should be done the digital domain. Furthermore multibit A/D conversion can be replaced by noise-shaped 1 bit conversion [6].This is especially interesting as 1 bit conversion is very easy to implement. In fact it can be implemented with a single comparator and a few switches. This dramatically reduces the matching requirements compared to traditional A/D converters. And it makes low voltage operation a lot easier.

II. MODULATOR TOPOLOGY

The implemented modulator is a 3rd order cascaded modulator type [6]. It consists of 3 integrators and a quantizer (fig. 1). It can showed [6] that the quantization noise at the output *Out* is exposed to a high pass filter function. While the transfer function *In* to *Out* is a low pass filter function. So the quantization noise is moved to high frequencies while a low frequency signal at the input passes unaffected to the output This phennonomen is called noise shaping [6].The coefficients a_1, b_1, b_2 and b_3 determines how the noise from the quantizer is shaped. Also the coefficients affect the stability of the modulator. The gains of the integrators G_1 ,G_2 and G_3 is used to scale the signal swing at the output of the integrators.

The stability is solely determined by the transfer function of the noise from the quantizer to the output of the modulator. This transfer function is called the noisetransferfunction, also denoted NTF. A higher order modulator has the ability to become unstable when the input exceeds a certain level. This level is called the Maximum Stable Amplitude (MSA). The 3rd order modulator has the advantage compared to a lower order modulator that noiseshaping filter function is steeper (steeper NTF, better SNR for a given OSR). However higher order modulators (number of integration's larger than 2) is often considered difficult to stabilise. This is not true. In this work the design strategy and methods from [6] is used. First the noise-transfer-function (NTF) is chosen as a butterworth filterfunction. The only free parameter then is the cut-off frequency which can be chosen to achieve the largest dynamic range. This achieved when MSA is chosen approx. to 0.45 times the quantizer level [6].

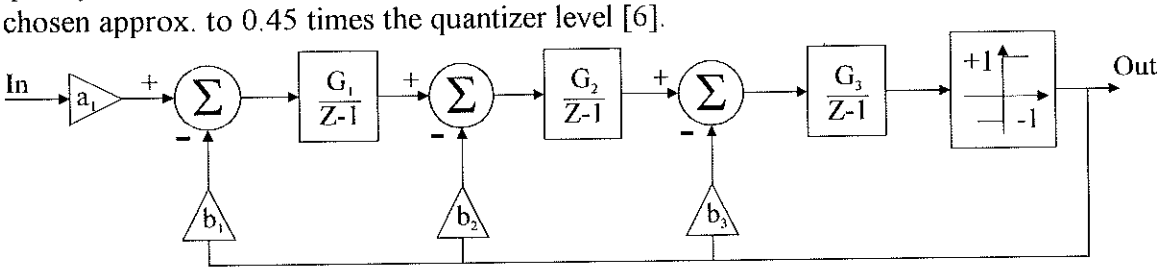

Figure 1. Topology of 3rd order ΣΔ- modulator.

This corresponds to a cut-off frequency relatively to the samplingfrequency of 0.095. A simulation of the output spectrum of the ideal modulator with a sine wave of 0.0052·fs at the input is shoved in Figure 2. The noise shaping is clearly seen in this figure.

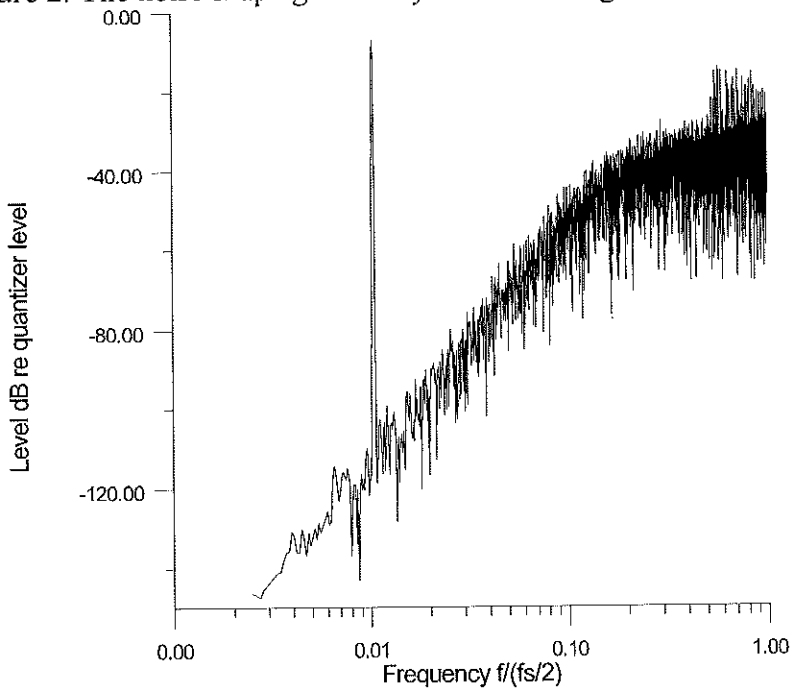

Figure 2. Output spectrum of the ideal modulator with a 0.0052·fs sinc wave input with amplitude of MSA .

The coefficients is : $a_1 = 1$, $b_1 = 1$, $b_2 = 0.6034$, $b_3 = 0.7862$, $G_1 = 0.1270$, $G_2 = 0.6666$ and $G_3 = 0.7500$. Signal swings on the output of the integrators has been scaled so that no clamping occurs while the amplitude of the input signal is below MSA. It is though desirable that clamping occurs when the signal amplitude exeds MSA. Otherwise the modulator will oscillate and the oscillation will continue even after the amplitude of the input signal is lowered below MSA.

III. Switched Capacitor Implementation Of Modulator

A. Amplifiers

As the modulator is intended for ultra low power applications it is important that the integrators settles with a minimum of current consumption. Therefore any compensation capacitor other than the load itself should be avoided [7]. This implies that the amplifier type used, should be single stage OTA's. In fig. 3 such a configuration is shoved. In the configuration of fig. 3 correlated double sampling (CDS) has been added by using a reset phase (phase 1) and a amplification phase (phase 2). The two phases are non-overlapping, with duty cycle 50%. The drawback of this clocking scheme is that the amplifier only is available during phase 2. Settling in the two phases is solely determined by the g_m of the OTA and the surrounding capacitive network. We will assume that the amplifier is class AB without slew rate limitations. The C_S , C_P , C_f and C_{load} are gain , parasitic , integration and load capacitance.

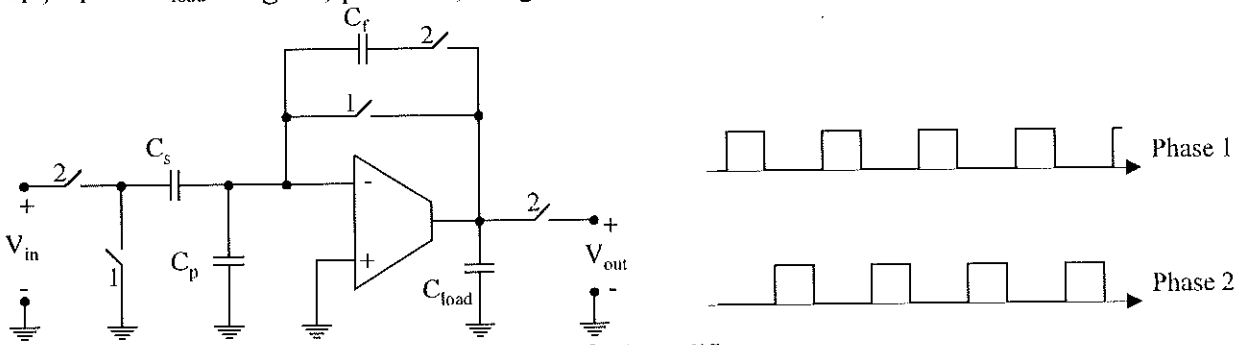

Figure 3. OTA amplifier

Amplifier settling and current consumption :

We will now calculate the settling time during phase 1 and 2 and the bias current needed. During phase 1 and phase 2 the time needed for settling T_s within an error band d is :

$$T_{s\varphi 1} = \frac{C_s + C_p + C_{load}}{g_m} \ln\left(\frac{1}{d}\right) \qquad T_{s\varphi 2} = \frac{C_{leff}}{g_m} \ln\left(\frac{1 + \frac{C_f}{C_{leff}}}{d}\right)$$

(1.a and 1.b)

Where C_{leff} equals $C_s+C_p+(C_f+C_s+C_p)\cdot C_{load}/C_f$.

As C_f and C_{leff} normally is given from noise considerations, T_s depends solely on the transconductance g_m of the OTA. So it is important that the g_m is as large as possible for a given current. An inverter with transistors operating in weak inversion is the optimum choice [7]. And the minimum bias current I_{bias} for the two phases is :

$$I_{bias\varphi 1} = \frac{n \cdot V_t}{2 \cdot T_s}(C_s + C_p + C_{load}) \ln\left(\frac{1}{d}\right) \qquad I_{bias\varphi 2} = \frac{n \cdot V_t}{2 \cdot T_s} \cdot C_{leff} \ln\left(\frac{1 + \frac{C_f}{C_{leff}}}{d}\right)$$

(2.a and 2.b)

Where n, V_t is the weak inversion slope factor and V_t equals 26mV. In [7] a thorough discussion on low power techniques is presented.

The switched inverter :

In order to achieve the largest possible g_m for a given current the amplifier has been implemented as a switched inverter [8], see fig. 4. The switching scheme resembles the one of fig. 3. All transistors are operated in weak inversion for maximum g_m/I_{bias}. In order to enlarge the low frequency gain, cascode transistors M2 and M3 has been added. The operation is as follows. During phase 1 the amplifier is biased and is not connected to the input signal. Transistor M5 biases the inverter during the biasing phase. Phase 2 is the amplification phase where it is connected as the amplifier of figure 3. As C_f is much larger than all other capacitors one sees from equation 2.a and 2.b that the bias current needed is approximately the same in phase 1 and 2. The switched inverter amplifier has the ability to operate at voltages just above the CMOS threshold voltage. As the switched inverter is a class AB circuit it has no slew rate limitations. The switched inverter is described in [1], [5] and [7].

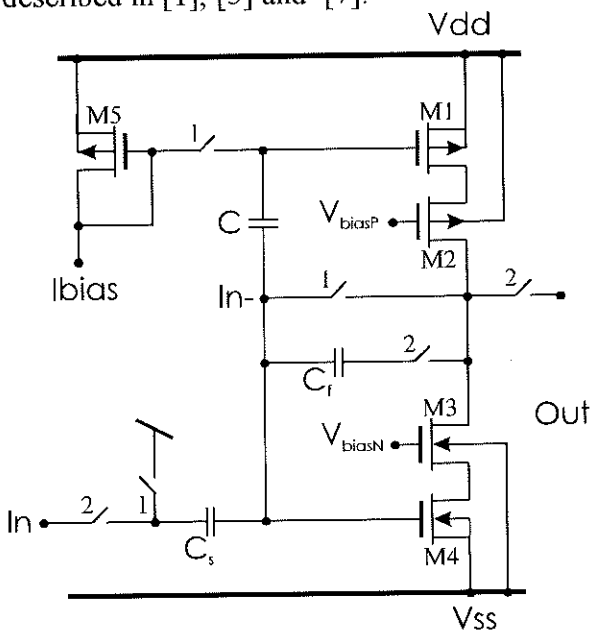

Figure 4. Switched inverter amplifier.

Switched inverter amplifier noise :

In sampled analogue systems the white noise from switches and amplifiers is under sampled and all of the avaylible noise power is folded within $-f_s/2$ and $+f_s/2$. Low frequency 1/f noise from transistors is not considered a problem as this is removed by CDS. Furthermore noise from switches is of minor importance compared to amplifier noise [5].

During phase 1 the noise is sampled onto capacitors C_s and C_p. In the following phase this noise is amplified to the output. The input referred noise contribution of phase 1 is :

$$\overline{V}_{nP1}^2 = \gamma \frac{kT}{C_s} \cdot \frac{\left(C_s + C_p + \frac{C_f \cdot C_{load}}{C_f + C_{load}} \right)^2}{C_s \cdot (C_s + C_p)} \qquad (3)$$

Where γ, k and T is n/2 (in case of a switched inverter amplifier), Bolzmans constant and temperature in Kelvin. In order to calculate the noise in the base band one has to divide by OSR. During phase 2 the equivalent input referred white noise has the rms. value of :

$$\overline{V}_{nP2}^2 = \overline{V}_{nP1}^2 \cdot \frac{C_s + C_p}{C_{leff}} \qquad (4)$$

Again one has to divide by OSR. In our case C_f is much larger than all of the other capacitors. So the two contributions is approximately equal. The theory of sampled noise is described in [3], [4] and [8]. Noise of the switched inverter is described in [5].

B. Integrators

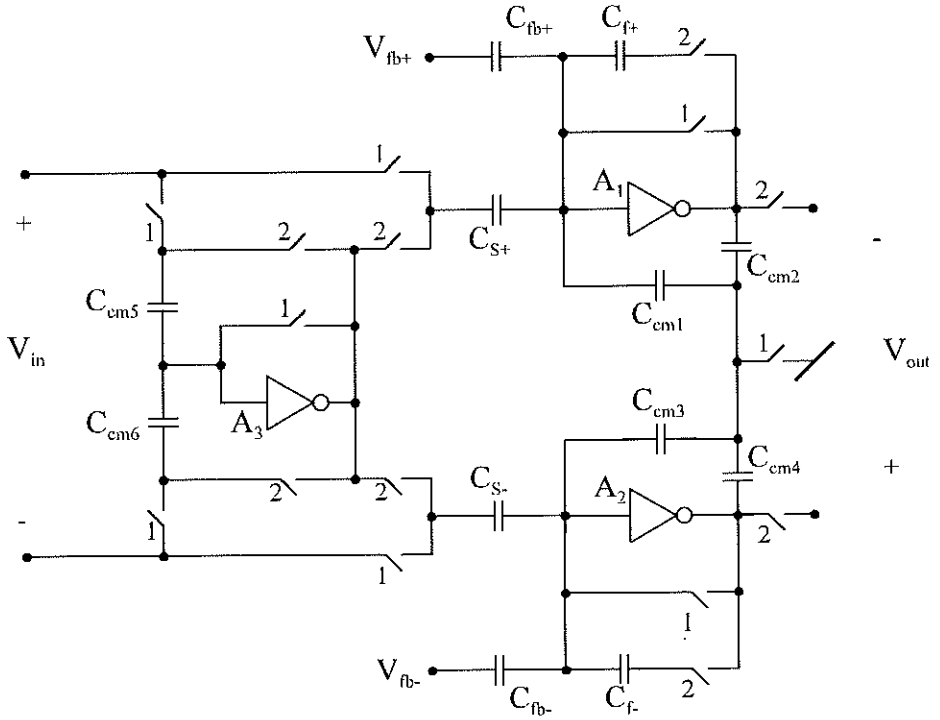

Figure 5. Principle schematics of integrators.

The largest problem associated with the switched inverter amplifier is the poor high frequency power supply rejection ratio PSRR. As the source of M1 is directly connected to V_{dd} the PSSR is only 6dB. CDS enhances the PSSR at low frequencies but unfortunately it also submerges frequency components around $f_s/2$ into the base band. The solution to this problem is to implement integrators as pseudo differential amplifiers with common mode feedback. Principle schematic of the integrators is showed in fig. 5. Switching phases resembles the ones of fig. 3. The two half parts of the integrator should match. C_{gain1} should match C_{gain2} and so on. In fig. 5 amplifiers A_1-A_3 is replaced by the core of the switched inverter of fig. 4. Common mode feedback is implemented by capacitors C_{cm1}-C_{cm4} . In case of complete matching these four capacitors does not affect the differential gain. But they sets the common mode gain to C_f/C_{gain} . As noise from the power supply is a common mode signal, it will be removed completely. That is, in case of complete matching. The common mode part of the input signal is removed by C_{m5} , C_{m6} and A_3. Noise from this part of the circuit does not affect the performance of the integrator as this noise contribution is common mode noise. If the biasing transistors (fig. 4, M5) are shared for A_1 and A_2 then their noise contributions will also be common mode noise. So the only transistors contributing to the noise is the input transistors of A_1 and A_2 . Low frequency 1/f noise from CMOS transistors, is removed by CDS.

C. *Comparator design*

The comparator is a design originally proposed by Krummenacher [2]. It implements the well known latched comparator, using switched inverters instead of the standard type inverters. This has the advantage that the minimum supply voltage is lowered to just above the CMOS threshold voltage. The switching scheme resembles the one of fig. 3.

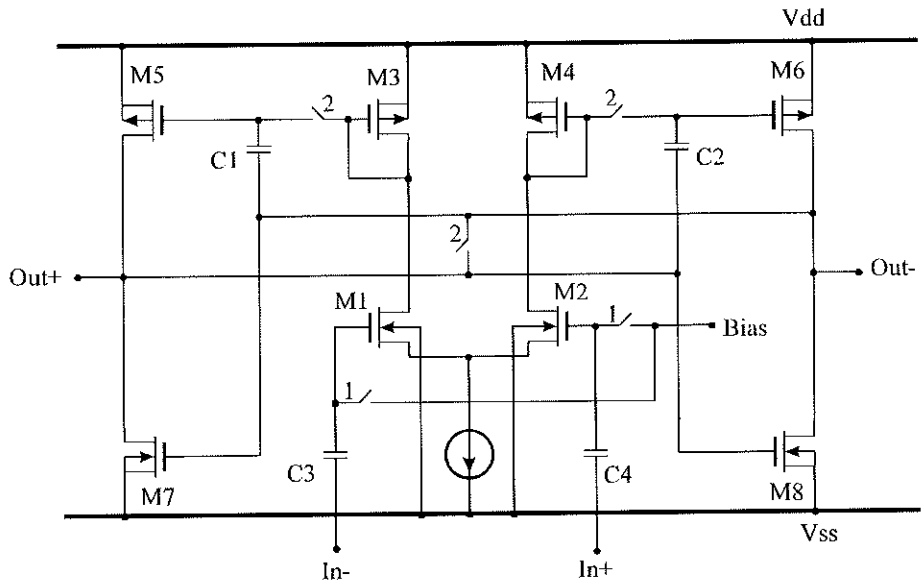

Figure 6. Low voltage comparator.

During phase 1 the common mode voltage of the input of the differential pair is set (M1 and M2). During phase 2 the signal is applied and the comparator is reset. In this phase an imbalance in the comparator is introduced. The current in one of the switched inverters is larger than in the other. When the comparator is released in phase 1 and the switches opens then the comparator flips to one of the sides.

IV. OVERALL DESIGN

Fig. 7 shoves the switched capacitor implementation of the modulator. Each of the integrators is implemented as the one of fig. 5. The comparator is implemented as the one of fig. 6. As the modulator is operated on a single supply the 1 bit D/A conversion can only achieve values 0v and V_{ref}. So an digital control block has been added. This controls the switching of the feedback capacitance's. If a feedback of $-V_{ref}$ is needed the feedback capacitance is switched to V_{ref} during phase 1 and then switched to Gnd during phase 2. If a feedback of V_{ref} is needed then the order is just the opposite. The voltage reference V_{ref} is a diodeconnected pnp transistor biased by a current source. Fast settling and low 1/f noise is main concerns. And a relatively large PSSR can easily be achieved. These issues is important as noise in the voltage reference is added directly to the signal without any suppression. The voltage reference is approximately 0.75V which means that MSA corresponds to a differential input voltage of 0.8V RMS. Delays of Z^{-1} has been introduced to realise the topology of fig. 1. Furthermore comparator plus digital control has a delay of Z^{-1}. As only noise from the first integrator plus the reference voltage is of importance, then integrator #2 and #3 can be noisier. The capacitance's used to realise coefficients a_1 and b_1 is chosen to 4 pF. This gives us a total calculated integrated white noise from integrator #1 and voltage reference of approx. 10μV RMS.

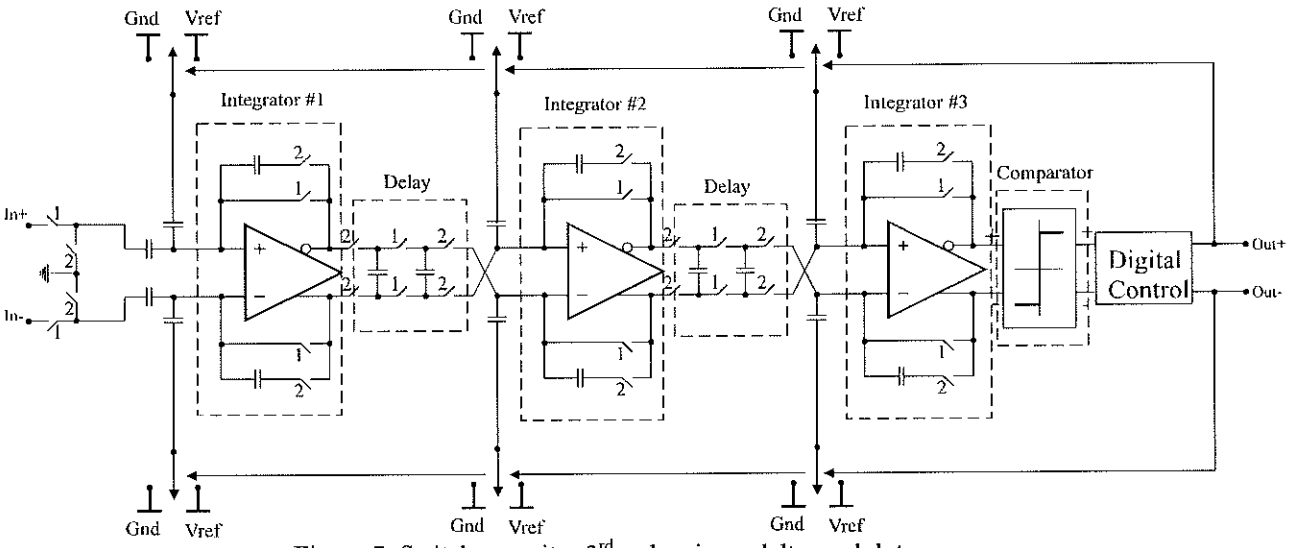

Figure 7. Switch capacitor 3rd order sigma delta modulator.

The bias current needed for integrator #1 and the voltage reference is 25μA and 50μA respectively. This assures that the first integrator and the voltage reference can settle within 0.39μ sec. This corresponds to the width of phase 1 and phase 2 where they are logic 'high'. The bias current requirements for integrator #2 and #3 is more relaxed as the noise from these are unimportant. The values of capacitance's in integrator #2 and #3 can be chosen smaller without affecting noise performance. Bias currents are set to 12.5μA in both. This reduces the power consumption significantly. The comparator and the digital control does not consume any power of significance. The main power consumers is integrator #1 and the voltage reference. The analogue part of the modulator is operated on a supply of 1.5V while the switches and the digital part is operated on 5V. This is to reduce power consumption without sacrificing performance . The use of different supply voltages requires level shifters [2]. If the modulator has to be operated on a single battery of 1.5V then a voltage tripler has to added. In [2] low-power oversampled A/D converters is treated thoroughly.

V. Simulation Results

At present no experimental results can be supplied. The ΣΔ modulator is presently being processed in 0.7μm CMOS process provided by MIETEC. Measurement results will be presented at the conference. Below, in table 1. is summarised the simulated specifications for the modulator. The simulation results is obtained by simulating the analogue circuitry in SPICE and the ideal modulator structure using MATLAB. The noise of the analogue circuitry simulated using ac analysis in SPICE. In this way the total input referred noise power can be found. The noise power in the base band can then be found by dividing by OSR. The result can be seen in table 1. The noise will though tend be to be higher than expected. This way of evaluating the noise performance do not take the cancelling of 1/f noise into account . Second order effects such as charge injection, coupling of noise through the substrate, PSSR, non-infinite amplifier gain and non-linear settling is not considered is these simulations of table 1. They are either to time consuming, can not be modelled in SPICE or are in this design very dependent on matching. A transient analysis in SPICE has been used to assure that the circuitry implemented corresponds to the modulator topology of fig. 1. Such a simulation do not give any clue of what the SNR of the modulator might be. This is because the transient analysis in SPICE do not take noise from switches and transistors into account. All second order effects tend to increase the noise.

Much attention has been offered in the design and layout phase in order to minimise these extra noise sources.

Maximum differential input signal MSA	$0.48V_{RMS}$
Analogue RMS noise voltage 0- 10kHz	$20.5\mu V_{RMS}$
Quantization RMS noise voltage 0 - 10kHz	-102dB re MSA ~ $3.8\mu V_{RMS}$
Total maximal SNR	87dB re MSA ~ $21\mu V_{RMS}$
Current Consumption	$100\mu A$
Supply Voltage Range	1V-1.5V & 5V(switches + digital part)

Table 1. Simulated specifications of modulator.

VI. Conclusion

A 3rd order switched capacitor $\Sigma\Delta$ modulator is presented. Overall chip size is 3.3mm versus 3.3mm. The modulator has been designed to have a maximum SNR of 87dB with a signal bandwidth of 5 kHz. The oversampling ratio is 128. The noise transferfunction is a butterworth highpass filter. Design procedure for finding the modulator coefficients are given. Furthermore a new fully differential switched amplifier is presented. The very low power consumption is due to this very efficient type of amplifier and the design strategy presented in this paper. Analytical expression of bias requirements and noise performance of amplifiers is presented. The total power consumption is as low as $150\mu W$. The modulator operates on power supply of 1.5V and 5V for analogue and digital part + switches respectively.

VII. Acknowledgements

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