OCP Based Adapter for Network-on-Chip

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Abstract

As technology improves, the number of transistors on a single chip is reaching one billion. This allows chip-designers to design complete systems on single chip with multiple CPUs, memory and analog circuits. With the large amount of resources available and with the demand for even shorter development time, reuse of intellectual property (IP) cores becomes inevitable.

Today a lot of effort is used to find an easy and efficient way, to let IP cores communicate with each other. A new topology in chip design is network-on-chip (NoC). With NoC the communication between cores can be standardized and traditional ad-hoc and/or bus-based solutions can be replaced with an on-chip network.

This thesis presents two network adapters for an asynchronous on-chip network. Our network adapters decouple communication from computation through a shared memory abstraction. We use Open Core Protocol (OCP) to provide a standard socket interface for connecting IP cores. The network adapters provide guaranteed services via connections and connection-less best effort services via source routing. The implementation of our network adapters has an area of $0.18mm^2$ and $0.13mm^2$ using a $0.18\mu m$ technology, and they run at a frequency of $225MHz$. A proposal for the improvement of synchronization between the synchronous and asynchronous domains is elaborated in this report, as studies have shown that the existing synchronization mechanism limits the throughput of the transactions and increases their latency.

Preface

This thesis has been carried out at the Computer Science and Engineering division of Informatics and Mathematical Modelling department at the Technical University of Denmark, from September 1, 2004 to February 28, 2005.

I would like to thank my supervisor Jens Sparsø for his guidance and support during this project. I would also like to thank Tobias Bjerregaard and Shankar Mahadevan for their help and for our interesting discussions. Thanks to Yoav Yanai for his critique and recommendations to improve this thesis. At last I want to thank my girlfriend for her great help and support, I love you very much.

Lyngby February 28, 2005

Rasmus Grødahl Olsen

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CHAPTER 1

Introduction

This chapter describes the background of the concept *network-on-chip* (NoC). The motivation for this project is discussed and a brief project description is presented. Finally, the structure of this thesis is described.

1.1 Background

As today's technology keeps advancing, the resources on a single chip grow. Chip design has moved to an era, where designers are no longer restricted by the available chip area. This leads to entire systems being designed on single chips. With the increase of the transistor count on a single chip and with an increased demand for even shorter time to marked, this means that there is a growing pressure toward design reuse. With the tendency to buy IP cores, the designer's task is moving from the building of individual IP cores toward system integration. IP cores can be regarded as "LEGO bricks" that are plugged together and the focus of system designer is shifted toward insuring that the system as a whole achieves the functional and non-functional requirements. In other words the reuse of IP cores spares the designer the need to "reinvent the wheel".

Traditionally, busses or ad-hoc interconnections have been used to communicate among cores. But with the increasing number of cores in a design, the number of busses and bridges also increases. This makes the design effort, scalability and testability much more complex[2, 5, 3]. A new paradigm for on-chip communication is the NoC, which takes the concept from traditional computer networks and applies it to on-chip communication systems. NoCs are the proposed solution to solve the design complexity of interconnections in large chip designs [2, 5].

NoCs are composed of routers and links which transport the data from one

destination to another, and *network adapters* (NA) which decouple communication from computation by providing the IP cores with a standard interface. This thesis will focus on designing and implementing a NA.

1.2 Problem Description

The challenge in designing a NA is the relation between the features, performance and cost. The design challenges are best described by comparing the two systems in Figure 1.1 and Figure 1.2. Figure 1.1 shows a bus based system (e.g., AMBA *Advanced Microcontroller Bus Architecture*) with a standard interface (e.g., OCP *Open Core Protocol*). Bus wrappers are translating OCP to the AXI (*Advanced Extensible Interface*) protocol, which is the protocol used by AMBA. This translation is very simple, due to the similarities in the OCP and AXI protocol specifications[12, 1], and mainly requires mapping corresponding signals. Figure 1.2 shows the system where the bus and bus wrapper are replaced with a network and NA. The challenges for the NA are to translate OCP to network packages without a too high cost in terms of area and power consumption, compared to the bus wrapper, and at the same time provide the services from the network to ensure performance.

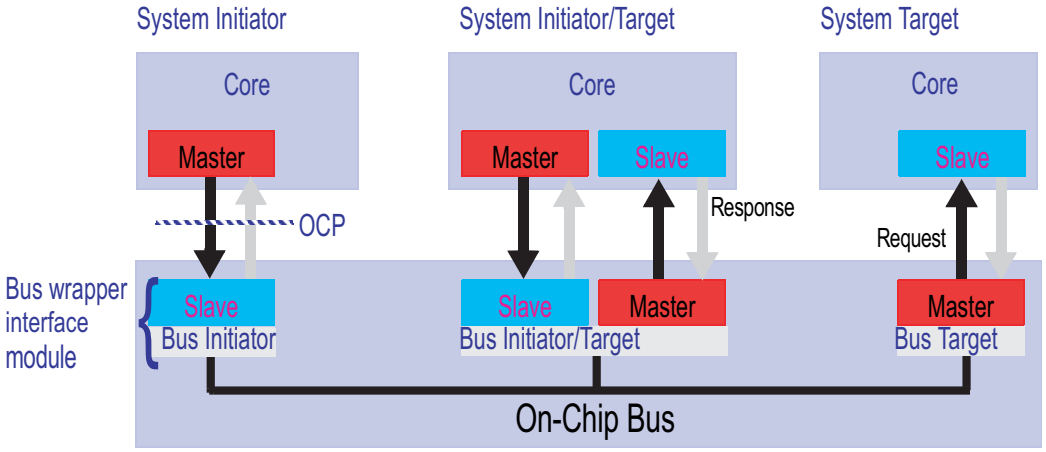


Figure 1.1 *Bus based System*

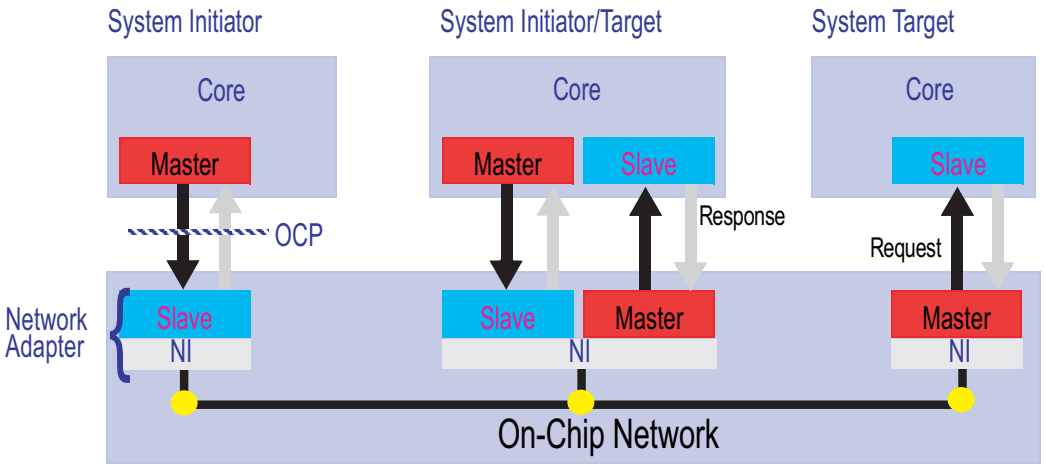


Figure 1.2 *NoC based System*

1.3 Objectives

The objectives of this thesis are:

1. Make an analysis of the requirements for a network adapter working in a System-on-Chip environment.
2. Design and implement a network adapter which provides a standard socket using OCP 2.0 that connects a IP core to the MANGO network. Resolve the synchronization issues between the synchronous IP cores and the asynchronous network.
3. Verify that the network adapter is OCP compliant.
4. Make a cost and performance analysis of the network adapter to provide technical data for comparison with similar designs.

1.4 Thesis Overview

The rest of the thesis is organized as follows:

Chapter 2 describes the architecture of the MANGO NoC, which is the target network for the network adapter in this project.

Chapter 3 analyzes the requirements of the network adapter. This is done in

order to address the key issues for system design and implementation.

Chapter 4 presents the system specifications of the NAs for the MANGO network.

Chapter 5 provides a detailed design and implementation of the network adapter.

Chapter 6 and 7 present the validation and synthesis results.

Chapter 8 discusses the topic which we believe are likely to undergo future improvements as well as making some suggestions for such improvements.

The final chapter is a summary and conclusion.

CHAPTER 2

The MANGO Network-on-Chip

In this chapter we will introduce the MANGO (*Message-passing Asynchronous Network-on-Chip providing Guaranteed services through OCP interfaces*) NoC, which is in development at the *Technical University of Denmark* (DTU).

The MANGO NoC is a packet switched, asynchronous network, which emphasizes a modular design architecture. It is suitable for the GALS (*globally asynchronous locally synchronous*) concept, where small synchronous islands are communicating with each other asynchronously.

2.1 MANGO Characteristics

2.1.1 Message Passing

As mentioned before, the MANGO NoC is a packet switched network. The packet switching is based on abstraction layers and protocol stack, where each component in the system implements a stack layer. The MANGO consists of three abstraction layers: the core layer, NA layer and network layer (see Figure 2.1). They work together to form the MANGO protocol stack.

The control is passed on from one layer to another when moving up and down in the protocol stack. When moving down a data unit is always encapsulated as payload and applied with a new header, and when moving up a data unit is decapsulated by discarding the package header from previous layer. Figure 2.2 shows how the MANGO protocol stack is mapped into the OSI (*Open System Interconnection*) reference model.

Core Layer - This layer is where the IP cores reside. Applications running on the IP cores communicate messages among each other using the underlying

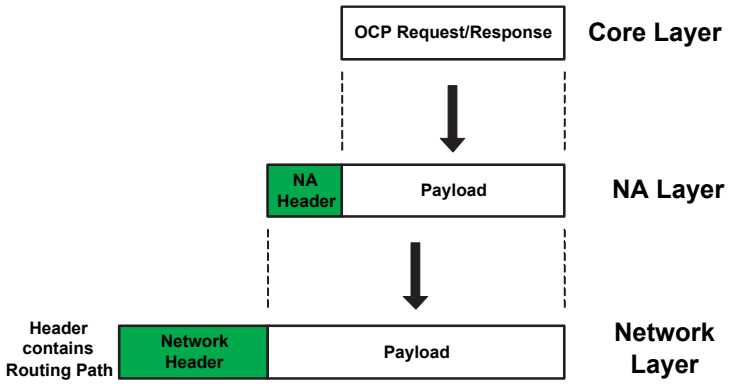


Figure 2.1 *MANGO Abstraction Layers[19]*

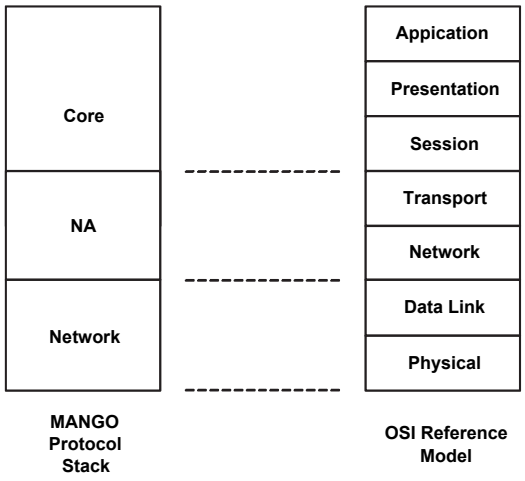


Figure 2.2 *MANGO Protocol Stack Map to the OSI Reference Model[19]*

layers.

NA Layer - This layer is where the NAs reside. They provide the high level communication services based on the primitive services in the network layer.

Network Layer - This is where the routers and links reside. Routers perform the transferring of the over the physical links in the network.

2.1.2 Services

The MANGO network provides the IP cores with two types of services:

Guaranteed Services(GS) GS are connection-based transactions where virtual point-to-point connections are established between NAs. Since the trans-

action is connection-based the packages can be sent without headers. The MANGO provides guarantees for worst case latency and throughput services.

Best Effort Services(BE) BE services are connectionless and routed in the network using source routing. The routing path is applied to the package header by the NA before it is sent in the network. The network does not give any performance guarantees, only completion guarantees.

2.1.3 Distributed Shared Memory

The address scheme in MANGO uses a shared memory distribution, where the address space is distributed evenly among each IP core and component in the network (i.e. network adapters and routers). This decouples communication from computation and makes the communication between IP cores independent from the network implementation.

2.1.4 OCP Interfaces

The MANGO provides a standard socket interface through OCP, where IP cores can be connected to the network in a “plug and play” style. The OCP offers communication features of a high abstraction level such as bursts, threads, connections etc.

2.2 MANGO Architecture

The network components that constitute MANGO are routers, links and NAs. IP cores are connected to the network via the NAs (see Figure 2.3).

2.2.1 Routers

Routers implement a number of unidirectional ports. Two of them are local ports which consist of a number of physical interfaces that connect the NA to the network. Packages are transfered in the network using wormhole-routing. This means a package can span over several routers on its way through the network. Internally, the router consists of a BE router and a GS router. The BE router routes BE packages based on the routing path defined in the package header. The GS router routes header-less GS packages using programmable connections, which

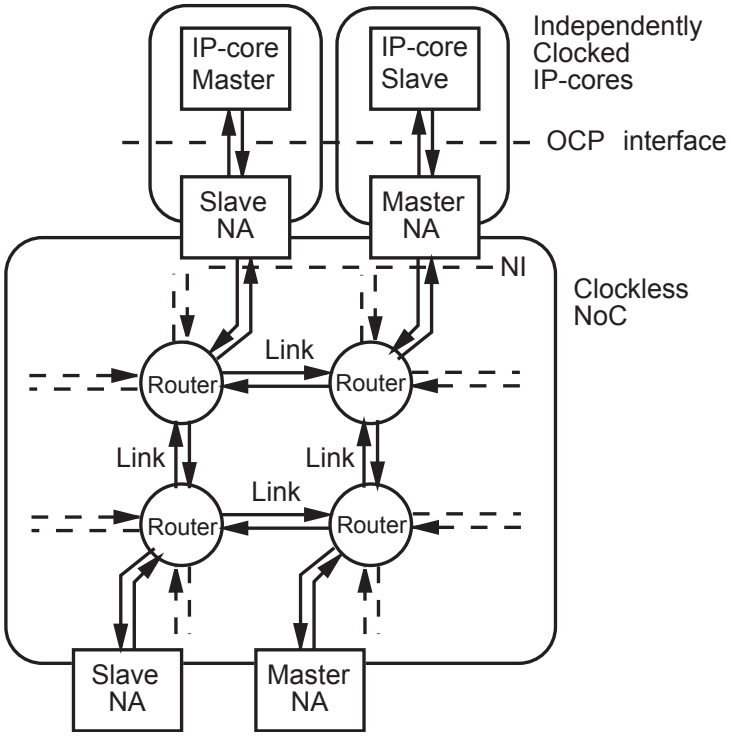


Figure 2.3 *MANGO Architecture[4]*

are logically independent of other network traffic activities. For a detailed description of the router architecture see [4].

2.2.2 Links

Links are the interconnections between routers. They connect the routers to form the network. They are unidirectional and implement a number of virtual channels by time-multiplexing the *flow-control units* (flits) sent on them. To maintain high throughput, long links can be pipelined.

2.2.3 Network Adapters

NAs provide the IP cores with easy access to the network services. They also provide a standard socket interface through OCP, and a high level of abstraction through shared memory distribution. The NAs combine the synchronous IP cores together with the asynchronous network, by performing the synchronization on the *network interface* (NI) which is the interface between the NA and the router.

CHAPTER 3

System Analysis

In this Chapter we will list the requirements of the NAs in relation to IP cores communication demands in a *system-on-chip* (SoC) design. Based on the requirements we will analysis the implementation complications that arise thereof. Finally, we will summarize the discussion and present the scope for the NAs' specifications.

3.1 Requirements

To describe the system, this section specifies the requirements of the NAs. The requirements can be seen as a contract that states what the system should do. It is used during the system analysis, design, implementation and test phases. The key words "**must**", "**should**" and "**may**" used in the following statements are to be interpreted as the level of importance.

3.1.1 General Requirements

Most ASIC designs share the same main requirements such as low cost, high performance, flexibility and scalability. Flexibility means that different scenarios **should** be taken into account. Scalability means that extra features and services **may** easily be applied to the design, thereby promoting change management and reducing time to market of new and enhanced products.

3.1.2 OCP Features

1. The OCP **must** provide the IP cores with read and write requests.
2. The OCP **should** provide the IP cores with burst transactions.

3. The OCP **should** provide the IP cores with split transactions.
4. The OCP **should** provide the IP cores with interrupts.
5. The OCP **may** provide the IP cores with readlink, readexclusive, writenon-post and writeconditional requests.

3.1.3 Services

1. The NAs **must** apply access for the IP cores to the network's services.
2. The NAs **should** differentiate the traffic from the network based on service type.

3.1.4 Performance

The NAs **should** meet the performance requirements of different traffics shown in Figure 3.1.

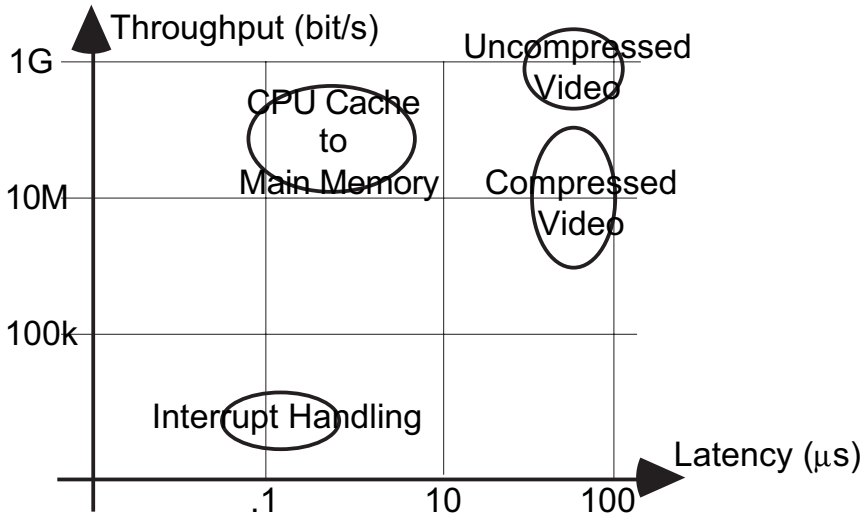


Figure 3.1 *Requirements for Different Traffics[11]*

From Figure 3.1, we can see the latency should meet the requirement for interrupt handling and the throughput should meet the requirement for uncompressed video.

3.2 Implementation Complications

In this section we will look at requirements listed in section 3.1 and discuss the possible solutions and the cost of implementing them in the NA. The result of this discussion will lead to the specification in chapter 4.

3.2.1 Slave NA and Master NA

In order to exploit the advantages by reusing modules, the network adapter needs to match the requirements to a wide range of IP cores. IP cores can generally be divided into three groups: i) Masters (e.g., CPUs, DSPs, etc.). ii) Slaves (e.g., memory, I/O devices, etc.). iii) Master/Slaves (e.g., bus controllers, etc.).

Masters are “active” cores which request services from the slaves while slaves are “passive” cores which respond to their masters request. Masters/Slaves are a hybrid between the two.

There is an unnecessary waste of hardware resources by implementing a NA to provide the services for both masters and slaves. The reason for this is because a network adapter is needed to be instantiated for each IP core that is to be connected to the network. In order to meet the requirements of a master/slave and at the same time avoid unnecessary redundancy, we split the NA design into two, Slave NA and Master NA. Slave NA is for matching the requirements of master cores, and Master NA is for matching the requirements of the slave core.

In the rest of this thesis the term Slave NA refers to a master core’s NA, while the term Master NA refers to a slave core’s NA. NAs refer to both Master NA and Slave NA.

3.2.2 Services

The Slave NA should keep track on which services that are available for an IP core. (i.e. which services have been setup for its IP core).

There are two types of services available in the MANGO network, GS and BE. GS are connection based. They need to be setup by writing to the address spaces of the routers and NAs, which will constitute the connection in the network between the source core and destination core. BE services are connection-less and are setup by applying the routing path (i.e. direction to routers on how to route a package) to the source NA.

Every request sent on the network will have a response (i.e. due to the OCP configuration chosen). A request and a response do not need to use the same service type. This gives four scenarios for which a service can be setup. The scenarios should be read as [*service used for request → service used for response*], where the request service is configured in the Slave NA and the response service is configured in the Master NA.

1. **BE→ BE:** The routing path is stored in the Slave NA and the Master NA can calculate the return routing path from the original routing path.
2. **GS→ GS:** The connection for transmitting the request is stored in the Slave NA and the connection for transmitting the response is stored in the Master NA.
3. **GS→ BE:** The connection for transmitting the request is stored in the Slave NA and the routing path for transmitting the response is stored in the Master NA.
4. **BE→ GS:** The routing path for transmitting the request is stored in the Slave NA and the connection for transmitting the response is also stored in the Slave NA and sent with the request in the package header to the Master NA. This is for the Master NA to distinguish between the BE → BE and BE → GS service.

In the rest of this thesis the following terms apply: BE service means a BE → BE, GS means GS → GS or GS → BE or BE → GS unless other is specified.

3.2.3 BE Package Transmit buffer

The network is routing BE services using wormhole routing. If a BE package is stalled in the network, it can stall several routing nodes, which depends on the BE package's package-length. In worst case a long BE package (i.e. a burst transaction) can stall the routing nodes through its routing path all the way back to the NA. In this case it can block the interface between the core and the NA. This prevents the core from transmitting. It is unfortunate to have BE traffic that can block guaranteed services.

To prevent the interface from getting blocked by BE packages, the BE packages should be buffered in the NA before it is transmitted over the network. In this way it's possible to let GS packages be sent before BE packages, when the BE packages are blocked in the network.

Since there is no maximum package-length, buffering of burst-writes needs a very large buffer. The resource expense for this is too high. Therefore the

application developer needs to keep in mind if bursts are sent using the BE service, they can block the interface when congestions occur in the network.

To make the NA flexible to the connected cores, the buffer size for BE packages can be determined by the NA user to match his design requirements. In this case the longest BE package can be sent without risking of blocking the interface.

In our design we have chosen a buffer depth of four. This matches the longest packages, which are not bust packages.

3.2.4 BE Packages Routing Path

The MANGO network routes BE packages by using source routing (see Chapter 2). When using source routing the NA needs to apply the full routing path to the package header before the package is sent.

If the network is homogeneous, an algorithm calculates the full routing path to any address in the network. But if the network is heterogeneous, it gets more complicated to determine an algorithm and implement it. Therefore a look-up table containing routing path to some of the cores is applied instead of an algorithm.

In a small network the look-up table can easily hold all the routing paths to the cores. In a larger network a core will not communicate will all other cores, therefore the look-up table only needs to hold the necessary routing paths.

The look-up table can be either dynamic or static. The dynamic look-up table functions like a cache. If a cache miss occurs, the table will be updated with a new routing-path.

A static table can be implemented as a ROM. This means the table contains all the predefined routing paths for specific applications. The table is read only and cannot be updated. If the application is changed the table may not be suitable anymore.

In our project we have chosen to implement the look-up table as a RAM, which is more flexible than a ROM, since it is possible to reinitialize the table for different applications. Compared with the dynamic table the flexibility is similar, except RAM doesn't have the cache functionality. The cache functionality may not be practical in a real system, due to the increased latency on transactions where a cache miss occurs.

3.2.5 Scheduling of Incoming Packages

The NI has several ports to transmit and receive packages. When receiving incoming packages on multiple ports simultaneously, some kinds of scheduling need to take place. Master cores can receive multiple responses if they make use of the threading capability in the OCP interface. Slave cores can receive multiple requests issued from different master cores. The scheduling can either be done by packages or bandwidth. Since a package contains a full OCP request or response, and the OCP specification does not support interleaving, a full package needs to be processed at a time. Bandwidth scheduling is done by a round-robin algorithm. There are several algorithms to choose from. Every one has its own advantages and disadvantages. Typically, a round-robin algorithm uses input buffers. Large buffers are very area consuming, which is not ideal for our design.

Package scheduling can be done by a simple state machine. Different priorities on BE and GS ports can be resolved with counters.

3.2.6 Synchronizing the NA and the Network

To transfer data from the synchronous domain (i.e. the NA) to the asynchronous domain (i.e. the network), control signals from the network need to be synchronized.

To make a safe synchronization of the *four phase handshake push protocol* (see section 4.1.2), a push synchronizer with two flip-flops should be used[8].

The important thing is to sample the asynchronous control signal from the network two times. The second sample is made to reduce the possibility of evaluating the wrong value of the first sample. This can occur if the flip-flop enters metastability or if the signal has a long delay[7].

With a two flip-flops synchronizer, the *mean time between failures* (MTBF)(i.e. the possibility of evaluation the wrong value when synchronizing) can be calculated by using Equation 3.1[7].

$$MTBF = \frac{e^{T/\tau}}{T_w f_c f_i} \tag{3.1}$$

Here f_c is the sample frequency , f_i is the data arrival frequency, τ is the exponential time constant of the rate of decay of metastability, and T_w is a related to the setup/hold window of the synchronizing flip-flop.

τ and T_w parameters are technology dependent and need to be measured. Since we do not have the parameters for the implemented technology, we used the parameters cited in [8], which refer to a $0.18\mu m$ technology, and added thereof 300%. This assisted us in making an educated guess as to worst-case scenarios. We used $T_W = 400ps$ and $\tau = 40ps$. Table 3.1 shows the MTBF for different sampling frequencies and with a data arrival rate of $4 \times f_c$. It can be seen that increasing the sampling frequency decreases the MTBF drastically. The same applies if τ and T_W are changed. For these reasons, the values included in Table 3.1 should only be considered as a guess.

$f_c[MHz]$	MTBF [years]
100	$1.19 \cdot 10^{95}$
200	$1.53 \cdot 10^{40}$
500	$1.38 \cdot 10^{12}$
1000	549

Table 3.1 *MTBF for Synchronization*

It is also important that the output control signals to the network are maintained free of any glitches. This can be ensured by taking the output value directly from a flip-flop.

Synchronization does incur a penalty in terms of latency, but cannot be excluded. Because without it, we cannot ensure correct system behavior. The synchronization will add to the latency of the system and will reduce its throughput.

3.2.7 OCP Features

To comply with the requirements from section 3.1, more advanced transaction commands need to be supported (i.e. Burst read/write and commands to use with direct memory access). All these commands are directly supported through the OCP interface.

3.2.7.1 Burst Transactions

The advantage gained by using burst transfers is that the bandwidth is used more effectively, since it is only necessary to send the starting address together with some information about the burst. The longer the burst is the better ratio between data and overhead gets. Another advantage is that the jitter between data flits

decreases when adding a burst header to the package, since many flits of data can be sent in sequence.

To take advantage of burst transactions the NA needs to package a burst in a package to transmit over the network. However, if a very long burst is packaged into one package, the burst can block a slave core from receiving request from other cores. This is because the NI between the NA and network narrows down to one connection, and the OCP interface from the NA to the core cannot time-multiplex the requests to generate virtual channels, such as the MANGO network is capable to do. This means that switching of request at the NI can only be done per package. The blocking of a slave will not affect the network regarding to GS, since it is a virtual connection, which will not block routing paths and connections to other cores. But if a burst-write request is sent to a slave using BE and this request is blocked by the slave, it will block the routing nodes in its routing-path and then block for other BE traffic to other cores.

To resolve this problem the application designer needs to avoid using BE when transmitting long burst packages.

3.2.7.2 Split Transactions

In the OCP interface threaded transactions refer to split transactions. Threaded transactions allow the core to use the network more efficiently by allowing the core to have multiple transactions running simultaneously. This feature will not be used by cores which do not support split transactions. Therefore, the complicated task to make account of the transactions should be handled by the IP cores.

3.2.7.3 Interrupt Handling

There are many different methods to implement interrupt, however the scope for this project will only be to implement a single interrupt as a virtual wire. How advanced interrupt handling should be done in a NoC can be a future work.

3.2.8 Implementation Issues/Trade-offs

Until now chip designers have considered interconnection on chip as free. But as today's chips become more and more complex and entire systems are integrated on a single chip, interconnections become more complex. Therefore, compared to the overall design the NoC should take up very few resources in relation to area

and power. As the NA is a part of the NoC, these design considerations should also apply for designing NA.

3.2.8.1 Area and Power

The area of the NA should be reasonable in size, compared to the cores connected to it and compared to the system design.

Functionalities take up area[19]. Features that are complicated to implement usually take up area. So we must always keep in mind that a feature should be implemented based on the necessity and cost.

Buffer-size has been shown to be an important factor on the area utilize by the design (see [6] and [19]). Since the network behaves as a large buffer, we should keep the buffer-size in the NA at minimum and instead try to utilize the buffer-space in the network.

3.2.8.2 Performance

When defining performance for a network there are three important parameters: throughput, latency and jitter. The throughput in the NA needs to match the throughput of the interface to the core connected, otherwise the NA becomes the bottleneck in the design.

The latency in NA should be small. The latency for a message will be two times the latency of the NA plus the latency of the network. Therefore, a small latency in the NA is important. Another important factor is the synchronization between the NA and the network. The time for making the synchronization is always added to the latency and jitter.

3.3 Setting the Scope for the Network Adapter

In this section we list the key implementation issues based on the requirements listed in section 3.1. The key implementation issues listed below and the requirements will be used in next chapter as the basis for the system specification.

Scheduling: Scheduling scheme based on a simple Round Robin algorithm. GS ports have equal priority and BE ports have lowest priority.

BE routing: A RAM look-up table to contain the routing-path for the application. The possibility to reinitialize the table between applications.

Burst transactions: The NA should support burst commands. There is no restriction on the burst-length, but the application developer should avoid transmitting long burst by using BE.

Split transactions: Support split transactions by using OCP threading.

Interrupts: Using a virtual wire from slave to master to set and clear an interrupt.

DMA commands: Support for *direct memory access* (DMA) commands (i.e. read-exclusive, read-link and conditional-write OCP commands).

CHAPTER 4

System Specifications

The system specifications are a strict guideline of essential aspects in the design. They will ensure that the system fits into the overall system design. In this Chapter we describe the system specifications for the Slave NA and Master NA. The system specifications should be used in the design phase of our project, and also can be used as a reference by the system and application developers who are using the NAs in their systems.

Our system specifications are divided into five parts; interface specifications, network service specifications, memory map specifications, package format specifications and system flexibility specifications.

4.1 Interfaces Specifications

The NA should provide two interfaces. One connects the NA to a core, which we name as *core interface* (CI); another connects the NA to the network, which we name as *network interface* (NI).

4.1.1 Core Interface

The CI must use the OCP v2.0[12]. OCP is a standard socket that allows two compatible cores to communicate with each other, using a point-to-point connection.

4.1.1.1 OCP Configuration

The OCP signals and their configurations used in our project are summarized in Table 4.1 (CI signals of Slave NA) and Table 4.2 (CI signals of Master NA). Signals whose width is configurable should be implemented as generics in VHDL.

So it allows the designer to customize the instantiation of each NA, to match the connected core's requirements. In our project the configurable signal widths are configured to the values which are written in parentheses.

Group	Name	Width	Driver	Function
Basic	Clk	1		OCP clock
	MAddr	configurable (32)	master	Transfer address
	MCmd	3	master	Transfer command
	MData	configurable (32)	master	Transfer data
	MDataValid	1	master	Write data valid
	SDataAccept	1	slave	accept write data
	SCmdAccept	1	slave	accept command
	SData	configurable (32)	slave	Transfer data
	SResp	2	slave	Transfer response
Burst	MBurstLength	configurable (8)	master	Transfer burst length
	MBurstSeq	3	master	Transfer burst sequence
	MReqLast	1	master	Last write request
	MDataLast	1	master	Last write data
	SRespLast	1	slave	Last read response
Threads	MConnID	configurable (2)	master	Connection identifier
	MThreadID	configurable (3)	master	Request thread identifier
	SThreadID	configurable (3)	slave	Response thread identifier
	MDataThreadID	configurable (3)	master	Write data thread identifier
Sideband	SInterrupt	1	slave	Slave interrupt

Table 4.1 *CI Signals of Slave NA*

In the following part we give some explanations for the contents of the tables 4.1 and 4.2.

4.1.1.2 Basic OCP Signals

The CI should be able to handle single *write*, *write-non-post*, *write-conditional*, *read-link* and *read* OCP commands. Therefore, the CI needs to use the basic OCP signals such as `MCmd`, `MData`, `MAddr`, `SCmdAccept`, `SResp` and `SData`[12]. In our project we interpret the `MAddr` from bit 31 down to 24 as "global address" and bit 23 down to 0 as "local address". The "global address" determines the

Group	Name	Width	Driver	Function
Basic	Clk	1		OCP clock
	MAddr	configurable (32)	master	Transfer address
	MCmd	3	master	Transfer command
	MData	configurable (32)	master	Transfer data
	MDataValid	1	master	Write data valid
	SDataAccept	1	slave	accept write data
	SCmdAccept	1	slave	accept command
	SData	configurable (32)	slave	Transfer data
	SResp	2	slave	Transfer response
Burst	MBurstLength	configurable (8)	master	Transfer burst length
	MBurstSeq	3	master	Transfer burst sequence
	MReqLast	1	master	Last write request
	MDataLast	1	master	Last write data
	SRespLast	1	slave	Last read response
Threads	MThreadID	configurable (2)	master	Request thread identifier
	SThreadID	configurable (2)	slave	Response thread identifier
	MDataThreadID	configurable (2)	master	Write data thread identifier
Sideband	SInterrupt	1	slave	Slave interrupt

Table 4.2 *CI Signals of Master NA*

destination core where a request should be transfered to, and the “local address” provides the internal address of the destination core where the request should be executed on.

One important feature in the OCP is that the data can be held on the ports until the data have been processed by using `SCmdAccept` signal. Using this handshake mechanism, whereby no new inputs can be accepted until the signal `SCmdAccept` is asserted, there is no need to maintain buffers for the new inputs. This in turn can be translated to an economy in terms of hardware resources and area.

The `MData`, `SData` and `MAddr` widths are configurable. In our CI they should be configured to 32-bit wide.

4.1.1.3 Burst Transactions

The CI should use burst transactions. Therefore, it should include `MBurstSeq` and `MBurstLength` signals. In our design we will allow burst up to 256 words. This means the width of the `MBurstLength` signal must be 8-bits.

OCP Burst Models In OCP there are three different burst models. (i) *Precise burst:* In this model, the burst length is known when the burst is sent. Each data-word is transfered as a normal single transfer, where the address and command are given for each data-word, which has been written or read. (ii) *Imprecise burst:* In this model, the burst-length can change within the transaction. The `MBurstLength` shows an estimate on the remaining data-words that will be transfered. Each data-word is transfered as in the precise burst model, with the command and address sent for every data-word. (iii) *Single request burst:* In this model, the command and address fields are only sent once. That is in the beginning of the transaction. This means that the destination core must be able to reconstruct the whole address sequence, based on the first address and the `MBurstSeq` signal. It is called packaging.

The single request burst model is packing the data. This reduces power consumption, bandwidth and congestion [12]. Since the NA will pack the transactions to send over the network, the single request burst model is an ideal choice.

Data-handshake extension To support single request burst, the OCP data-handshake extension has to be used. The data-handshake signals are `MDataValid` and `SDataAccept`. Not all burst sequences are valid in the single request burst model. Only the burst sequences that can be packaged are valid. These are `INCR`, `DFLT1`, `WRAP` and `XOR`.

To avoid the need of using a counter to keep track of the burst-length, the signals `MReqLast`, `MDataLast` and `SRespLast` should be used. This saves area and makes the implementation simpler.

In the OCP a transfer is normally done in two phases. By introducing the data-handshake extension an extra transfer phase needs to be added. To avoid introducing this third phase (which makes the implementation much more complicated) the OCP parameter `reqdata_together` is enabled. This specifies a fixed timing relation between the request and data-handshake phase. This timing relation means that the request and data-handshake phase must begin and end together.

4.1.1.4 Connections

A connection is specified in OCP by using the `MConnID` signal. We use this signal to let a master cores select which service (i.e. a connection is directly mapped to a service) should be used for a transaction. Therefore, the signal is added to CI of Slave NA. Slave cores do not select services, so the `MConnID` signal is not needed by CI of Master NA. In the NA the Connection ID is directly mapped to the service and/or a port in the NI. In our design there will be four transmitting ports to the network. This means the width of `MConnID` must be 2-bit.

4.1.1.5 Threads

To support split transactions the `MThreadID` and `SThreadID` are added to the CI. This allows a master to issue multiple request (in theory one for each thread) and can thereby use the bandwidth more efficiently. If split transactions are not supported, the master must receive the responses in the same order as the requests were made. In a network this is very difficult to guarantee if requests are sent to different destinations or are routed on different paths. The reason for this is that different paths in the networks have varying speeds, which makes the mechanism of the right ordering unreliable.

Since the CI is configured to use multiple threads and the hand-shake extension, the `MDataThreadID` must be included in the CI (see [12]). The `MDataThreadID` is used to indicate which thread the data belong to, when issuing write requests.

4.1.1.6 Interrupt

To implement interrupts, the sideband signal `SInterrupt` is added to the CI.

4.1.2 Network Interface

The NI is the boundary between the synchronous domain (i.e. the NA and IP core) and the asynchronous domain (i.e. the network). The NI is the same for both the Slave NA and the Master NA. In order to have a reliable communication between two domains, the control signals from the network must be synchronized and the output signals from the NI must be glitch-free.

The number of input and output ports in the NI should be parameterized. To achieve this, it is suggested that a port should be implemented as one module.

This makes it easier to design a “core generator” to instantiate NAs with different number of ports.

The input and output ports in the NI should use a four-phase handshake push protocol with late data validity as shown in Figure 4.1.

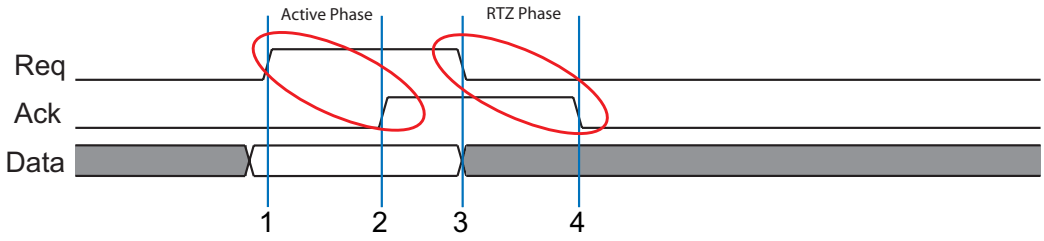


Figure 4.1 *4-phase Push Handshake Protocol*

1. The initiator applies the data and then starts the active phase by asserting `Req` from low to high. It must be ensured that the data is valid before the `Req` is asserted high.
2. The source accepts the data by asserting `Ack` from low to high. This ends active phase.
3. The initiator asserts `Req` from high to low. This starts the return-to-zero (RTZ) phase.
4. The source asserts `Ack` from high to low. This ends the RTZ phase.

Table 4.3 shows the signal configuration for NI.

Port type	Name	Width	Driver	Function
Transmit	Req	1	router	request signal
	Ack	1	network adapter	acknowledge signal
	Data	33	router	transfer data
Receive	Req	1	network adapter	request signal
	Ack	1	router	acknowledge signal
	Data	33	network adapter	transfer data

Table 4.3 *Signal Configuration for NI.*

4.1.2.1 Buffers

All data input ports from the NI must be buffered. For preventing blocking of the CI the buffer depth must be four flits for BE buffers and three flits for GS buffers. Four-flits is the maximum length of a package, except burst-write request and burst-read response.

The buffers should indicate when data are ready in the buffer. This must occur in two situations as: i) The buffer is full; ii) A package is stored in the buffer (i.e. the buffer contains a *end of package* (EOP) bit, see the package formats in section 4.3).

4.2 Service Management Specifications

There are two service management tasks for the Slave NA combined with service management. One is to keep track on the services available for the IP core connected to the Slave NA, and the other is to select and use the desired service when the IP core requests it.

4.2.1 Setup and Tear Down of BE Services

A BE service is setup by applying the routing path to destination core to the Slave NA's routing table (see memory map in section 4.4). It can be teared down, simply by overwriting the routing path in the Slave NA's routing path table.

4.2.2 Setup and Tear Down of GS

There are three combinations of GS services. To setup a service, it needs to be mapped to a connection ID in the Slave NA. This is done by writing to the corresponding connection configuration register, see section 4.4 for a memory map. To tear down a GS service its connection configuration register is "cleared". To see the specific configuration of the registers read section 4.4. Next we will look at how to setup GS under three different scenarios.

Setting up a GS → GS

1. The service is mapped to connection ID p in the Slave NA by configuring the corresponding connection configuration register. This connection is mapped to the Slave NA's transmitting port p.

2. The routers are configured so a connection is established from the Slave NA's transmitting port *p* to the Masters NA's receiving port *q*.
3. The Master NA's receiving port *q* is mapped to its transmitting port *r* by writing to the corresponding configuration register.
4. The routers are configured so a connection is established from the Master NA's transmitting port *r* to the Slave NA's receiving port *s*.

Setting up a GS → BE

1. The service is mapped to a connection ID *p* in the Slave NA by configuring the corresponding connection configuration register. This connection is mapped to the Slave NA's transmitting port *p*.
2. The routers are configured, so a connection is established from the Slave NA's transmitting port *p* to the Masters NA's receiving port *q*.
3. The Master NA's receiving port *q* is mapped to a routing path by written to the corresponding configuration register of port *q*.

Setting up a BE → GS

1. The service is mapped to a connection ID *p* in the Slave NA by configuring the corresponding connection configuration register. The connection configuration register is configured to the value of Master NA's transmitting port *q* and mapped to the Slave NA's BE transmitting port.
2. The routers are configured so a connection is established from the Master NA's transmitting port *q* to the Slave NA's receiving port *r*.

4.2.3 Selecting a Service

A service is selected by the IP core by setting the `MConnID` field on the CI. Table 4.4 shows how the connection IDs are mapped to the services.

`MConnID`	Service types	Comment
0	BE	default cannot be changed.
1	GS	Configurable
2	GS	Configurable
3	GS	Configurable

Table 4.4 *Connection Map to Service*

4.3 Package Format Specifications

The package format is an essential part of designing the NAs. The package format is reflected in the implementation of the encapsulation and decapsulation units in the NAs.

It has been specified that a package is constructed by flits which are 32-bit wide and the flits sent on the network must be applied an extra bit to indicate the end of a package.

4.3.1 Defining Package Types

In order to keep the design complexity low we try to reduce the package types to a minimum. This makes the encapsulation and decapsulation of requests and responses simpler.

We define two package types for the NA layer in the MANGO protocol stack: i) Request package. ii) Response package. Request packages are always sent from master cores to slave cores. Response packages are always sent from slave cores to master cores.

The package types for the network layer in the MANGO protocol stack have already been defined. They are BE packages and GS packages. The BE package encapsulates the request and response packages from the NI layer and applies a 32-bit header, which contains the routing path of the package. The GS package is a header-less package and is therefore the same as the request and response packages in the NA layer.

All flits are added an *end of package* (EOP) bit when sent to the network. This is to indicate where the packages end.

4.3.1.1 Request Package Header

The package header contains vital information that is needed in order for the Master NA to issue the request, return the response and manage the network services. The request package header is shown in Figure 4.2 and spans over two flits.

The fields in the request package header are:

Command: The command field `MCmd` from the OCP request.

Thread ID: The thread id for identifying the OCP transaction.

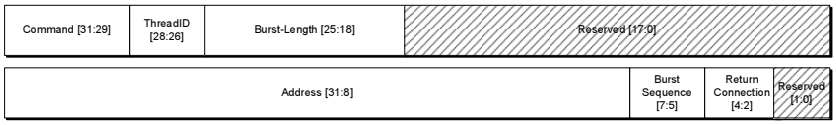


Figure 4.2 *Request Package Header*

Burst-Length: The length of the OCP burst (i.e. the size of the payload in the NA layer).

Reserved: Reserved for further expansions of the features and services of the NAs.

Address: The "local address" of the OCP `MAddr` field (i.e. bit 23 down to bit 0 of `MAddr`).

Burst Sequence: The OCP burst sequence field `MBurstSeq`.

Return Connection: Information to the Master NA about which transmit port the response should be returned to. This field is only valid for BE → GS transactions.

Reserved: Reserved for further expansions of the features and services of the NAs.

4.3.1.2 Response Package Header

The response package header contains vital information about the response as shown in Figure 4.3.

Figure 4.3 *Response Package Header*

The fields in the response package header are:

Reserved: Reserved for further expansions of the features and services of the NAs.

Thread ID: The thread id for identifying the OCP transaction.

Response: This hold the OCP `SResp` field.

4.4 Memory Map Specifications

The Slave NA can be configured through the CI or the NI and the Master NA can be configured through the NI by making a write transaction in the NAs memory space. The NAs are part of the systems memory space, which means no additional ports or instructions are needed to configure them. This makes the NAs very flexible in relation to the IP cores and the network.

If the NAs are configured via the NI, the configuration must be done by using the BE service (i.e. port zero). If the Slave NA is configured through the CI, the IP core should address the Slave NA by setting the "global address" to zero. Figure 4.4 and Figure 4.5 show the memory map for the Slave NA and the Master NA.

Address	data-width 32-bits
0x00	Temporary Thread IDs
0x1F	
0x20	Configuration Registers
0x3F	
0x40	Configure interrupt

Figure 4.4 *Master NA Memory Map*

Address	data-width 32-bits
0x00	Connection Configuration Registers
0x1F	
0x20	Routing Path Table
0x5F	
0x60	Set interrupt

Figure 4.5 *Slave NA Memory Map*

4.4.1 Connection Configuration Registers

The connection configuration registers are located in the Slave NA from address $0x0$ to $0x1F$. They store the configuration of a connection (i.e. GS). One configuration register is 32-bits where bit 31 down to 4 are "don't cares". Bit 3 indicates if a service is setup in the connection. '1' means a service is setup, '0' means it is free. 3-Bits, bit 2 down to 0, are for setting the Masters NA's transmitting port, when a service is setup to BE $\rightarrow$ GS. zeros means it is disabled. A value larger than zero means the response transmitting port of the Master NA (see Figure 4.6).

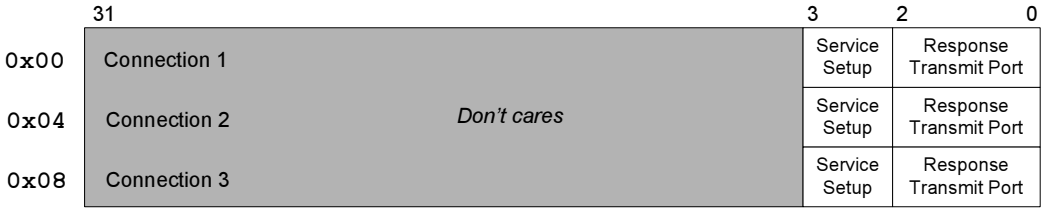


Figure 4.6 *Connection Configuration Register*

4.4.2 Routing Path Table

As shown in Figure 4.5, the routing-path table is located in the Slave NA from address $0x20$ to $0x5F$. It is used for setting up BE → BE services. To setup a service the core id (i.e. the "global address") and the routing path must be written to the look-up table. The core id is stored as a 32-bit word, where bit 31 down to 24 are "don't cares". The corresponding routing path is stored on the following address also as a 32-bit word (see Figure 4.7).

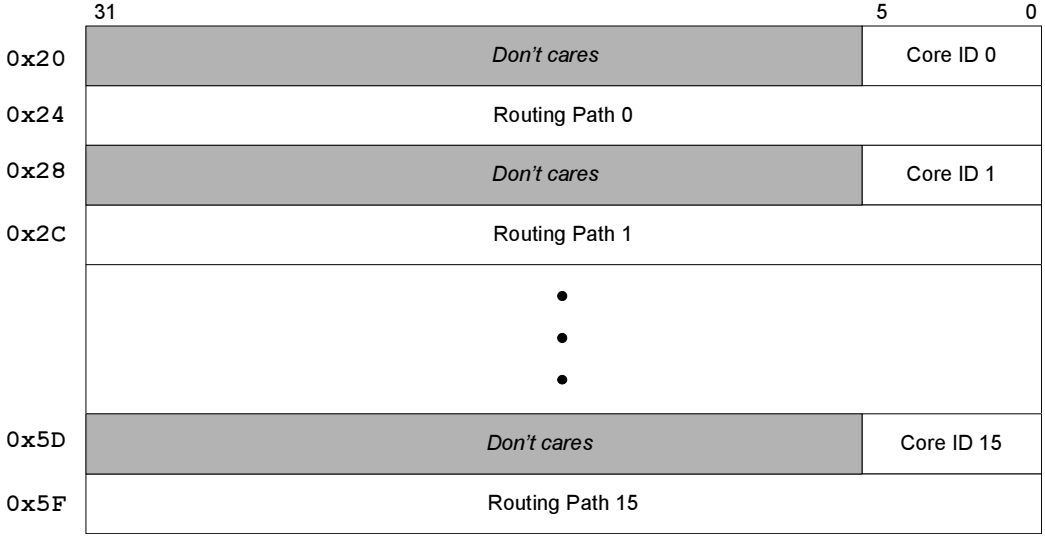


Figure 4.7 *Memory Map of Routing Path Table*

In our design the look-up table has 16 entries, which means 16 BE services can be setup.

4.4.3 Set Interrupt Register

The set interrupt register is located in the Slave NA at address $0x60$. It is 32-bits wide, where bit 31 down to 1 are “don’t cares”. It is used to set the interrupt value low or high.

4.4.4 Temporary Thread IDs

The temporary thread IDs are located in the Master NA at address $0x00$ to $0x1F$. This is private memory space for the Master NA and cannot be accessed.

4.4.5 Port Map Configuration Registers

The port map registers are located in the Master NA from address $0x20$ to $0x3F$. They are used to map the Master NA’s receiving ports to Master NA’s transmitting ports (GS $\rightarrow$ GS) or map the Master NA’s receiving port to a routing path (GS $\rightarrow$ BE).

The port map registers are 32-bit wide. To distinguish a port number from a routing path, the value is compared to the largest port number in the design. A routing path is 32-bit wide, while the port number is 3-bit wide. The routing path can never have more than four zeros in a row. This is due to the routing algorithm chosen in the MANGO network. Six zeros means that the package will bite its own tail. This is not allowed.

4.4.6 Configure Interrupt Register

The configure interrupt register is located in the Master NA at address $0x40$. It is 32-bit wide. It contains the routing path if the interrupt should be sent using BE or a transmitting port if the interrupt should be transmitted using GS.

4.5 Network Adapter Parameters

Parameterizing the NA is not an easy task and cannot be done only by using VHDL. This project will focus on a modular design approach and encapsulate each task into separate modules. Parametrization of signal widths, memory and buffer sizes will be done in VHDL.

It also requests a script to generate the different VHDL modules and combine them. Writing such a script is not in the scope of this project, but when designing the modules this should be kept in mind. By dividing the design into modules it also makes optimizations and changes to modules easier.

CHAPTER 5

Micro Architectural Design and Implementation

In this Chapter we go thought the hierarchical structure and explain the design of each module in details. This leads to a design specification describing the modules at *register transfer level* (RTL). For each module we explain specific choice in the implementation.

The design emphasizes modularity. This is done by encapsulating each task in the NA adapter into a module. It makes further development and optimization simpler, as each module can be developed and optimized separately. Also replacement of modules can be done without altering the design, as long as the replacement module follows the design specification for the specific module (e.g., the CI could be replaced to comply with a different socket specification, such as AXI or Wishbone). This makes the design very flexible and easy to adapt to different systems.

5.1 Module Protocol

First we describe the module protocol, which is used to communicate between modules. The protocol is very simple. Parallels can be drawn to the OCP signals `MCmd` and `SCmdAccept`. Figure 5.1 shows the timing diagram of the protocol.

The protocol has two excellent properties. One property is the control signals can ripple through each module in the design, so data can get through with very low latency. Another property is when throughput should be emphasized over latency, pipeline registers can be added between the modules which use the protocol.

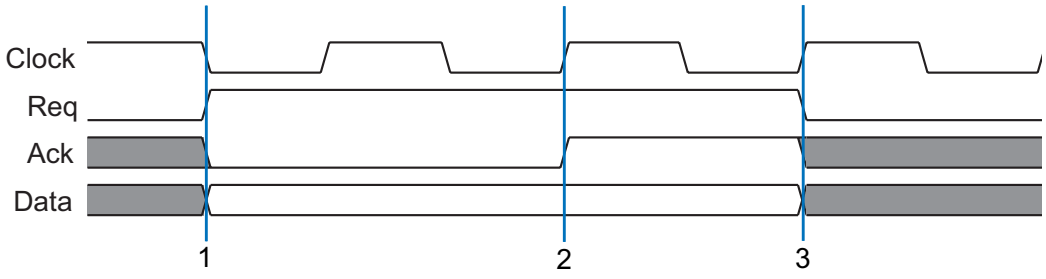


Figure 5.1 *Timing Diagram of Module Protocol*

The three phases in the Timing Diagram are:

1. The initiator module starts the transfer on the rising edge of the clock by asserting the `Req` signal from low to high. At the same time data are presented on `Data`.
2. The source module accepts the transfer by asserting the `Ack` signal from low to high.
3. The transfer ends on the next rising clock edge after the transfer has been accepted.

5.2 Slave Network Adapter

The tasks of the Slave NA are to receive requests from the master core, encapsulate the request into a package, transmit packages to the network, receive response from the network, decapsulate response and transmit response to master core.

Slave NA architecture is built on two data-flows. One data-flow is the request data flow, where the core is the source and the network the destination. It consists of three modules such as “OCP Request Module”, “Request Control Module” and “NI Transmit Module” (*Network Interface Transmit Module*). The second data-flow is the response data-flow where the network is the source and the core the destination. It consists of three module such as “NI Receive Module” (*Network Interface Receive Module*), “Response Control” and “OCP Response Module”. There is a look-up table shared by the two data-flows. The look-up table is used by the request data-flow to resolve the connection or routing path for a given transaction. The look-up table can be updated by the core through the request data-flow and from network through the response data-flow. The relation between modules is shown in Figure 5.2.

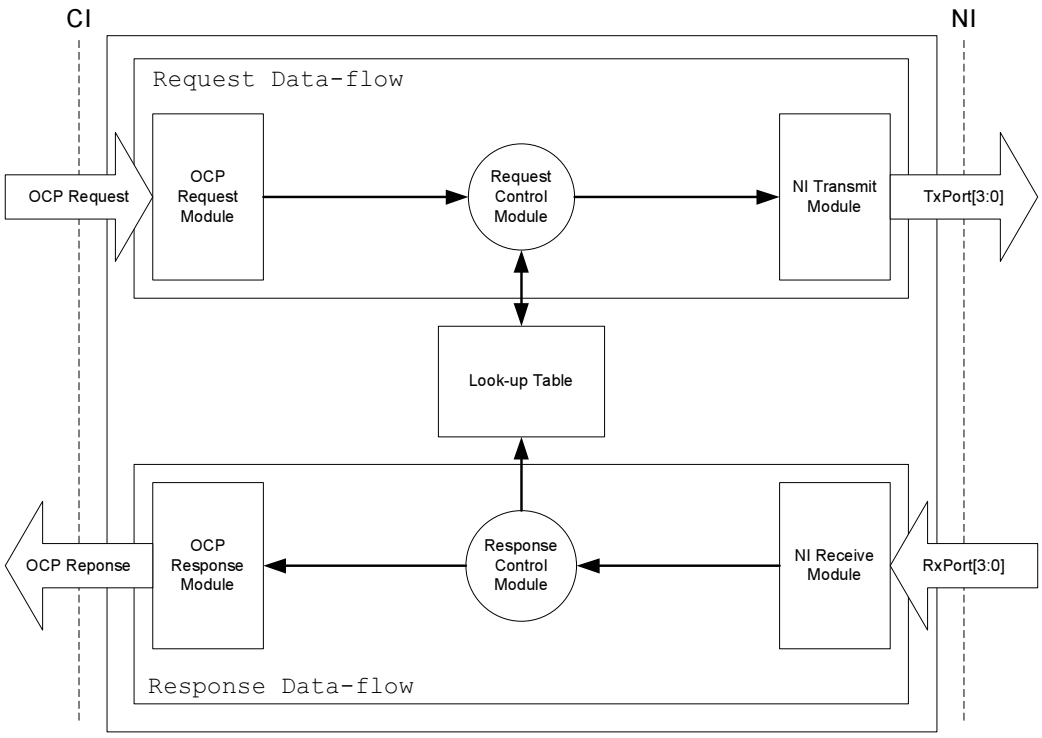


Figure 5.2 *Slave Network Adapter Architecture*

5.2.1 Request Data-flow

The request data-flow is divided into three stages. The first stage is where the data are received by the “OCP Request Module” from core via the CI. The second stage is where the data are processed and encapsulated by the “Request Control Module”. Data for configuring the slave NA are written to the look-up table. The third stage is where the data are transmitted to the network by the “NI Transmit Module” via the NI. The boundary between the stages follows the protocol described in section 5.1.

5.2.1.1 OCP Request Module

The “OCP Request Module” controls the CI. This module uses the OCP to receive request from the CI and forward the request to the “Request Control Module” by using the simple module protocol as described in section 5.1. Figure 5.3 shows the state diagram of the “OCP Request Module”.

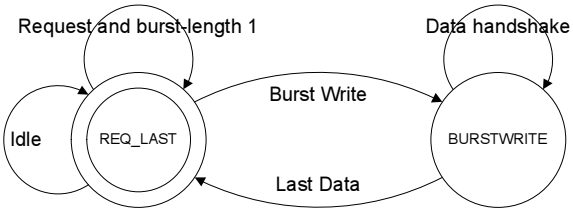


Figure 5.3 *State Diagram of OCP Request Module*

Implementation This module is implemented as a Mealy finite state machine. A Mealy implementation is chosen over Moore for two reasons: i) Mealy machines have a lower latency; ii) Mealy machines take up less resources in terms of area. In [12] this is referred as a combinatorial slave implementation.

5.2.1.2 Request Control Module

"Request Control Module" is in the second stage of the request data-flow. It receives the request from "OCP Request Module", analyzes the request and constructs the network package.

Analyze Request "Request Control Module" analyzes the request to determine the destination of the request. The request can either be to configure the Slave NA, or it can be a request for another core, which needs to be encapsulated and sent to the "NI Transmit Module".

The destination can be determined by the "global address" (i.e. the six most significant bits in the address field). If the "global address" is zero, the request is for configuring the Slave NA. The request is processed and the data are written to the look-up table. If the "global address" is different from zero, the destination is found in the look-up table by using the connection id and the "global address". After the destination and service are determined, the "Request Control Module" can construct the package.

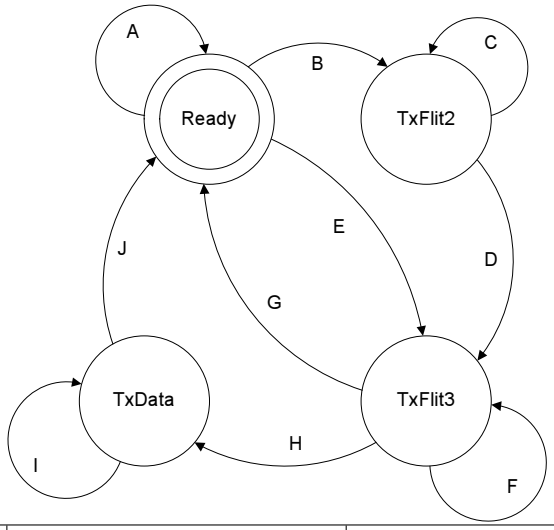
Construct Package The are two package formats. One is used for GS. This is the NA package format. The other is used for BE, and is the network package format. The network package format encapsulates the NA package format (see section 4.3).

The package header is created based on which service the request should be transmitted on. If the command in the request is a write command, a payload

should be added to the package.

After each package flit is created, this module sends the flit to the “NI Transmit Module” using the simple module protocol. After the “NI Transmit Module” has received the flit, the “Request Control Module” can construct the next flit in the package. The “Request Control Module” indicates the last flit by setting the EOP flag as described in section 4.3.

The state diagram of the “Request Control Module” is shown in Figure 5.4.



State	Transaction Condition		Action
READY	A	No “OCP Request” **or** flit has not been sent	Wait for data from “OCP Request Module” **or** wait for flit has been sent.
	B	“OCP Request” ready and service is BE → BE/GS	Create flit 1 in package header and send(BE)
	E	“OCP Request” ready and service is GS → BE/GS	Create flit 2 in package header and send(GS)
TxFlit2	C	flit has not been sent	Wait until flit 2 has been sent
	D	Flit has been sent	Create flit 2 in package header and send(BE)
TxFlit3	F	Flit has not been sent	Wait until flit 3 has been sent
	G	last flit in request is sent	Create flit 3 in package header and send(BE/GS). This is EOP.
	H	Flit has been sent	Create flit 3 in package header and send(BE/GS)
TxData	I	flit has been sent **or** flit has not been sent	Wait until data flit has been sent
	J	last flit has been sent	Transmit data flit(BE/GS)

Figure 5.4 *State Diagram of Request Control Module*

Implementation This module is implemented as a Mealy finite state machine based on the same reasons as described in “OCP Request Module”. Table 5.1 shows the port map of the module.

Port name	Direction	Width	Description
Clk	in	1	clock signal
Reset_n	in	1	reset signal active low
OCPReady_i	in	1	handshake signal from OCP req module
OCPDone_o	out	1	handshake signal to OCP req module
LUTValid_i	in	1	data valid signal from lut
LUTData_o	out	32	data bus to lut(write data)
LUTData_i	in	32	data bus from lut(routing path)
LUTData2_i	in	3	data bus from lut (service config)
LUTWrite_o	out	1	handshake signal to lut
LUTDone_i	in	1	handshake signal from lut
LUTConnID_o	out	2	select service
LUTAddr_o	out	24	write address bus
NIReady_o	out	1	handshake signal to NI transmit module
NIDone_i	in	1	handshake signal from NI transmit module
Data_o	out	32	data bus to NI transmit module
EOP_o	out	1	EOP bit to NI transmit module
MCmd_i	in	3	OCP command
MConnID_i	in	2	OCP connection ID
MReqLast_i	in	1	OCP last request flag
MDataLast_i	in	1	OCP last data flag
MAddr_i	in	32	OCP address bus
MData_i	in	32	OCP data bus
MBurstLength_i	in	8	OCP burst-length field
MBurstSeq_i	in	3	OCP burst sequence field
MThreadID_i	in	3	OCP thread ID field

Table 5.1 *Port Map of Request Control Module*

5.2.1.3 NI Transmit Module

“NI Transmit Module” receives package flits from the “Request Control Module” and sends it out from the NA to the network.

The “NI Transmit Module” has four transmitting ports to the network as shown in Figure 5.5.

Since the CI is a point to point connection and the GS ports are connected directly to the CI without any buffers, the GS ports will never operate simultaneously. We decided to use three GS ports in the “NI Transmit Module” for enabling the future extensions of the NA (see section 8.2). Here multiple cores are connected to the NA via multiple CIs.

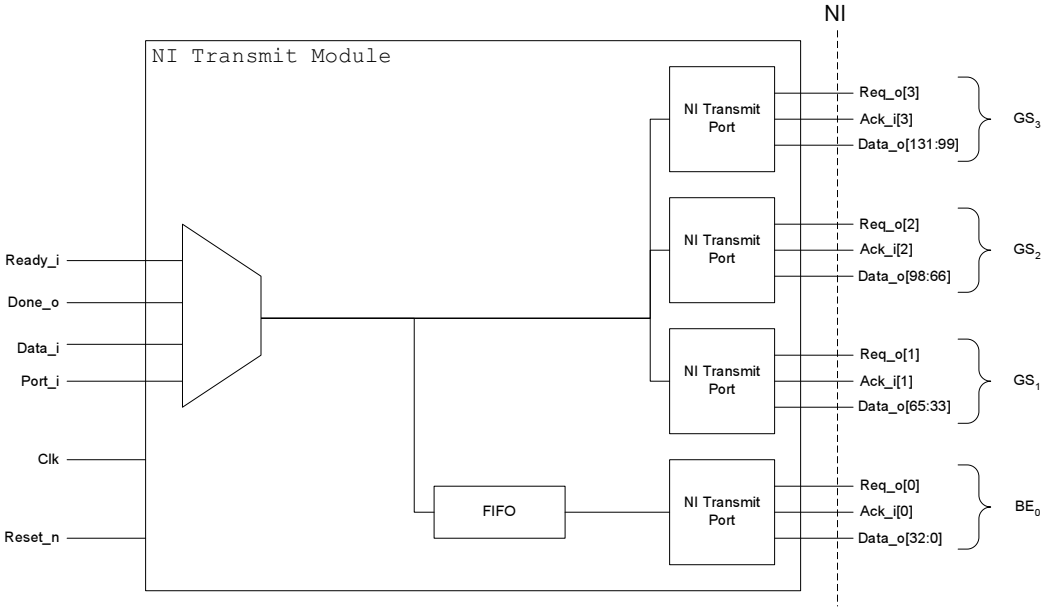


Figure 5.5 *NI Transmit Module*

Transmit Port "Transmit Port" is the synchronizer between the NA and the network. It receives the package flits from the "OCP Request Module" or from the FIFO in the "NI Transmit Module" by using the module protocol. Then it transmits the flits to the network using the *four phase handshake push protocol* as described in section 4.1.2.

Implementation The transmit port is implemented as a Mealy finite state machine. Figure 5.6 shows the port map, state diagram, how we insure the control signal from the NA is glitch free, and how the control signal from the network is synchronized. The theory of the synchronization has been described in section 3.2.6.

5.2.2 Response Data-flow

The Response data-flow is also divided into three stages. The first stage is where the data are received by the "NI Receive Module" from network via the NI. The second stage is where the data are processed and decapsulated by the "Response Control Module". Data for configuring the slave NA are written to the look-up table. The third stage is where the data are transmitted to the master core by the

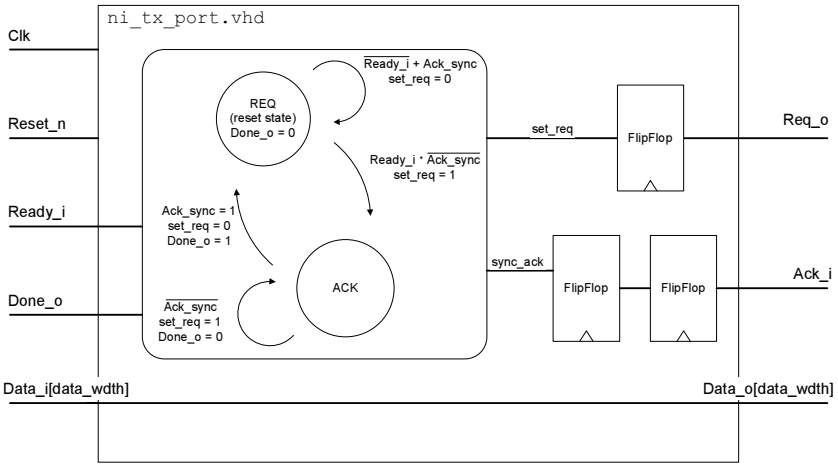


Figure 5.6 *Transmit Port Diagram*

"OCP Response Module" via the CI. The boundary between the stages follows the protocol described in section 5.1.

5.2.2.1 NI Receive Module

"NI Receive Module" receives package flits from the network through four receiving ports. The flits will be buffered in four FIFOs, where a scheduler will manage to forward the flits to the "Response Control Module" by using the module protocol (see section 5.1). The structural diagram of "NI Receive Module" is shown in Figure 5.7.

Receive Port "Receive Port" is the synchronizer between the NA and the network. It receives the package flits from the network using the *four phase handshake push protocol* as described in section 4.1.2, and writes the package flits to a FIFO using the module protocol.

Implementation The "Receive Port" is implemented as a Mealy finite state machine. Figure 5.8 shows the port map, state diagram, how we insure the control signal from the NA is glitch free, and how the control signal from the network is synchronized. The theory of the synchronization is described in section 3.2.6.

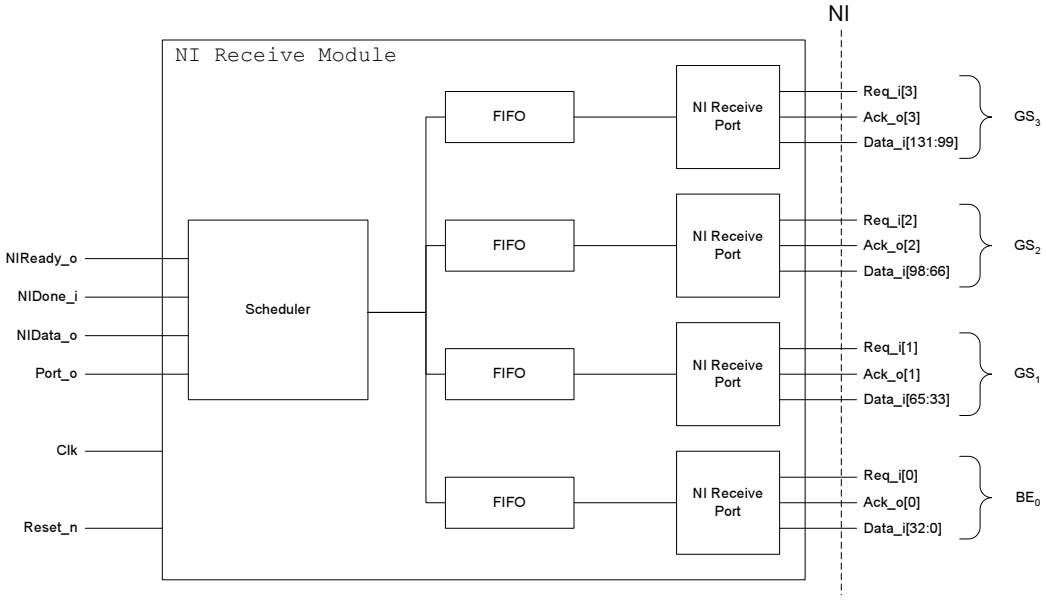


Figure 5.7 *NI Receive Module*

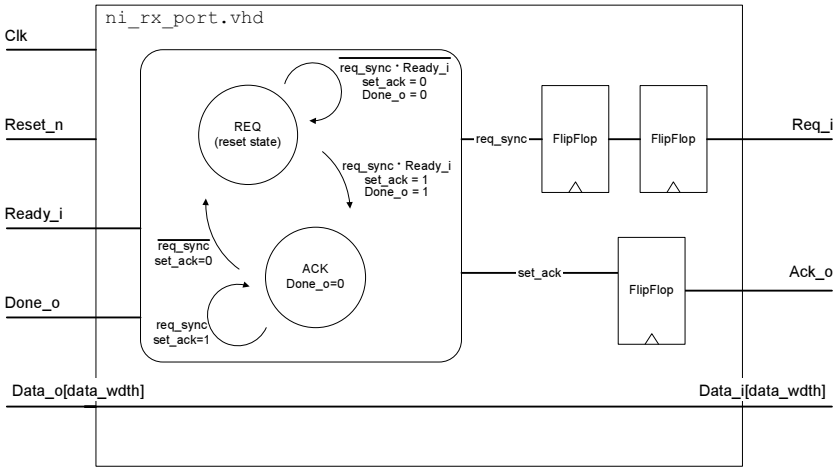


Figure 5.8 *Receive Port Diagram*

5.2.2.2 FIFO

The FIFO is a first in, first out memory. The implemented FIFO is based on a dual port memory block as shown in Figure 5.9.

The FIFO is implemented with synchronous read and write. When a read or write operation is issued, the operation must be validated first. If the FIFO is

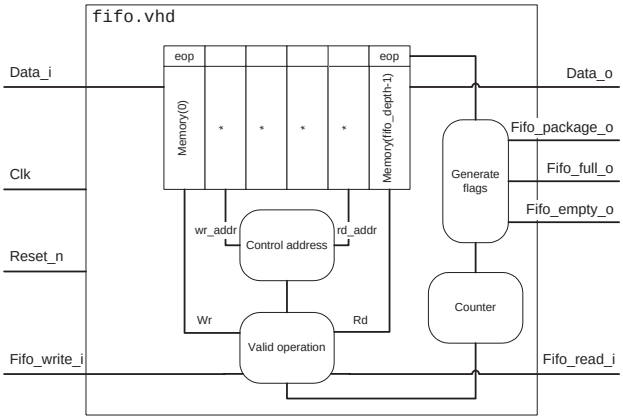


Figure 5.9 *FIFO Diagram*

empty a read cannot occur, and if the FIFO is full a write cannot occur. If an operation is not valid, the operation is ignored.

The FIFO has two address pointers. One points at the read location, and another points at the write location. Each time an operation has been validated, the corresponding pointer gets incremented. When a pointer reaches the allowed maximum address, it will be reset when it gets incremented again.

A counter holds the status information of the FIFO. If a write operation is validated, the counter is incremented by one. If a read operation is validated, the counter is decremented by one. If both a read operation and a write operation are validated, the counter remains unchanged.

The flag generator generates the flags based on the status of the FIFO. If the counter is zero the FIFO is empty, and if the counter is at maximum the FIFO is full. An additional flag has been implemented to indicate if the FIFO contains an EOP bit. The EOP bit is a copy of the most significant bit in the data word. When a word has been read from the FIFO, the EOP bit gets cleared.

The FIFO depth and data width are implemented as generics, which are defined when the module is instantiated.

5.2.2.3 Scheduler

The scheduler's task is to merge the received data-streams from the FIFOs. This is done by multiplexing the packages on the different data streams. The multiplexing of the packages is done by using a round robin algorithm, where the GS data-streams have equal priority and the BE data-stream has no priority.

It is preferable that the scheduling algorithm in the NA is the same as in the network. We have chosen a simple Round Robin algorithm to implement the scheduler, due to the lack of information about the scheduling algorithm in the network. When a full specification of the network is available, the scheduling module can be replaced with an algorithm that matches the network's algorithm. The flowchart of the round robin algorithm is shown in Figure 5.10.

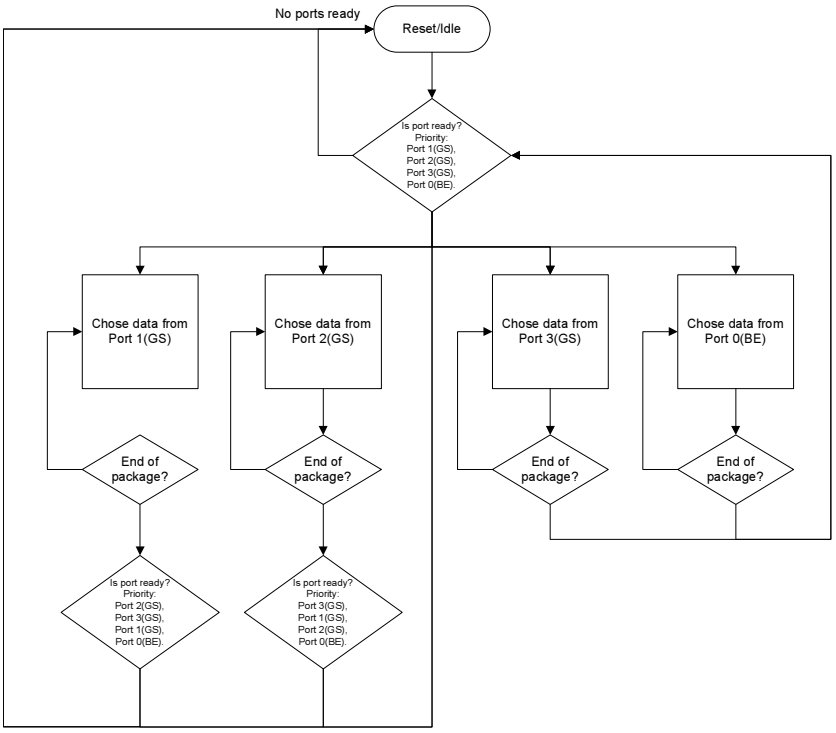


Figure 5.10 *Flowchart of Round Robin Algorithm*

Implementation The scheduler is implemented as a Mealy finite state machine. It supports four data-streams. If additional receiving ports are added to "NI Receive Module", the scheduler module cannot be configured by using the generics in the VHDL implementation. Instead a small script can be made to generate the VHDL implementation of the scheduler. This will be considered to be out the scope of this projects. The port map of the scheduler is shown in Figure 5.11.

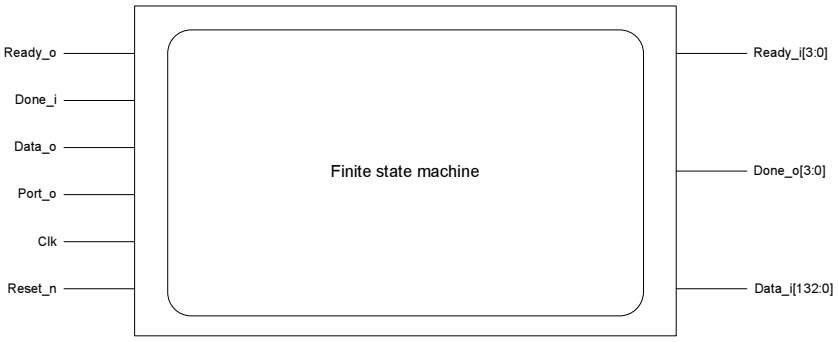


Figure 5.11 *Scheduler Port Map*

5.2.2.4 Response Control Module

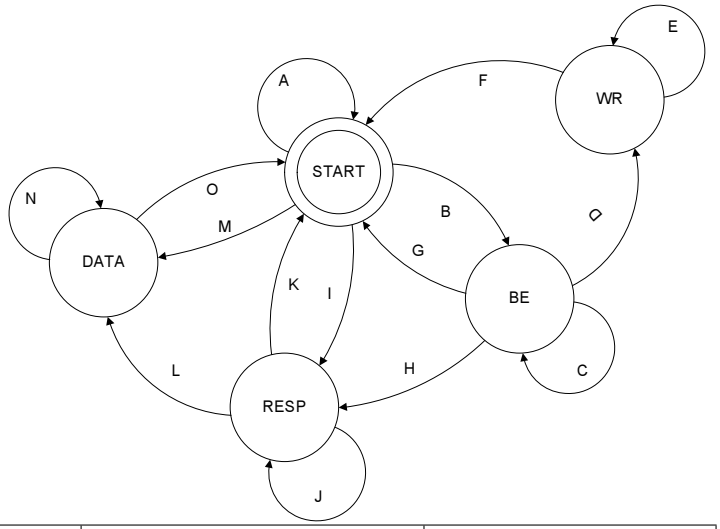
The tasks of the “Response Control Module” are to decapsulate the packages received from the “NI Receive Module”, analyze package, use the request packages to configure the look-up table, and send the response package to “OCP Response Module” using the module protocol as described in section 5.1.

Figure 5.12 shows the design of the state diagram of the “Response Control Module”.

Implementation The “Response Control Module” is implemented as a Mealy finite state machine. Table 5.2 shows the port map of the module.

Port name / Direction / Width			Description
Clk	in	1	clock signal
Reset_n	in	1	reset signal active low
NIReady_i	in	1	handshake signal from NI receive module
NIDone_o	out	1	handshake signal to NI receive module
NIData_i	in	32	data bus from NI receive module
OCPReady_o	out	1	handshake signal to OCP resp module
OCPDone_i	in	1	handshake signal from OCP resp module
LUTWrite_o	out	1	handshake signal to look-up table
LUTDone_i	in	1	handshake signal from look-up table
LUTAddr_o	out	24	write address bus to look-up table
LUTData_o	out	32	write data bus to look-up table
Port_i	in	2	port indicator from NI receive module
SResp_o	out	2	OCP response field to CI
SThreadID_o	out	8	OCP thread id field to CI

Table 5.2 *Port Map of Response Control Module*



State	Transaction / Condition		Action
START	A	flit from NI not ready (**or** flits is GS **and** response accepted)	wait for flit **or** issue response
	B	flit is BE	discard flit 1
	I	flit is GS **and** not response accepted	issue response
	M	flit is GS **and** response accepted	get next flit
BE	C	response not accepted	wait
	D	request to NA	get next flit
	G	response accepted **and** EOP	get next package
	H	response accepted	get next flit
WR	E	write to LUT not completed	wait
	F	write to LUT complete	get next package
RESP	J	response not accepted	wait
	K	response accepted **and** EOP	get next package
	L	response accepted	get next flit
DATA	N	response not accepted **or** response accepted	wait **or** get next flit
	O	response accepted **and** EOP	get next package

Figure 5.12 *State Diagram of Response Control Module*

5.2.2.5 OCP Response Module

The task of “OCP Response Module” is to transmit the response back to the master core via CI. This module handles the response phase of the OCP. Figure 5.13 shows the state diagram of the “OCP Response Module”.

Implementation The “OCP Response Module” is implemented as a Mealy finite state machine, following the guidelines in OCP specification[12].

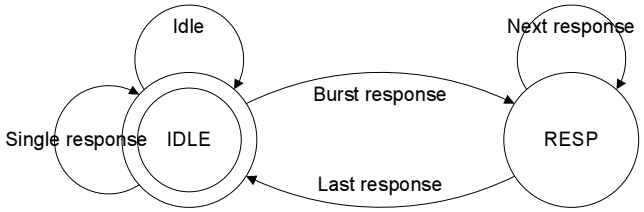


Figure 5.13 *State Diagram of OCP Response Module*

5.2.3 Look-up Table

The look-up table is shared by the request data-flow and the response data-flow. It holds the configurations of the GS connections and the routing paths for BE. The architecture and port map of look-up table is shown in Figure 5.14.

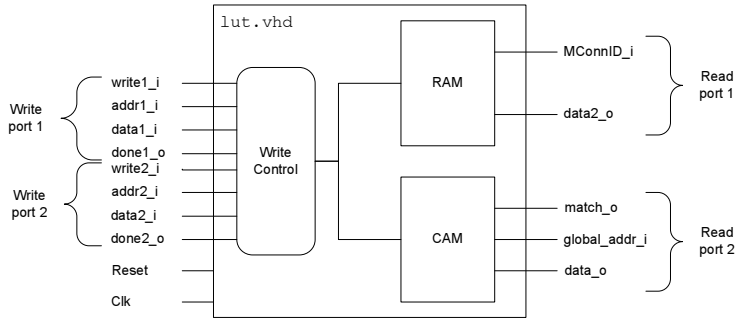


Figure 5.14 *Look-up Table*

The look-up table has two write ports, “write port 1” and “write port 2”. “write port 1” is used by the request data-flow to write to the look-up table. “write port 2” is used by the response data-flow to write to the look-up table. “write control” process makes sure that only one port is granted write access at a time. This is done by giving the most resent used port the lowest priority, so both ports get equal chance to write to the look-up table.

“write port 1” and “write port 2” both include a write signal, address signal, data signal and done signal. The write ports are using the module protocol which is described in section 5.1.

5.2.3.1 Random Access Memory (RAM)

The RAM block stores the GS configurations. If the request should be sent by using GS, the configuration register should be zero. If the request should be sent

by using BE and the returning response should be sent by using GS, the configuration register should contain the value of the transmit port in the Master NA. This is described in pseudo code below.

```
if register[connection id] = 0 then
   request is sent using GS on connection = connection id
else
   request is sent using BE on connection = 0
   response is sent using GS on Master NA connection = register[connection id]
```

The RAM is read by the request data-flow through “Read port 1”. The read address used is the connection id.

Implementation The RAM is implemented as a dual port RAM with synchronous write and asynchronous read. This allows requests to be sent while the look-up table is being updated through the response data flow. The asynchronous read is chosen to keep a low latency, in terms of clock cycles, through the Slave NA. This means a read can be done in one cycle and not in two, which is the case for a synchronous read.

The data width, address width and size are given through generic which are chosen when the module is instantiating. In this way the RAM module can easily be reused in other parts of the design. Figure 5.15 shows the diagram of the RAM module.

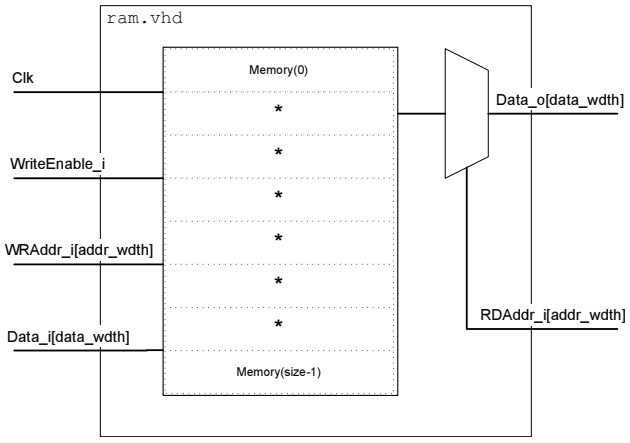


Figure 5.15 *RAM Diagram*

5.2.3.2 Content Addressable Memory (CAM)

The CAM block stores the he routing paths for BE. The routing path is found in the CAM by searching for the index tag matching the “global address”. The CAM is read by the request data-flow through “Read port 2”.

Implementation The CAM is implemented as two RAM blocks. One is for storing the tags and another is for storing the routing paths as shown in Figure 5.16. Each RAM block has a synchronous write port.

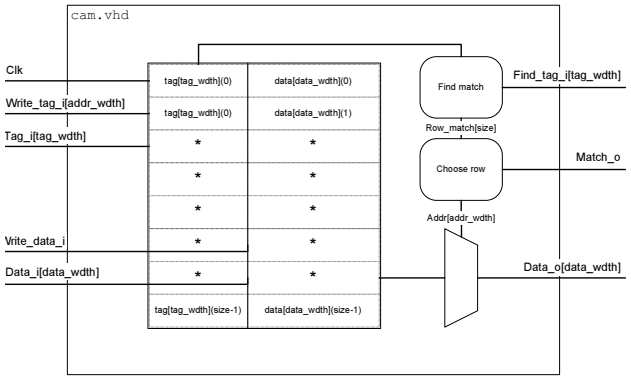


Figure 5.16 *CAM Diagram*

Reading from the CAM is done by searching the tags to see if a match exists. All tags are compared in parallel and for every row where a match is found, the row is marked. If no row is marked, no match exists and the `Match_o` is held low. If one or more rows exist, a marked row has to be selected. The select mechanism selects the last matching row and reads out the data value (i.e. the routing path). `Match_o` is asserted to indicate a match.

The tag width, data width, address width and CAM size are defined when the module is instantiated. This is done by using generic in VHDL.

5.3 Master Network Adapter

The tasks of Master NA are to receive request packages from the network, decapsulate the request packages, transmit the request to the slave core, receive response from the slave core, encapsulate response and transmit response to the network.

Master NA architecture is built on two data-flows. One data-flow is the request data flow, where the network is the source and the slave core is the destination. It consists of three modules such as “NI Receive Module”, “Request Control Module” and “OCP Request Module”. Another data-flow is the response data-flow where the slave core is the source and the network is the destination. It consists of three module such as “OCP Response Module”, “Response Control Module” and “NI Transmit Module”. There is a register table shared by the two data-flow. The request data-flow uses it to store the configuration of the Master NA and temporarily store the thread id of the transaction. The response data-flow uses it to read the configuration of the Master NA and get the thread id of a transaction. The relation between modules is shown in Figure 5.17.

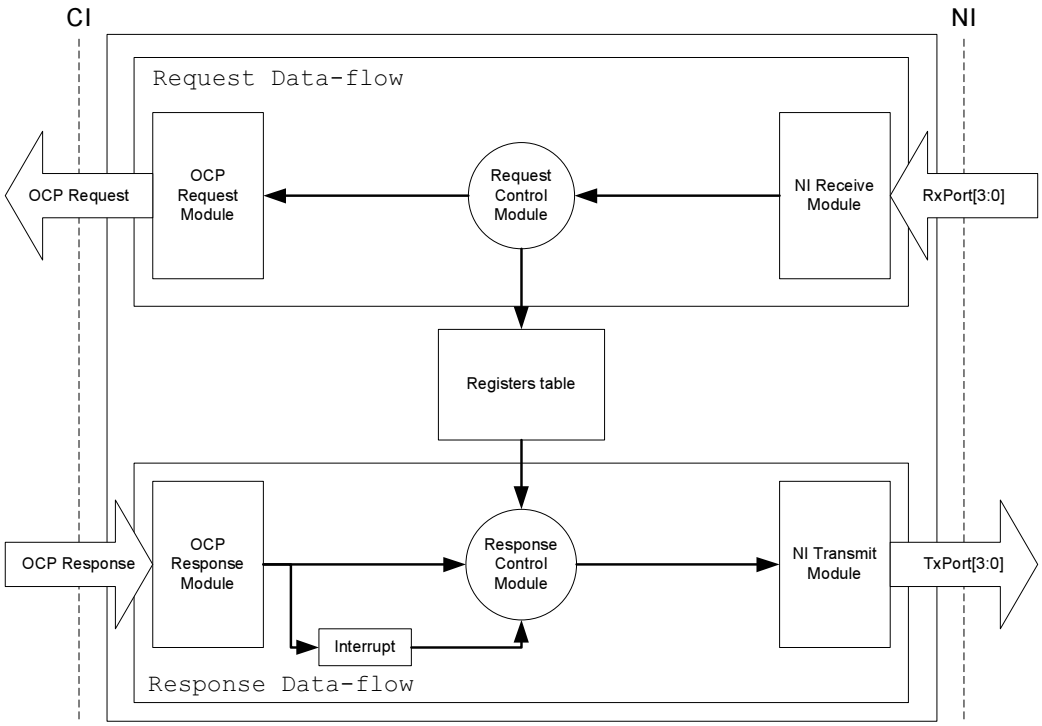


Figure 5.17 *Master Network Adapter Architecture*

5.3.1 Request Data-flow

The Request data-flow is divided into three stages. The first stage is where the data are received by the “NI Receive Module” from network via the NI. The second

stage is where the data are processed and decapsulated by the “Request Control Module”. Data for configuring the Master NA is written to the register table. The third stage is where the data are transmitted to the slave core by the “OCP Request Module” via the CI. The boundary between the stages follows the module protocol described in section 5.1.

5.3.1.1 NI Receive Module

This module is the same as “NI Receive Module” described in section 5.2.2.1 of the Slave NA.

5.3.1.2 Request Control Module

“Request Control Module” is in the second stage of the request data-flow. It receives the package request from “NI Receive Module”, decapsulate and analyze the request.

Analyze Request “Request Control Module” analyzes the request to find out from which port it came from. If requests came from GS ports, they need to be sent further to the slave core. If requests from BE port, further analyze is needed to find out it is for configuring register table or it needs to be sent further to slave core. The further analyze procedure is to check if the network package header’s value is equal and less than four, then the request package is for configuring the Master NA, otherwise the package is for the slave core.

The destination can be determined by the “global address” (i.e. the six most significant bits in the address field). If the “global address” is zero, the request is for configuring the Slave NA. The request is processed and the data are written to the look-up table. If the “global address” is different from zero, the destination is found in the look-up table by using the connection id and the “global address”. After the destination and service are determined, the “Request Control Module” can construct the package.

The “Request Control Module” unpacks the package received from the NI. To determine if the package is for configuring the NA or is a request for the core, the routing path in the first flit is analyzed. Data to the NA are written to the configuration registers. Data that contain a request are unpacked, and an OCP request is created.

Analyze Package and Extract Information In section 4.3 we have described the two package formats of the network and NA. All incoming packages on port zero are network packages and sent using BE. Network packages can either be for the core or to configure the NA. To determine the destination the routing header is analyzed. Incoming packages on other ports are NA packages. They have been sent using GS. The packages are all for the core, since configuration of the NA has to be done by using a BE service.

Request Type The NA needs to determine request type in order to package the response correctly. The request type can be found by looking at the command field in the first flit of the NA package. If the request is a write type request, the NA will write zero to the thread's response type register, otherwise it will write one (i.e. the request type is read). This information is used by the "Request Control Module" to find out if the data field from the CI should be put as payload in the response package.

Substitution of Thread ID The NA has to substitute the thread ID that is sent with a package. The thread ID in the package corresponds to the OCP transaction made in the Slave NA and is therefore a local thread ID. To avoid mixing local thread ID's from different cores, the thread ID is substituted with a new thread ID. The new thread ID matches the port number from which the data were received by the NI. This means the Master NA has the same number of threads as the number of ports it has in the NI. And each thread ID is mapped to an incoming port number.

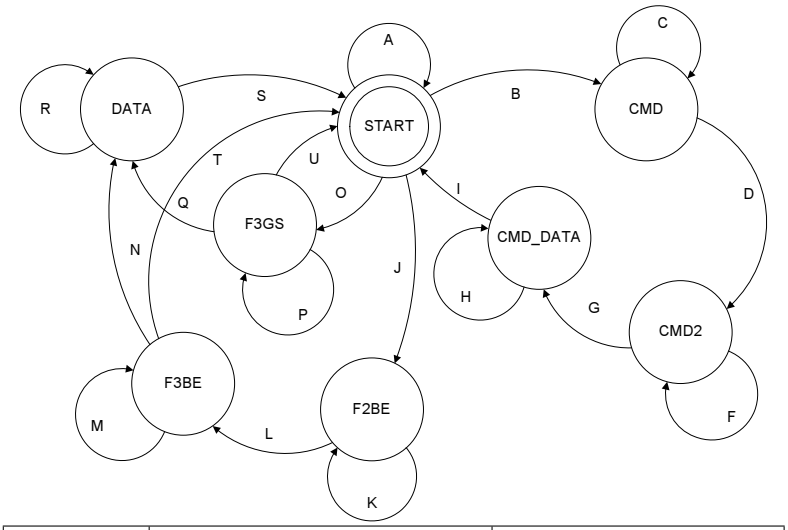
The local thread ID is saved in a register belonging to the new thread, so it can be substituted again, if a response is sent back as described in section 5.3.2.2.

Preparing the Request for the CI When the first flit of the NA package is received, the NA sets up the command, burst length and the substituted thread ID. When the second flit is received, the NA sets up the address and burst type.

The state diagram of the "Request Control Module" is shown in Figure 5.18.

Implementation The "Request Control Module" is implemented as a Mealy finite state machine.

We have implemented a latch to store the address and the burst type, after they are extracted from the package. Then a read request can end in the same clock period when the address and burst type are extracted. We can also implement



State	Transaction / Condition		Action
START	A	wait for request	wait
	B	request for NA	discard flit
	J	request is BE	discard flit
	O	request is GS **and** decapsulate flit	wait for next flit
CMD	C	decapsulate flit	wait for next flit
	D	decapsulate flit	get next flit
CMD2	F	decapsulate flit	wait for next flit
	G	decapsulate flit	get next flit
CMD_DATA	H	write data to NA	wait for write complete
	I	write data to NA **and** EOP	get next request
F2BE	K	decapsulate flit	wait for next flit
	L	decapsulate flit	get next flit
F3BE	M	decapsulate flit	wait for next flit
	N	decapsulate flit	get next flit
	T	decapsulate flit **and** EOP	send request **and** get next request
F3GS	P	decapsulate flit	wait for next flit
	Q	decapsulate flit	get next flit
	U	decapsulate flit **and** EOP	send request **and** get next request
DATA	R	send request	get next flit
	S	send request **and** EOP	get next request

Figure 5.18 *State Diagram of Request Control Module*

a register instead of a latch, then a request would take an extra clock period to execute.

Table 5.3 shows the port map of the module. The module uses the module protocol (see section 5.1) to interact with its connected modules.

Port name / Direction / Width			Description
Clk	in	1	clock signal
Reset_n	in	1	reset signal active low
NIReady_i	in	1	handshake signal from NI receive module
NIDone_o	out	1	handshake signal to NI receive module
NIPort_i	in	2	port indicator from NI receive module
NIData_i	in	32	data bus from NI receive module
OCPReady_o	out	1	handshake signal to OCP req module
OCPDone_i	in	1	handshake signal from OCP req module
OCPCmd_o	out	3	OCP command field from CI
OCPAddr_o	out	32	OCP address field from CI
OCPBurstLength_o	out	8	OCP burst-length field from CI
OCPThreadID_o	out	3	OCP thread ID field from CI
OCPBurstSeq_o	out	3	OCP burst sequence field from CI
DestNA_i	in	1	indicate request is for NA
NAWrite_o	out	1	write enable signal to registers
NADataResp_o	out	1	indicates if a response have a payload
NAData_o	out	32	write data bus to registers
NAAddr_o	out	24	write address bus to registers

Table 5.3 *Port Map of Request Control Module*

5.3.1.3 OCP Request Module

The task of “OCP Request Module” is to transmit the request to the slave core via CI. This module handles the request phase of the OCP. Figure 5.19 shows the state diagram of the “OCP Request Module”.

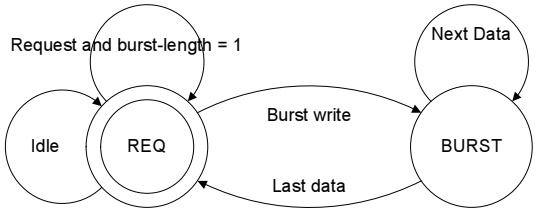


Figure 5.19 *State Diagram of OCP Request Module*

Implementation The “OCP Request Module” is implemented as a Mealy finite state machine.

5.3.2 Response Data-flow

The response data-flow is also divided into three stages. The first stage is where the data are received by the “OCP Response Module” from slave core via the CI. The second stage is where the data are processed and encapsulated by the

“Response Control Module”. The third stage is where the data are transmitted to the network by the “NI Transmit Module” via the NI. The boundary between the stages follows the protocol described in section 5.1.

5.3.2.1 OCP Response Module

The “OCP Response Module” controls the CI. This module uses the OCP to receive response from the CI and forward the response to the “Response Control Module” by using the simple module protocol (see section 5.1).

Figure 5.20 shows the design of the state diagram for the “OCP Response Module”.

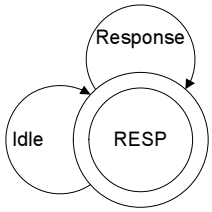


Figure 5.20 *State Diagram of OCP Response Module*

Implementation The “OCP Response Module” is implemented as a Mealy finite state machine.

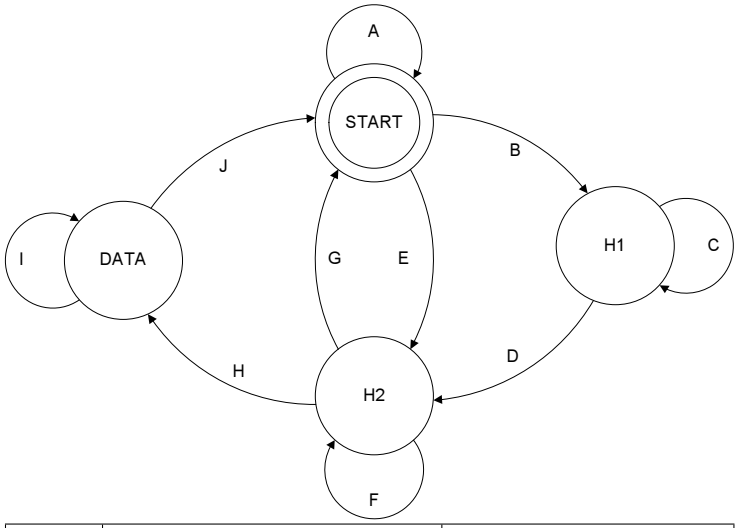
5.3.2.2 Response Control Module

“Response Control Module” is in the second stage of the resonse data-flow. It receives the response from “OCP Response Module” and constructs the network package.

Create Response Package Before the response package is created, the “Response Control Module” gets the information about the thread from the thread information registers, which store the response type and the connection which the response should be sent on. If the response is to be sent in connection zero, the “Response Control Module” creates a network package. If the response is sent on one of the other three connections, a NA package is created.

The “Response Control Module” can find out from the response type register that if the package should be appended with a payload. This is the case for read type responses.

The state diagram of “Response Control Module” is shown in Figure 5.21.



State	Transaction / Condition		Action
START	A	check interrupt **and** wait for response	send interrupt **or** wait
	B	BE response	apply routing path to header
	E	GS response	transmit flit
H1	C	wait for transmission completes	transmit flit
	D	encapsulate next flit	transmit flit
H2	F	wait for transmission completes	transmit flit
	G	transmission completes	get next response
	H	transmission completes	encapsulate next flit
DATA	I	wait for transmission completes **or** transmission completes	transmit flit**or** encapsulate next flit
	J	transmission complete	get next flit

Figure 5.21 *State Diagram of Response Control Module*

Implementation The “Response Control Module” is implemented as a Mealy finite state machine. The port map is shown in Table 5.4.

5.3.2.3 Service Management Registers

There is a register to hold routing path or return port for each input port. If port zero is used the routing path is saved first. If the return path is different from zero the routing path is overwritten with the return port. The threadID is stored in a different register.

Port name / Direction / Width			Description
Clk	in	1	clock signal
Reset_n	in	1	reset signal active low
NIReady_i	in	1	handshake signal from NI receive module
NIDone_o	out	1	handshake signal to NI receive module
NIData_i	in	32	data bus from NI receive module
OCPReady_o	out	1	handshake signal to OCP resp module
OCPDone_i	in	1	handshake signal from OCP resp module
LUTWrite_o	out	1	handshake signal to look-up table
LUTDone_i	in	1	handshake signal from look-up table
LUTAddr_o	out	24	write address bus to look-up table
LUTData_o	out	32	write data bus to look-up table
Port_i	in	2	port indicator from NI receive module
SResp_o	out	2	OCP response field to CI
SThreadID_o	out	8	OCP thread id field to CI

Table 5.4 *Port Map of Response Control Module*

5.3.2.4 Interrupt Module

The Interrupt Module controls the interrupt. Whenever the `SInterrupt` signal on the CI changes, the interrupt module will send a package to set the interrupt in the Slave NA. It functions like a virtual wire with a delay.

implementation The Interrupt Module is implemented as a small finite state machine. One state for each state of the interrupt (i.e. two states corresponding to high and low individually).

5.4 Parametrization

To adapt and optimize the NAs for a given core, all values for signal bus width, memory map, memory and FIFO size, and packages format have been extracted from the implementation.

The parameters related to design are declared in separate package files. The OCP parameters are stored in `ocp.vhd`. The package format is declared in the `package_format.vhd` file. The memory map is declared in `memory_map.vhd` file. The parameters have a relation with the system design and will apply for all instantiations of the NAs.

The parameters related to the signal bus widths, the memory and FIFO sizes and the number of ports in the NI are defined through generics at the instantiation of the NA component. Since not all cores require and use all services and functionalities, it is possible to customize the NA to match its core.

CHAPTER 6

Test and Verification

Test and verification are important phases of digital design. We should find a effective way to find errors and verify the system behavior in relation to the system and design specifications.

6.1 Test Methods

The two test methods we use for testing are module test and system integration test.

6.1.1 Module Test

Our test starts from module level to make sure every module works correctly. Every module in the design has been tested and verified individually. We create a test-bench for each module and run specific test-cases to verify correct behavior of each module. The information about module test cases can be found in Appendix A.

6.1.2 System Integration Test

Once individual modules have been tested, they can be integrated to create a complete system. Our system integration test is developed from the system specification in chapter 4. At this stage we focus on interactions between the modules, the functionalities and performance of the system as a whole. In the rest of this chapter we focus on describing the system integration test.

6.2 System Test Strategy

We use the divide and conquer technique as our test strategy. The Slave NA and Master NA are each divided into six regions. These regions follow the stages of the data-flows, which are described in chapter 5. Figure 6.1 shows the sequence in which the regions are conquered (i.e. verified).

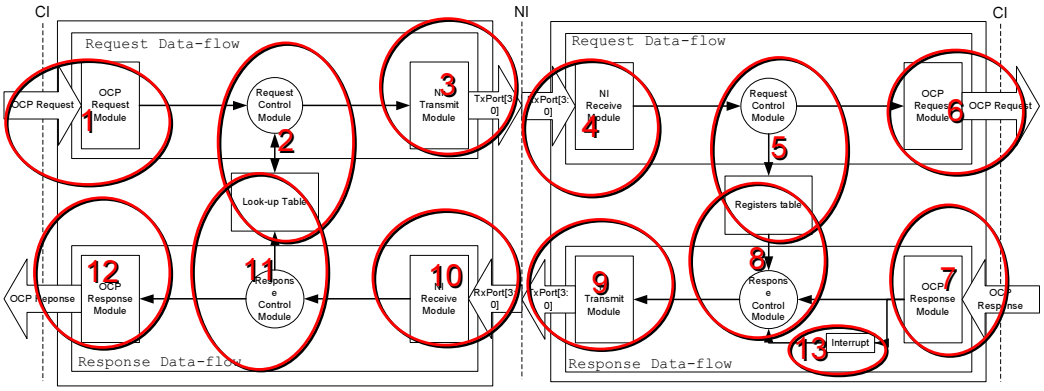


Figure 6.1 *Divide and Conquer Strategy of the System Integration Test*

6.3 System Test-bench

We use CoreCreator tool to create the system test-bench. CoreCreator is developed by Sonics for the OCP-IP Association. It offers several IP cores for test and verification of the OCP. These IP cores can be used to verify the CI and generate test vectors for testing the system. In addition to the CoreCreator's IP cores, we have created our own verification modules for verifying the NI and the behavior of the Slave NA. Figure 6.2 shows the diagram of system test-bench.

6.3.1 Q-Master Core

The Q-Master (Quick Master) is a behavioral model to simulate master cores. It is used to send requests over an OCP interface. This is an easy way to test stimuli to the system, verify the cores functionality and assure OCP compliance.

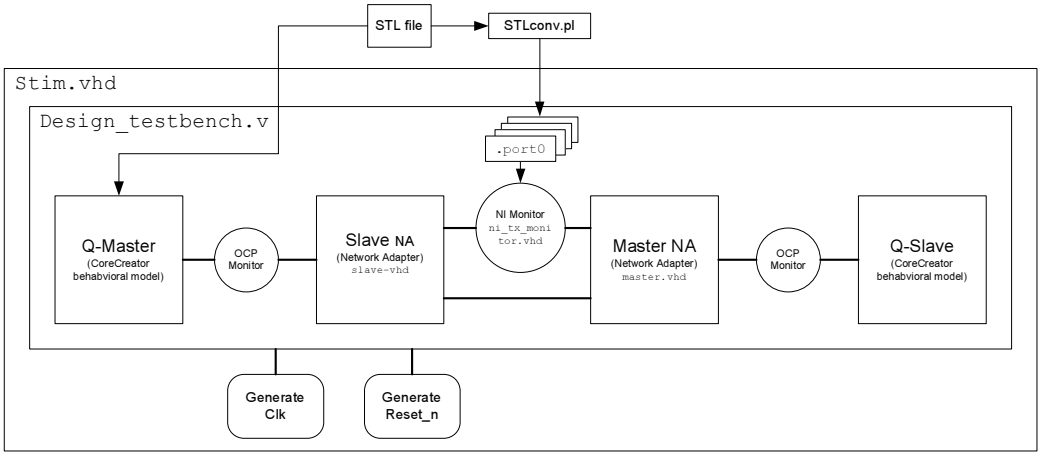


Figure 6.2 *System Test-bench Diagram*

The Q-Master can be controlled by commands read from a *Socket Transaction Language* (STL) script. The STL can easily create test vectors for the Q-Master module. A STL script is read by the Q-Master to generate OCP traffic on its interface. For a list of STL commands and the syntax, see [13]. In this way the Q-Master can be programmed to simulate different master cores, while Q-Master provides the system with OCP-compliant stimuli.

The Q-Master has several parameters which can be configured. They are the latency parameters for different signals in the request, data-handshake and response phase of an OCP transaction. In this system test-bench the Q-Master uses the default values. For a full description of the Q-Master, see [13].

6.3.2 Q-Slave Module

The Q-Slave (Quick Slave) is a behavioral model to simulate simple slave cores, such as memories or I/O devices. The Q-Slave has several parameters, such as response latency, write buffers and read buffers, possibility of read error etc. For a full description of the Q-Slave, see [13].

6.3.3 OCP Monitors

There are two OCP monitors in the system test-bench. The OCP monitor traces the traffic on the OCP interface and writes the result to a log file. The log file can be

analyzed to extract performance data and any violations of the OCP. The content of the log file is very useful for verifying that an interface is OCP-compliant.

6.3.4 STL Script Converter and NI Monitor

The STL Script Converter is a Perl script (`STLconv.pl`) to convert the STL file used by the Q-Master into `std_logic_vector` files. These files are read by "NI Monitor" for comparing with the output of the data sent by the Slave NA. The Perl script stores the same data that the Slave NA uses for its configuration. The Perl script will use them to generate package headers the same way as the Slave NA generates.

We have four `std_logic_vector` output files, one for each transmit port in the Slave NA. To compare the data sent by the Slave NA with the `std_logic_vector` output files, we implement a "NI Monitor", which has four sub-monitors, one for each transmit port. Each sub-monitor compares the data coming from its corresponding port with the `std_logic_vector` output file. It will generate an error if the data do not match the output file. The monitor also checks the NI protocol and generates an error if it is violated.

This will verify if the network packages are created and sent correctly by the Slave NA.

6.4 Test Cases

To verify each region shown in Figure 6.1 the following test cases are used.

Case 1: *Configure Slave NA from CI.* The Q-Master writes to the look-up table to configure the Slave NA. Through this test we validate the correct behavior of region 1 and 2.

Case 2: *Request data-flow of the Slave NA.* The Q-Master sets up GS and BE in the Slave NA. Then the Q-Master sends simple writes and burst writes using these services. The correct behavior of the request data-flow of the Slave NA is validated by the OCP monitor and NI monitor. Region 2 and 3 have been tested.

Case 3: *Configure the Master NA from NI.* The Q-Master sends simple writes to configure the Master NA. We validate the values written to the register table in the Master NA by checking the wave-plot diagrams (see Appendix D) created by ModelSim. Region 4 and 5 have been tested.

Case 4: *Request data-flow of the Master NA.* The Q-Master sends simple writes and burst write to the Q-Slave. We validate the requests in the Master NA's CI by checking the wave-plot diagrams (see Appendix D). Region 5 and 6 have been tested.

Case 5: *Response data-flow of the Master NA.* The Q-Master configures the Slave NA and Master NA to use BE → BE, GS → GS, BE → GS and GS → BE services. The Q-Master writes to the Q-Slave by using simple write and burst write. The Q-Master reads the values just written from the Q-Slave. The read and write values are compared by checking the response on the Slave NA's NI, through the wave-plot diagrams (see Appendix D). Region 7, 8 and 9 have been tested.

Case 6: *Response data-flow of the Slave NA.* The same test as above was used. The read and write values are compared by checking the response on the Slave NA's CI, through the wave-plot diagrams (see Appendix D). Region 10, 11 and 12 have been tested.

6.5 Test Results

During test and verification of the CI, an OCP violation has been detected. This violation was related to a missing response when the NAs were configured. Due to the late discovery and lack of time, OCP-compliance was achieved by disabling `write_resp` in the OCP configuration, resulting in disabling the `WriteNonPost`, `ReadLink` and `WriteConditional` OCP request commands. In Chapter 8 an explanation is given relating to which minor design changes can resolve the problem without reducing features.

The RTL design was tested and verified. No other problems were found and OCP-compliance is therefore achieved.

The synthesized net-list were tested. Its functionality was verified. However, OCP-compliance could not be ascertained because of timing violations.

The following test cases have not been addressed, due to limitations in the test system. These tests need to be performed on a network which is currently not available. Without the availability of such network, the test cases cannot be run.

1. Simultaneously incoming traffic on multiple ports, to test the scheduler, which has been tested in module test but not system test.
2. The routing path conversion in the master request data-flow has only been tested in the module test.

CHAPTER 7

Cost and Performance

The cost and performance of the NAs are a vital part of this project. It is through the cost and performance results that design decisions can be measured.

In this chapter the synthesis results will be presented, and a cost analysis will be made based on the synthesis results by extracting the area and power consumption from the synthesis. The Slave NA's performance and Master NA's performance will be evaluated in terms of speed, throughput, jitter and latency.

7.1 Synthesis Results

The synthesis of the Slave NA and the Master NA has been performed with Synopsys Design Compiler using the *CORELIB8DHS_HCMOS8D_1.8V 3.1* standard cell library from STMicroelectronics[17]. This is a $0.18\mu m$ CMOS technology.

Table 7.1 and Table 7.2 show the area, power and timing parameters displayed in a hierarchical order for each module of the Slave NA and the Master NA.

7.2 Cost Analysis

In this section we will discuss the cost of the implementation of the Slave NA and the Master NA based on the synthesis results. The cost will be discussed in terms of area utilization and power consumption.

Module	Amount	t_{setup} [ns]	t_{delay} [ns]	Power [mW]	Area [μm^2]
slave	1	0.17	4.45	546	182738
• slave_req	1	0.17	4.45		120389
○ slave_req_ocp	1	-	0.43		438
○ slave_req_control	1	0.20	1.38		4579
○ lut	1	0.23	2.40		91926
◇ ram	1	0.14	0.32		1658
◇ cam	1	0.21	1.06		88862
○ ni_tx	1	0.14	1.25		26353
◇ fifo	1	0.14	1.25		16367
◇ ni_tx_port	4	0.20	0.29		258
• slave_resp	1	-	2.00		62349
○ slave_resp_ocp	1	-	0.07		53
○ slave_resp_control	1		0.52		3166
○ ni_rx	1	0.23	1.77		69693
◇ scheduler	1	0.17	1.11		4349
◇ fifo	4	0.14	1.25		16367
◇ ni_rx_port	4	0.22	0.31		258

Table 7.1 *Synthesis Results for Slave NA*

Module	Amount	t_{setup} [ns]	t_{delay} [ns]	Power [mW]	Area [μm^2]
master	1	0.17	4.34	28	120127
• master_req	1	-	2.65		91348
○ master_req_ocp	1	-	0.44		327
○ master_req_control	1	-	1.24		7393
○ master_registers	1	0.14	1.04		23248
◇ ram_1	1	0.14	0.68		16416
◇ ram_2	1	0.14	0.32		2162
○ ni_rx	1	0.23	1.77		69693
◇ scheduler	1	0.17	1.11		4349
◇ fifo	4	0.14	1.25		16367
◇ ni_rx_port	4	0.22	0.31		258
• master_resp	1	-	1.83		28778
○ master_resp_ocp	1	-	0.20		41
○ master_resp_control	1	-	0.88		4767
○ master_interrupt	1	-	0.46		282
○ ni_tx	1	0.14	1.25		26353
◇ fifo	1	0.14	1.25		16367
◇ ni_tx_port	4	0.20	0.29		258

Table 7.2 *Synthesis Results for Master NA*

7.2.1 Area

The size of the NAs is an important metric because it facilitates calculating the interconnection overhead introduced by the MANGO NoC. As a Slave NA and/or a Master NA should be instantiated for each IP core connected to the network, it is desired that the area is small compared to the IP cores.

7.2.1.1 Area of Slave NA

From Table 7.1 it is shown that the CAM (i.e. the routing path table) is very area consuming compared to the total size of the Slave NA. This implementation has a CAM with room for 16 entries. If area is an important factor, a homogeneous network should be considered, then the CAM can be replaced with an algorithm to calculate the routing paths. This will decrease the size considerably.

Other components that are relatively expensive in terms of area occupancy are the buffers in the “NI Transmit Module” and the “NI Receive Module”. We have already chosen a small buffer size, but if the network can be designed so the possibility of congestions is reduced or specific IP cores are immune to the extra latency added when congestion occurs, these buffers can be removed.

7.2.1.2 Area of Master NA

From Table 7.2 it is shown that configuration registers and the buffers consume most of the area utilized by the Master NA. To reduce the configuration registers the number of receive ports or the variety of services must be reduced. A reduction of the area occupied by ports can already be obtained at instantiation, but some IP cores could use them. The other possibility is to remove the storing of routing paths in the Master NA, this removes the GS $\rightarrow$ BE combination of transaction services. The reduction of buffer size has been discussed in the previous section.

Substantial reductions in the area occupancy of the Master NA cannot be made without affecting the correct behavior of the system.

7.2.2 Power

The power consumption results are from the Synopsys synthesis and are based on an estimate were the switching activity on all input ports is set to 50%. This is not a very precise estimate. A power simulation was planed, but do to the limiting time this were not achieved. It would have been interesting to evaluate the power consumption results based on the energy used per transaction. This will however be left for future work.

7.3 Performance

In this section we will present the performance results in terms of speed, latency, jitter and throughput. We will also explain how the measurements are done and under which conditions they were performed.

7.3.1 Speed

The speed of the Slave NA and the Master NA is presented as the maximum frequency which the designs can run. The maximum frequency can be calculated as

$$f_{max} = \frac{1}{c} \tag{7.1}$$

Here c is the longest combinatorial delay in the design i.e. the critical path.

7.3.1.1 Critical Path for Slave NA

The critical path for the Slave NA is $4.41ns$ and goes through the following modules; “NI Receive Module”, FIFO, scheduler, “Response Control Module”, Look-up table and CAM, see Figure 7.1. This path is used when the routing path table is updated from the NI.

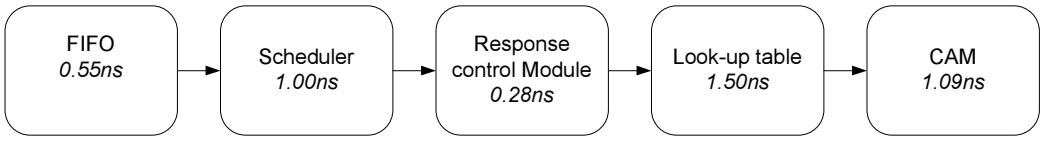


Figure 7.1 *Critical Path for Slave NA*

The critical path results in a maximum frequency for Slave NA at $f_{max} = 226.8MHz$

7.3.1.2 Critical Path for Master NA

The critical path for the Master NA is $4.34ns$ and goes through the following modules; FIFO, scheduler, “Request Control Module”, “OCP Request Module”,

"Request Control Module", scheduler and FIFO, see Figure 7.2. This path is used when a request is sent from a buffer in the "NI Receive Module" to the CI.

Figure 7.2 *Critical Path for Master NA*

The critical path results in a maximum frequency for Master NA at $f_{max} = 230.4MHz$

7.3.2 Latency

The latency is measured for single write requests and single read responses. The measurements are performed on the system test-bench (see section 6.3) after the Slave NA and the Master NA have been initialized. The following condition is assumed in the latency measurements as: the network latency is zero and congestions in network do not occur.

7.3.2.1 Request Latency

We have measured the request latency from a request is issued by the "Q-Master" on the Slave NA's CI to it is received by the "Q-Slave" on the Master NA's CI.

Table 7.3 shows the measurement obtained by the latency simulation on the system test-bench.

Which modules in the request data-flow contribute to the latency are described as following.

Slave OCP Request Module: The CI between the master core and the Slave NA does not introduce any latency.

Slave Request Control Module: The encapsulation of the request takes one clock cycles per package flit.

Slave NI Transmit Module: The synchronization and transmission of a flit take 4 clock cycles. This means the latency introduced for transmitting a request is the number of flits in the request $\times$ 4.

Master NI Receive Module: The synchronization and reception of a flit take 4 clock cycles. This means the latency introduced for receiving a request is the number of flits in the request $\times$ 4.

Data-flow	Service	Request type	Latency[cycles]	Latency[μs]
Request	BE	write	43	0.19
	GS	write	30	0.13
	BE	read	31	0.14
	GS	read	20	0.09
Response	BE	read	31	0.14
	GS	read	17	0.07
	BE	interrupt[1]	20	0.09
	BE	interrupt[1]	10	0.04

Result obtained by using Equation 7.2.

Table 7.3 *Result of Latency Measurements*

Master Request Control: The decapsulation of the request takes one clock cycles per flit in the request.

Master OCP Request Module: The CI between the slave core and "Master NA" does not introduce any latency

The latency can therefore be described as

$$Latency_{Req} = 2 \cdot (flits_{req} + flits_{req} \cdot Latency_{sync}) \tag{7.2}$$

Here $flits_{req}$ is the number of flits in the request package, and $Latency_{sync}$ is the time for synchronization.

7.3.2.2 Response Latency

We have measured the response latency from the time response is issued by the "Q-Slave" in the CI of the Master NA to the time "Q-Master" receives the response in the CI of the Slave NA. The procedure is similar to the request latency measurements.

The list below describes which modules in the response data-flow contribute to the latency.

Master OCP Request Module: The CI between the slave core and the Master NA does not introduce any latency.

Master Request Control Module: The encapsulation of the response takes one clock cycles per package flit.

Master NI Transmit Module: The synchronization and transmission of a flit take 4 clock cycles. This means the latency introduced for transmitting a response is the number of flits in the response $\times$ 4.

Slave NI Receive Module: The synchronization and reception of a flit take 4 clock cycles. This means the latency introduced for receiving a response is the number of flits in the request $\times$ 4.

Slave Request Control: The decapsulation of the response takes one clock cycles per flit in the request.

Slave OCP Request Module: The CI between the master core and the Slave NA does not introduce any latency

The latency for the response can therefore be described in the same way as for the request latency by using Equation 7.2.

7.3.2.3 Jitter in Bursts

For burst read and write, the jitter is measured as the latency between data-word in the burst (i.e. the delta time between two data-words). The jitter was measured to be 4 clock cycles. This is the same as the time it takes to make the synchronization in the NI.

7.3.2.4 Interrupt Latency

The interrupt latency has not been measured through simulation due to the limited time. An estimate has been calculated by using Equation 7.2 with a package-length of two flits for BE and one flit for GS.

7.3.3 Throughput

The throughput measurements are more complicated to perform. The design is based on the fact that the network can be used as buffer (see Chapter 3). In the system test-bench, as there is no network and therefore no buffer, this will lead to congestions. The measurement will be affected by the congestion that will occur during the synchronization. Instead, an approximation of the throughput is made, where it is assumed that the network will not contribute with congestions.

The NI uses four cycles to send one flit. This is due to the synchronization. From this a throughput estimation can be made, based on the synchronization time and package size. The data throughput of the request and response data-flows, in

both the Slave NA and Master NA, can be calculated with Equation 7.3.

$$throughput = \frac{flits\,in\,package - flits\,in\,package\,header}{flits\,in\,package \cdot syncronization\,cycles} \tag{7.3}$$

7.3.3.1 Request Throughput

The request throughput is measured from the Slave NA's CI to the Master NA's CI by sending write requests.

7.3.3.2 Response Throughput

The response throughput is measured from the Master NA's CI to the Slave NA's CI. It is assumed that the responses are from a read requests.

Table 7.4 shows the throughput for the request data-flow and response data-flow for different service types and burst-length. The estimates is based on a clock frequency at $225MHz$.

Data-flow	Service	Burst-length	Throughput[$words/clk$]	Throughput[$Mbit/s$]
Request	BE	1	$\frac{1}{16}$	450
	BE	32	$\frac{32}{140}$	1646
	BE	256	$\frac{256}{1036}$	1880
	GS	1	$\frac{1}{12}$	600
	GS	32	$\frac{32}{136}$	1694
	GS	256	$\frac{256}{1032}$	1786
Request	BE	1	$\frac{1}{12}$	600
	BE	32	$\frac{32}{136}$	1694
	BE	256	$\frac{256}{1032}$	1786
	GS	1	$\frac{1}{8}$	900
	GS	32	$\frac{32}{132}$	1745
	GS	256	$\frac{256}{1028}$	1793

Table 7.4 *Throughput Estimate*

7.3.4 Performance Summary

In Equation 7.2 it clearly shows that the latency introduced by synchronization has a huge impact on the total latency. To lower the latency we suggest that different synchronization methods are investigated. The size of the package (i.e. the package header) is also important. This could be reduced for some requests, but in addition extra hardware will be needed to handle different package headers.

Equation 7.3 shows that the synchronization also has impact on the throughput. Comparing the performance results with the requirements from section 3.1 shows that they are just met. The performance on latency does not leave any room for latency in the network.

When comparing the performance of the NAs with performance of the routers in the MANGO NoC[4], it can be seen that the optimization effort should focus on decreasing the synchronization time. The MANGO routers are running at a frequency of $515MHz$ with worst-case timing parameters (i.e. $795MHz$ with typical timing parameters) on a $0.13\mu m$ technology (the NAs performance results are based on a $0.18\mu m$ technology). If the sampling frequency in the NI can be doubled, it will match the performance of the MANGO routers perfectly. In this case we cannot achieve any benefits through pipelining the NAs. In Chapter 8 we will explain how to decrease the sampling time.

CHAPTER 8

Future Work

In this chapter we will discuss further development of the network adapters. The ordering of the sections in this chapter is the suggested priority for each task.

8.1 Response and Error Handling

In order to debug applications and enable the more advanced OCP requests (i.e. read link and write conditional), a shortcut between the request and response data-flows in the Slave NA needs to be implemented. This will allow the write_resp parameter to be enabled in the OCP configuration. With this parameter enabled every write request will have a response. Then the NA can notify the core if a request results in an error. The error might be a write to an illegal address in the NA, or a request to a core, which is not known by the NA.

It will also enable the write conditional and read link request, which currently are disabled, because the write response is disabled.

Another useful thing for debugging would be if the core could read the configuration registers in the Slave NA. This will also be possible if this shortcut between the request and response data-flow is implemented.

In Figure 8.1 an updated design is shown. It has the capability for error handling in the Slave NA. The modifications are showed with the dashed lines. An extra FIFO needs to be placed between the “Request Control Module” in the request data-flow, and the “Scheduler” in the response data-flow. This is just an extra transmitting and receiving port, which is directly connected.

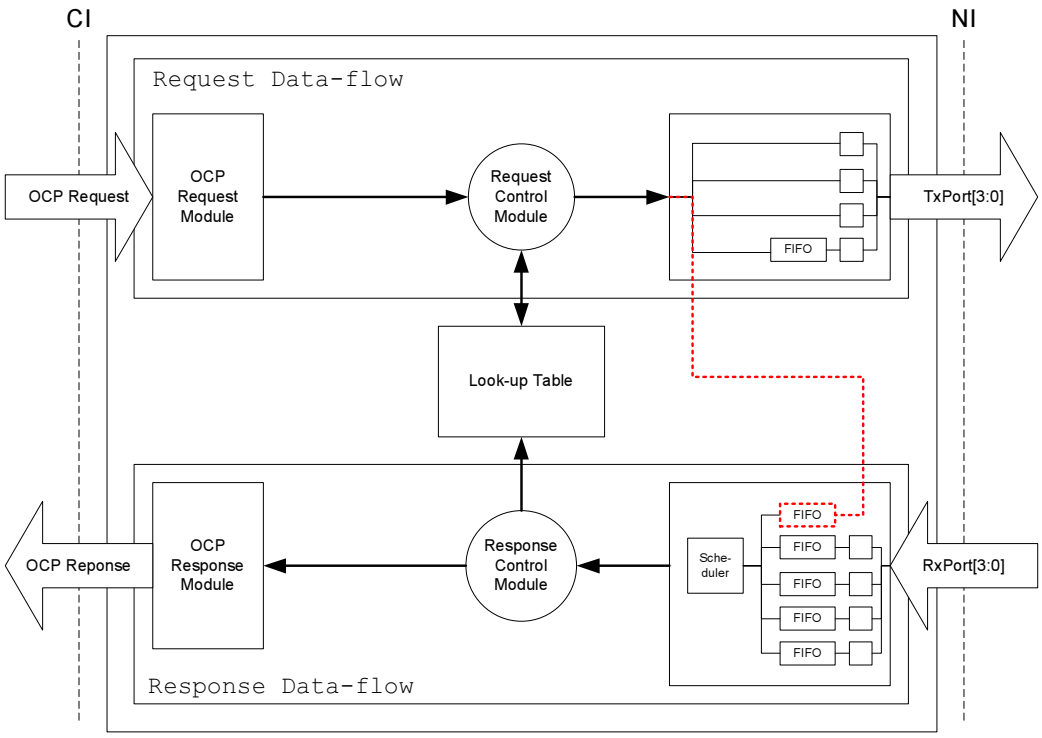


Figure 8.1 *Slave Network Adapter with Response/Error Handling*

8.2 Optimizations

In this section we will discuss different ways to optimize the design. We will look at the synchronization as a way to optimize the performance, and resource sharing as a way to reduce the implementation costs.

8.2.1 Performance

In section 7.3 we showed that the latency introduced by synchronization has a strong impact on performance in terms of throughput and latency. If the synchronization latency can be decreased in relation to the clock frequency on the CI, performance can be gained for both latency and throughput.

We propose two methods for decreasing the synchronization latency in relation to the clock frequency on the CI.

1. *Increase sample frequency.* The sample frequency can easily be doubled by clocking the first flip-flop on the clocks falling edge and second flip flop on the clock's rising edge. Recalculation of MTBF needs to be done in order to issue the quality of the system. This minor change will half the synchronization latency.
2. *Asynchronous four-phase to two-phase converter.* The two-phase protocol is faster because it does not have the RTZ phase. By adding such a converter the latency can be halved.

8.2.2 Cost

An interesting topic is to research benefits of resource sharing in the NAs by implementing multiple CIs. In this way multiple IP cores could share routing path table and buffers, which have major influence on area consumption. The NA for the Æthetial network connects multiple IP cores to the network[15].

CHAPTER 9

Conclusion

The purpose of this M.Sc. project has been to develop a network adapter for the asynchronous MANGO Network-on-Chip. The key requirements have been to provide a standard socket interface using the *open core protocol*, to support guaranteed services and best effort services, and to design and implement the network adapter with low latency and a small area utilization.

A Slave NA and a Master NA have been designed and implemented for the MANGO NoC, in order to comply with the requirements of a wide range of IP cores. The NAs decouple communication from computation through a shared memory abstraction and offer a high level of communication services by providing a standard socket interface using the OCP. They also provide connection based guaranteed services and connection-less source routed best effort services from the MANGO network to the IP cores.

The main achievements of our design and implementation are:

1. Scalability: This is achieved through a modular design by encapsulating each task of the NAs into individual module.
2. Flexibility: This is achieved by parameterizing modules, in this way the NAs adapt easily to specific needs of a wide variety of IP cores.
3. Low latency: The NAs are designed with low latency that allows package flits to be sent every clock period.
4. Low Area: This have been achieved by minimizing the input/output buffers, and instead utilizing the MANGO network for increased buffer capacity.

The implementation of both NAs have been synthesized using a $0.18\mu m$ technology. They have an area of $0.18mm^2$ and $0.13mm^2$, and run at a maximum frequency of $225MHz$.

A cost and performance analysis has been made. The performance analysis shows that reducing synchronization time is the key issue to improve latency, jitter

and throughput performance for both the Slave NA and Master NA.

Abbreviations

AMBA	Microcontroller Bus Architecture
ASIC	Application Specific Integrated Circuit
AXI	Advanced eXtensible Interface
CI	Core Interface
CPU	Central Processing Unit
DMA	Direct Memory Access
DSP	Digital Signal Processor
DTU	Technical University of Denmark
EOP	End Of Package
FIFO	First In, First Out
Flit	FLowcontrol uITs
GALS	Globally Asynchronous Locally Synchronous
I/O	Input/Output
IP	Intellectual Property
LSB	Least Significant Bit
MANGO	Message-passing Asynchronous Network-on-Chip providing Guaranteed services through OCP interfaces
MI	Module Interface
MPEG	Moving Picture Experts Group
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
NA	Network Adapter
NC	Network Controller
NI	Network Interface
NoC	Network-on-Chip

OCP	Open Core Protocol
OSI	Open System Interconnection
RTL	Register Transfer Level
RTZ	Return-To-Zero
STL	Socket Transaction Language
SoC	System-on-Chip
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

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APPENDIX A

Module Test Cases

CAM

1. Write to all addresses in the CAM's address space.
2. Write to addresses out of the CAM's address space.
3. Search for tag that does not exist.
4. Search for tag that exist.
5. Search for tag which has multiple entries.
6. Write to CAM while searching.

RAM

1. Write to all addresses in the RAM's address space.
2. Write to addresses out of the RAM's address space.
3. Write and read from different addresses simultaneously.
4. Write and read from the same addresses simultaneously.

Look-up Table

1. Write to all addresses in the LUT's address space.
2. Write to addresses out of the LUT's address space.
3. Write and read from different addresses simultaneously.
4. Write and read from the same addresses simultaneously.
5. Search for tag that does not exist.

6. Search for tag that exist.
7. Search for tag which has multiple entries.
8. Write to LUT while searching.
9. read and search from LUT simultaneously.
10. read, write and search from LUT simultaneously.
11. write to both write port simultaneously.

FIFO

1. Write to FIFO.
2. Read from FIFO.
3. Test full flag.
4. Test empty flag.
5. Test package flag.
6. write when FIFO is full.
7. Test read when FIFO is empty.
8. read and write simultaneously.
9. read and write simultaneously when FIFO is empty.
10. read and write simultaneously when FIFO is full.

Interrupt

1. Test interrupt from low to high.
2. Test interrupt from high to low.

NI Receive Port

1. Test four phase handshake push protocol.
2. Test Module protocol.

NI Receive Module

1. Test four phase handshake push protocol.

2. Test Module protocol.
3. Test scheduler with data on a BE port.
4. Test scheduler with data on a GS port.
5. Test scheduler with data on a BE port and a GS port.
6. Test scheduler with data on all ports.

NI Transmit Port

1. Test four phase handshake push protocol.
2. Test Module protocol.

NI Transmit Module

1. Test four phase handshake push protocol.
2. Test Module protocol.
3. Test transmitting on different ports.

APPENDIX B

Interface Configurations

```
version 4.0
module "master" {
        core_id 0x0000 0x000 0x0 "Master Network Adapter"
        interface "reset" bundle "reset" {
                interface_type "core"

                port "Reset_n" net "Reset_n"
        }
        interface "rx" bundle "async4phase_push" {
                interface_type "rx"
                prefix "Rx"


                port "Req_i" net "Req"
                port "Ack_o" net "Ack"
                port "Data_i" net "Data"

        }
        interface "tx" bundle "async4phase_push" {
                interface_type "tx"
                prefix "Tx"


                port "Req_o" net "Req"
                port "Ack_i" net "Ack"
                port "Data_o" net "Data"

        }
        interface "ocp2" bundle "ocp2" {
                interface_type "master"
                prefix "OCP"

                param controlbusy 0
                param burstseq_dflt2_enable 0
                param rdlwrc_enable 0
                param respaccept 1
                param burstseq_unkn_enable 0
                param burstseq_xor_enable 1
                param addrspace 0
                param read_enable 1
                param clkctrl_enable 0
                param sdata 1
                param datahandshake 1
                param burstsinglereq 1
                param sreset 0
                param serror 0
                param threads 4
                param writenonpost_enable 0
                param burstlength 1
                param write_enable 1
                param writeresp_enable 0
                param burst_aligned 0
                param status 0
                param reqdata_together 1
                param scanctrl_wdth 0
                param sdatathreadbusy_exact 0
                param burstseq_dflt1_enable 0
                param sthreadbusy 0
                param dataaccept 1
                param broadcast_enable 0
                param reqinfo 0
                param force_aligned 0
```



```
                param mdata 1
                param controlwr 0
                param sflag 0
                param reqlast 1
                param mdatainfo 0
                param jtag_enable 0
                param statusrd 0
                param sdatainfo 0
                param control 0
                param endian 0
                param readex_enable 1
                param mthreadbusy_exact 0
                param burstlength_wdth 8
                param interrupt 1
                param connid 0
                param byteen 0
                param cmdaccept 1
                param jtagtrst_enable 0
                param mflag 0
                param atomiclength 0
                param sdatathreadbusy 0
                param burstseq_strm_enable 1
                param addr_wdth 32
                param merror 0
                param mthreadbusy 0
                param burstprecise 1
                param statusbusy 0
                param addr 1
                param mreset 1
                param burstseq 1
                param respinfo 0
                param mdatabyteen 0
                param burstseq_incr_enable 1
                param burstseq_wrap_enable 1
                param sthreadbusy_exact 0
                param resp 1
                param data_wdth 32
                param scanport 0
                param resplast 1
                param datalast 1

                port "Clk" net "Clk"
                port "MReset_no" net "MReset_n"
                port "MCmd_o" net "MCmd"
                port "MAddr_o" net "MAddr"
                port "MThreadID_o" net "MThreadID"
                port "MDataThreadID_o" net "MDataThreadID"
                port "MBurstLength_o" net "MBurstLength"
                port "MBurstPrecise_o" net "MBurstPrecise"
                port "MBurstSeq_o" net "MBurstSeq"
                port "MBurstSingleReq_o" net "MBurstSingleReq"
                port "MReqLast_o" net "MReqLast"
                port "MDataLast_o" net "MDataLast"
                port "SCmdAccept_i" net "SCmdAccept"
                port "MData_o" net "MData"
                port "MDataValid_o" net "MDataValid"
                port "MDataThreadID_o" net "MDataThreadID"
                port "SDataAccept_i" net "SDataAccept"
                port "SResp_i" net "SResp"
                port "SThreadID_i" net "SThreadID"
                port "SData_i" net "SData"
                port "SRespLast_i" net "SRespLast"
```

```
                port "MRespAccept_o" net "MRespAccept"
                port "SInterrupt_i" net "SInterrupt"

        }
}
```

```
version 4.0
module "slave" {
        core_id 0x0000 0x000 0x0 "Slave Network Adapter"
        interface "reset" bundle "reset" {
                interface_type "core"

                port "Reset_n" net "Reset_n"
        }
        interface "rx" bundle "async4phase_push" {
                interface_type "rx"
                prefix "Rx"


                port "Req_i" net "Req"
                port "Ack_o" net "Ack"
                port "Data_i" net "Data"

        }
        interface "Tx" bundle "async4phase_push" {
                interface_type "tx"


                port "Req_o" net "Req"
                port "Ack_i" net "Ack"
                port "Data_o" net "Data"

        }
        interface "ocp2" bundle "ocp2" {
                interface_type "slave"
                prefix "OCP"

                param controlbusy 0
                param burstseq_dflt2_enable 0
                param rdlwrc_enable 0
                param respaccept 1
                param burstseq_unkn_enable 0
                param burstseq_xor_enable 1
                param addrspace 0
                param read_enable 1
                param clkctrl_enable 0
                param sdata 1
                param datahandshake 1
                param burstsinglereq 1
                param sreset 1
                param serror 0
                param threads 8
                param writenonpost_enable 0
                param burstlength 1
                param write_enable 1
                param writeresp_enable 0
                param burst_aligned 0
                param status 0
                param reqdata_together 1
                param scanctrl_wdth 0
                param sdatathreadbusy_exact 0
                param burstseq_dflt1_enable 0
                param sthreadbusy 0
                param dataaccept 1
                param broadcast_enable 0
                param reqinfo 0
                param force_aligned 0
                param mdata 1
```



```
                param controlwr 0
                param sflag 0
                param reqlast 1
                param mdatainfo 0
                param jtag_enable 0
                param statusrd 0
                param sdatainfo 0
                param control 0
                param endian 0
                param readex_enable 1
                param mthreadbusy_exact 0
                param burstlength_wdth 8
                param interrupt 1
                param connid 1
                param byteen 0
                param cmdaccept 1
                param jtagtrst_enable 0
                param mflag 0
                param atomiclength 0
                param sdatathreadbusy 0
                param burstseq_strm_enable 1
                param addr_wdth 32
                param merror 0
                param mthreadbusy 0
                param burstprecise 1
                param connid_wdth 2
                param statusbusy 0
                param addr 1
                param mreset 0
                param burstseq 1
                param respinfo 0
                param mdatabyteen 0
                param burstseq_incr_enable 1
                param burstseq_wrap_enable 1
                param sthreadbusy_exact 0
                param resp 1
                param data_wdth 32
                param scanport 0
                param resplast 1
                param datalast 1

                port "Clk" net "Clk"
                port "SReset_no" net "SReset_n"
                port "MCmd_i" net "MCmd"
                port "MAddr_i" net "MAddr"
                port "MConnID_i" net "MConnID"
                port "MThreadID_i" net "MThreadID"
                port "MDataThreadID_i" net "MDataThreadID"
                port "MBurstLength_i" net "MBurstLength"
                port "MBurstPrecise_i" net "MBurstPrecise"
                port "MBurstSeq_i" net "MBurstSeq"
                port "MBurstSingleReq_i" net "MBurstSingleReq"
                port "MReqLast_i" net "MReqLast"
                port "MDataLast_i" net "MDataLast"
                port "SCmdAccept_o" net "SCmdAccept"
                port "MData_i" net "MData"
                port "MDataValid_i" net "MDataValid"
                port "SDataAccept_o" net "SDataAccept"
                port "SResp_o" net "SResp"
                port "SThreadID_o" net "SThreadID"
                port "SData_o" net "SData"
                port "SRespLast_o" net "SRespLast"
```

```
                port "MRespAccept_i" net "MRespAccept"
                port "SInterrupt_o" net "SInterrupt"

        }
}
```

APPENDIX C

Synthesis Reports

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : cam_addr_width4_data_width32_tag_width8_size16
Version: 2002.05
Date   : Wed Jan 26 13:43:09 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              88
Number of nets:             2470
Number of cells:            1935
Number of references:         21

Combinational area:       34205.542969
Noncombinational area:    54657.496094
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          88862.718750
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : cam_addr_width4_data_width32_tag_width8_size16
Version: 2002.05
Date   : Wed Jan 26 13:43:19 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: write_data_i
              (input port)
  Endpoint: cam_table_reg[0][DATA][28]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  cam_addr_width4_data_width32_tag_width8_size16
                     maxarea_192000        CORELIB8DHS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock (input port clock) (rise edge)                    0.00       0.00
  input external delay                                    0.00       0.00 r
  write_data_i (in)                                       0.00       0.00 r
  U1442/Z (M_IVHSP)                                       0.04       0.04 f
  U1542/Z (M_ND2HSP)                                      0.08       0.12 r
  U1545/Z (M_BFHSP)                                       0.14       0.26 r
  U1541/Z (M_BFHSP)                                       0.36       0.62 r
  U1537/Z (M_BFHSP)                                       0.43       1.06 r
  cam_table_reg[0][DATA][28]/E (FD7HSP)                   0.00       1.06 r
  data arrival time                                                  1.06

  clock Clk (rise edge)                                  50.00      50.00
  clock network delay (ideal)                             0.00      50.00
  cam_table_reg[0][DATA][28]/CP (FD7HSP)                  0.00      50.00 r
  library setup time                                     -0.21      49.79
  data required time                                                49.79
  --------------------------------------------------------------------------
  data required time                                                49.79
  data arrival time                                                 -1.06
  --------------------------------------------------------------------------
  slack (MET)                                                       48.73


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : fifo_fifo_depth3_data_wdth33
Version: 2002.05
Date   : Wed Jan 26 13:01:44 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               73
Number of nets:               516
Number of cells:              380
Number of references:          19

Combinational area:       6266.876953
Noncombinational area:    10100.729492
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          16367.616211
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : fifo_fifo_depth3_data_wdth33
Version: 2002.05
Date   : Wed Jan 26 13:01:54 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: wr_addr_reg[0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: fifo_reg[2][1]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fifo_fifo_depth3_data_wdth33
                     maxarea_048000        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  wr_addr_reg[0]/CP (F_FD2QHS)             0.00       0.00 r
  wr_addr_reg[0]/Q (F_FD2QHS)              0.22       0.22 r
  U362/Z (M_IVHSP)                         0.14       0.36 f
  U202/Z (M_ND2HSP)                        0.10       0.46 r
  U374/Z (ND2AHS)                          0.16       0.63 r
  U373/Z (M_IVHSP)                         0.39       1.01 f
  U194/Z (F_MUX21HSP)                      0.23       1.25 f
  fifo_reg[2][1]/D (FD7HSP)                0.00       1.25 f
  data arrival time                                   1.25

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  fifo_reg[2][1]/CP (FD7HSP)               0.00      50.00 r
  library setup time                      -0.14      49.86
  data required time                                 49.86
  ----------------------------------------------------------
  data required time                                 49.86
  data arrival time                                  -1.25
  ----------------------------------------------------------
  slack (MET)                                        48.61


1
design_analyzer>
```

```
****************************************
Report : area
Design : lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GSram_size4_B
Ecam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8
Version: 2002.05
Date   : Wed Jan 26 15:10:42 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              164
Number of nets:               258
Number of cells:              118
Number of references:          16

Combinational area:       36286.367188
Noncombinational area:    55640.535156
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          91926.531250
Total area:                 undefined
1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GSram_size4_B
Ecam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8
Version: 2002.05
Date   : Wed Jan 26 15:10:33 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: addr1_i[21]
              (input port)
  Endpoint: cam_1/cam_table_reg[0][DATA][12]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GSram_size4_BEcam_si
ze16_BEcam_addr_wdth4_BEcam_tag_wdth8
                     maxarea_192000        CORELIB8DHS
  cam_addr_width4_data_width32_tag_width8_size16
                     maxarea_192000        CORELIB8DHS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock (input port clock) (rise edge)                    0.00       0.00
  input external delay                                    0.00       0.00 r
  addr1_i[21] (in)                                        0.00       0.00 r
  U95/Z (NR3HSX05)                                        0.10       0.10 f
  U91/Z (F_ND4HS)                                         0.10       0.20 r
  U161/Z (OR3HS)                                          0.17       0.37 r
  U156/Z (AN3HS)                                          0.17       0.54 r
  U150/Z (F_AN2HSP)                                       0.21       0.75 r
  cam_1/write_tag_i (cam_addr_width4_data_width32_tag_width8_size16)
                                                          0.00       0.75 r
  cam_1/U2697/Z (M_IVHSP)                                 0.16       0.91 f
  cam_1/U2696/Z (M_ND2HSP)                                0.40       1.31 r
  cam_1/U2782/Z (M_IVHSP)                                 0.62       1.93 f
  cam_1/U2771/Z (M_IVHSP)                                 0.47       2.40 r
  cam_1/cam_table_reg[0][DATA][12]/E (FD7HSP)             0.00       2.40 r
  data arrival time                                                  2.40

  clock Clk (rise edge)                                  50.00      50.00
  clock network delay (ideal)                             0.00      50.00
  cam_1/cam_table_reg[0][DATA][12]/CP (FD7HSP)            0.00      50.00 r
  library setup time                                     -0.23      49.77
  data required time                                                49.77
  --------------------------------------------------------------------------
  data required time                                                49.77
  data arrival time                                                 -2.40
  --------------------------------------------------------------------------
  slack (MET)                                                       47.37
```



```
1
design_analyzer>
```

```
Warning: In design 'master', there is 1 feedthrough. (LINT-30)
Warning: In design 'master', there are 2 output ports shorted to other output po
rts. (LINT-30)
Warning: In design 'master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localad
dr_wdth24_RxPorts4_fifo_depth3_ram_addr_wdth2_threadid_wdth2', there is 1 submod
ule connected to power or ground. (LINT-30)
Warning: In design 'master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localad
dr_wdth24_RxPorts4_fifo_depth3_ram_addr_wdth2_threadid_wdth2', there is 1 submod
ule with pins connected to the same net. (LINT-30)
Warning: In design 'master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8
_threadid_wdth2_localaddr_wdth24_RxPorts4', there are 7 output ports shorted to
other output ports. (LINT-30)
Warning: In design 'ni_rx_port_data_wdth33_3', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_2', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_1', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_0', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'master_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_thr
eadid_wdth2', there are 77 feedthroughs. (LINT-30)
Warning: In design 'master_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_thr
eadid_wdth2', there is 1 output port shorted to another output port. (LINT-30)
Warning: In design 'master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr
_wdth24_TxPorts4', there is 1 port not connected to any nets. (LINT-30)
Warning: In design 'master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr
_wdth24_TxPorts4', there is 1 submodule connected to power or ground. (LINT-30)
Warning: In design 'master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2', the
re is 1 port not connected to any nets. (LINT-30)
Warning: In design 'master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2', the
re are 37 feedthroughs. (LINT-30)
Warning: In design 'ni_tx_port_data_wdth33_3', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_2', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_1', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_0', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'master_interrupt_data_wdth32_localaddr_wdth24', there are 29
 output ports shorted to other output ports. (LINT-30)

Information: Use the 'check_design' command for
         more information about warnings. (LINT-99)


****************************************
Report : power
        -hier
        -analysis_effort low
Design : master
Version: 2002.05
Date   : Tue Mar  1 11:53:07 2005
****************************************


Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)
```



```
Operating Conditions:
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
master                  maxarea_192000    CORELIB8DHS
master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_RxPorts4_f
ifo_depth3_ram_addr_wdth2_threadid_wdth2
                        maxarea_192000    CORELIB8DHS
master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2_loca
laddr_wdth24_RxPorts4
                        maxarea_007680    CORELIB8DHS
ni_rx_RxPorts4_data_wdth33_fifo_depth3
                        maxarea_192000    CORELIB8DHS
ni_rx_port_data_wdth33_3
                        maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_4
                        maxarea_014080    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_3
                        maxarea_014080    CORELIB8DHS
ni_rx_port_data_wdth33_2
                        maxarea_000960    CORELIB8DHS
ni_rx_port_data_wdth33_1
                        maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_2
                        maxarea_014080    CORELIB8DHS
scheduler_data_wdth33_ports4
                        maxarea_007680    CORELIB8DHS
ni_rx_port_data_wdth33_0
                        maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_1
                        maxarea_014080    CORELIB8DHS
master_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2
                        maxarea_000960    CORELIB8DHS
master_registers_data_wdth32_RxPorts4_ram_addr_wdth2_threadid_wdth2_localaddr_wd
th24
                        maxarea_048000    CORELIB8DHS
ram_data_wdth32_addr_wdth2_size4
                        maxarea_048000    CORELIB8DHS
ram_data_wdth4_addr_wdth2_size4
                        maxarea_003840    CORELIB8DHS
master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4
                        maxarea_048000    CORELIB8DHS
master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4
                        maxarea_007680    CORELIB8DHS
master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2
                        maxarea_000960    CORELIB8DHS
ni_tx_TxPorts4_data_wdth33
                        maxarea_048000    CORELIB8DHS
ni_tx_port_data_wdth33_3
                        maxarea_000960    CORELIB8DHS
ni_tx_port_data_wdth33_2
                        maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_0
                        maxarea_014080    CORELIB8DHS
ni_tx_port_data_wdth33_1
                        maxarea_000960    CORELIB8DHS
ni_tx_port_data_wdth33_0
                        maxarea_000960    CORELIB8DHS
master_interrupt_data_wdth32_localaddr_wdth24
                        maxarea_000960    CORELIB8DHS
```

```
Global Operating Voltage = 1.6
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

Hierarchy	Switch Power	Int Power	Leak Power	Total Power	%
master	10.376	18.375	5.01e+06	28.756	100.0
master_resp_1	1.299	3.625	1.28e+06	4.926	17.1
master_interrupt_1	1.11e-02	5.67e-02	1.24e+04	6.78e-02	0.2
ni_tx_1	0.959	3.217	1.10e+06	4.177	14.5
ni_tx_port_0	3.70e-03	7.22e-02	1.32e+04	7.59e-02	0.3
ni_tx_port_1	3.40e-03	7.17e-02	1.32e+04	7.51e-02	0.3
fifo_1	0.297	2.391	5.60e+05	2.688	9.3
ni_tx_port_3	3.22e-03	7.11e-02	1.32e+04	7.43e-02	0.3
ni_tx_port_2	3.25e-03	7.12e-02	1.32e+04	7.44e-02	0.3
master_resp_ocp_1	1.46e-02	4.36e-03	1.50e+03	1.90e-02	0.1
master_resp_control_1	0.315	0.347	1.64e+05	0.662	2.3
master_req_1	2.101	14.750	3.73e+06	16.855	58.6
master_registers_1	0.222	2.990	9.62e+05	3.213	11.2
ram_2	1.64e-02	0.307	8.72e+04	0.324	1.1
ram_1	0.164	2.145	6.59e+05	2.310	8.0
master_req_ocp_1	2.91e-03	2.44e-02	1.42e+04	2.73e-02	0.1
ni_rx_1	1.620	10.772	2.43e+06	12.395	43.1
fifo_0	0.338	2.556	5.57e+05	2.894	10.1
ni_rx_port_1	6.24e-03	8.55e-02	1.20e+04	9.17e-02	0.3
scheduler_1	0.209	0.190	1.49e+05	0.399	1.4
fifo_1	0.350	2.561	5.57e+05	2.912	10.1
ni_rx_port_0	6.26e-03	8.55e-02	1.20e+04	9.18e-02	0.3
ni_rx_port_2	6.32e-03	8.59e-02	1.20e+04	9.22e-02	0.3
fifo_3	0.344	2.560	5.57e+05	2.904	10.1
fifo_2	0.344	2.558	5.57e+05	2.903	10.1
ni_rx_port_3	6.26e-03	8.55e-02	1.20e+04	9.18e-02	0.3
master_req_control_1	0.256	0.964	3.25e+05	1.220	4.2

```
Current design is 'master'.
{"master"}
design_analyzer> Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
        master_resp_1/ni_tx_1/U48/A master_resp_1/ni_tx_1/U48/Z master_resp_1/ni
_tx_1/U49/A master_resp_1/ni_tx_1/U49/Z
Information: Timing loop detected. (OPT-150)
        master_resp_1/ni_tx_1/U50/A master_resp_1/ni_tx_1/U50/Z master_resp_1/ni
_tx_1/U51/A master_resp_1/ni_tx_1/U51/Z
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U48'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U50'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U52'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U56'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U58'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U60'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U62'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U64'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U66'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U68'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U70'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U72'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U74'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U78'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U80'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U82'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U84'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U86'
```



```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U88'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U90'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U92'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U94'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U96'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U34'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U36'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U38'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U40'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U42'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U44'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U46'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U54'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U76'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U98'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U114'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U116'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U118'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U122'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U124'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
```

```
_tx_1/U126'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U128'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U130'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U132'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U134'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U136'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U138'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U140'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U144'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U146'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U148'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U150'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U152'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U154'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U156'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U158'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U160'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U162'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U100'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U102'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U104'
        to break a timing loop (OPT-314)
```



```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U106'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U108'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U110'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U112'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U120'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U142'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U164'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U180'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U182'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U184'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U188'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U190'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U192'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U194'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U196'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U198'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U200'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U202'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U204'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U206'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U210'
```

```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U212'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U214'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U216'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U218'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U220'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U222'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U224'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U226'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U228'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U166'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U168'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U170'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U172'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U174'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U176'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U178'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U186'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U208'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U230'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U246'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
```



```
_tx_1/U296'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U274'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U252'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U244'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U242'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U240'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U238'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U236'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U234'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U232'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U294'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U292'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U290'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U288'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U286'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U284'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U282'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U280'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U278'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U276'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U272'
        to break a timing loop (OPT-314)
```

```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U270'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U268'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U266'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U264'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U262'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U260'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U258'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U256'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U254'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U250'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'master_resp_1/ni
_tx_1/U248'
        to break a timing loop (OPT-314)

****************************************
Report : area
Design : master
Version: 2002.05
Date   : Tue Mar  1 11:40:01 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              412
Number of nets:               469
Number of cells:                2
Number of references:           2

Combinational area:       54865.714844
Noncombinational area:    65262.148438
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          120127.484375
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
```



```
        -delay max
        -max_paths 1
Design : master
Version: 2002.05
Date   : Tue Mar  1 11:40:01 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: master_req_1/ni_rx_1/fifo_1/count_reg[0]
              (rising edge-triggered flip-flop clocked by OCPClk)
  Endpoint: master_req_1/ni_rx_1/fifo_3/count_reg[1]
            (rising edge-triggered flip-flop clocked by OCPClk)
  Path Group: OCPClk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master             maxarea_192000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_2
                     maxarea_014080        CORELIB8DHS
  ni_rx_RxPorts4_data_wdth33_fifo_depth3
                     maxarea_192000        CORELIB8DHS
  master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2_lo
caladdr_wdth24_RxPorts4
                     maxarea_007680        CORELIB8DHS
  master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_RxPorts4
_fifo_depth3_ram_addr_wdth2_threadid_wdth2
                     maxarea_192000        CORELIB8DHS
  scheduler_data_wdth33_ports4
                     maxarea_007680        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_3
                     maxarea_014080        CORELIB8DHS

  Point                                                          Incr       Path
  ----------------------------------------------------------------------------
  clock OCPClk (rise edge)                                       0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  master_req_1/ni_rx_1/fifo_1/count_reg[0]/CP (F_FD2QHS)
                                                                 0.00       0.00 r
  master_req_1/ni_rx_1/fifo_1/count_reg[0]/Q (F_FD2QHS)
                                                                 0.24       0.24 f
  master_req_1/ni_rx_1/fifo_1/U300/Z (M_ND2HSP)                  0.08       0.32 r
  master_req_1/ni_rx_1/fifo_1/U299/Z (M_IVHSP)                   0.05       0.38 f
  master_req_1/ni_rx_1/fifo_1/fifo_full_o (fifo_fifo_depth3_data_wdth33_2)
                                                                 0.00       0.38 f
  master_req_1/ni_rx_1/U11/Z (M_IVHSP)                           0.07       0.44 r
  master_req_1/ni_rx_1/U7/Z (F_ND2AHSP)                          0.13       0.57 f
  master_req_1/ni_rx_1/scheduler_1/ready_i[1] (scheduler_data_wdth33_ports4)
                                                                 0.00       0.57 f
  master_req_1/ni_rx_1/scheduler_1/U560/Z (M_IVHSP)              0.17       0.74 r
  master_req_1/ni_rx_1/scheduler_1/U526/Z (F_ND2AHSP)            0.08       0.82 f
  master_req_1/ni_rx_1/scheduler_1/U662/Z (AO25HS)               0.10       0.92 r
  master_req_1/ni_rx_1/scheduler_1/U643/Z (F_ND2AHSP)            0.27       1.18 r
  master_req_1/ni_rx_1/scheduler_1/U648/Z (M_IVHSP)              0.12       1.30 f
  master_req_1/ni_rx_1/scheduler_1/U659/Z (AO12HS)               0.49       1.79 r
  master_req_1/ni_rx_1/scheduler_1/data_o[32] (scheduler_data_wdth33_ports4)
                                                                 0.00       1.79 r
  master_req_1/ni_rx_1/NIData_o[32] (ni_rx_RxPorts4_data_wdth33_fifo_depth3)
                                                                 0.00       1.79 r
  master_req_1/master_req_control_1/NIData_i[32] (master_req_control_data_wdth32
```

```
_addr_wdth32_burstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                  0.00       1.79 r
  master_req_1/master_req_control_1/U447/Z (M_IVHSP)      0.14       1.93 f
  master_req_1/master_req_control_1/U401/Z (F_MUX21HSP)
                                                  0.16       2.09 f
  master_req_1/master_req_control_1/U479/Z (F_AO4HS)      0.22       2.31 r
  master_req_1/master_req_control_1/OCPReady_o (master_req_control_data_wdth32_a
ddr_wdth32_burstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                  0.00       2.31 r
  master_req_1/master_req_ocp_1/ReqReady_i (master_req_ocp_data_wdth32_addr_wdth
32_burstlength_wdth8_threadid_wdth2)
                                                  0.00       2.31 r
  master_req_1/master_req_ocp_1/U39/Z (F_AN2HSP)          0.19       2.50 r
  master_req_1/master_req_ocp_1/ReqDone_o (master_req_ocp_data_wdth32_addr_wdth3
2_burstlength_wdth8_threadid_wdth2)
                                                  0.00       2.50 r
  master_req_1/master_req_control_1/OCPDone_i (master_req_control_data_wdth32_ad
dr_wdth32_burstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                  0.00       2.50 r
  master_req_1/master_req_control_1/U449/Z (M_IVHSP)      0.08       2.59 f
  master_req_1/master_req_control_1/U550/Z (AO17NHSP)     0.14       2.73 f
  master_req_1/master_req_control_1/U544/Z (AO25HS)       0.42       3.15 r
  master_req_1/master_req_control_1/NIDone_o (master_req_control_data_wdth32_add
r_wdth32_burstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                  0.00       3.15 r
  master_req_1/ni_rx_1/NIDone_i (ni_rx_RxPorts4_data_wdth33_fifo_depth3)
                                                  0.00       3.15 r
  master_req_1/ni_rx_1/scheduler_1/done_i (scheduler_data_wdth33_ports4)
                                                  0.00       3.15 r
  master_req_1/ni_rx_1/scheduler_1/U654/Z (IVHS)          0.36       3.51 f
  master_req_1/ni_rx_1/scheduler_1/U515/Z (AO22HSX05)     0.20       3.71 r
  master_req_1/ni_rx_1/scheduler_1/done_o[3] (scheduler_data_wdth33_ports4)
                                                  0.00       3.71 r
  master_req_1/ni_rx_1/fifo_3/fifo_read_i (fifo_fifo_depth3_data_wdth33_3)
                                                  0.00       3.71 r
  master_req_1/ni_rx_1/fifo_3/U310/Z (M_ND2HSP)           0.19       3.90 f
  master_req_1/ni_rx_1/fifo_3/U182/Z (F_ND2AHSP)          0.06       3.96 r
  master_req_1/ni_rx_1/fifo_3/U305/Z (M_IVHSP)            0.04       4.00 f
  master_req_1/ni_rx_1/fifo_3/U304/Z (F_EN3HSP)           0.19       4.19 f
  master_req_1/ni_rx_1/fifo_3/U303/Z (F_MUX21HSP)         0.14       4.34 f
  master_req_1/ni_rx_1/fifo_3/count_reg[1]/D (F_FD2QHS)
                                                  0.00       4.34 f
  data arrival time                                          4.34

  clock OCPClk (rise edge)                        5.00       5.00
  clock network delay (ideal)                     0.00       5.00
  master_req_1/ni_rx_1/fifo_3/count_reg[1]/CP (F_FD2QHS)
                                                  0.00       5.00 r
  library setup time                             -0.17       4.83
  data required time                                         4.83
  --------------------------------------------------------------------------
  data required time                                         4.83
  data arrival time                                         -4.34
  --------------------------------------------------------------------------
  slack (MET)                                                0.49


1
design_analyzer>
```

```
Current design is 'master_interrupt_data_wdth32_localaddr_wdth24'.
{"master_interrupt_data_wdth32_localaddr_wdth24"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_interrupt_data_wdth32_localaddr_wdth24
Version: 2002.05
Date   : Tue Mar  1 11:40:57 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               37
Number of nets:                18
Number of cells:               11
Number of references:           7

Combinational area:        155.648010
Noncombinational area:     126.975998
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           282.623993
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_interrupt_data_wdth32_localaddr_wdth24
Version: 2002.05
Date   : Tue Mar  1 11:40:57 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[1]
              (rising edge-triggered flip-flop)
  Endpoint: InterruptReady_o
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_interrupt_data_wdth32_localaddr_wdth24
                     maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  CurrentState_reg[1]/CP (FD4QHSP)         0.00       0.00 r
  CurrentState_reg[1]/Q (FD4QHSP)          0.26       0.26 f
  U31/Z (EOHS)                             0.16       0.42 f
  U30/Z (M_ND2HSP)                         0.04       0.46 r
  InterruptReady_o (out)                   0.00       0.46 r
  data arrival time                                   0.46
```



```
  ----------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : ram_data_wdth32_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 15:50:34 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               70
Number of nets:               482
Number of cells:              316
Number of references:           5

Combinational area:       5931.013184
Noncombinational area:    10485.752930
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          16416.767578
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ram_data_wdth32_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 15:50:41 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: WRAddr_i[1]
              (input port)
  Endpoint: memory_reg[0][1]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ram_data_wdth32_addr_wdth2_size4
                     maxarea_048000        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock (input port clock) (rise edge)     0.00       0.00
  input external delay                     0.00       0.00 f
  WRAddr_i[1] (in)                         0.00       0.00 f
  U151/Z (M_IVHSP)                         0.03       0.03 r
  U189/Z (M_ND2HSP)                        0.06       0.09 f
  U188/Z (M_IVHSP)                         0.33       0.42 r
  U121/Z (F_MUX21HSP)                      0.26       0.68 f
  memory_reg[0][1]/D (FD7HSP)              0.00       0.68 f
  data arrival time                                   0.68

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  memory_reg[0][1]/CP (FD7HSP)             0.00      50.00 r
  library setup time                      -0.14      49.86
  data required time                                 49.86
  ----------------------------------------------------------
  data required time                                 49.86
  data arrival time                                  -0.68
  ----------------------------------------------------------
  slack (MET)                                        49.18


1
design_analyzer>
```

```
****************************************
Report : area
Design : ram_data_wdth4_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 15:52:53 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               14
Number of nets:                74
Number of cells:               48
Number of references:           6

Combinational area:        851.967896
Noncombinational area:    1310.719971
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          2162.687988
Total area:                 undefined
1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ram_data_wdth4_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 15:52:36 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: memory_reg[0][0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: memory_reg[0][0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ram_data_wdth4_addr_wdth2_size4
                     maxarea_003840        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  memory_reg[0][0]/CP (FD7HSP)             0.00       0.00 r
  memory_reg[0][0]/Q (FD7HSP)              0.17       0.17 f
  U42/Z (F_MUX21HSP)                       0.15       0.32 f
  memory_reg[0][0]/D (FD7HSP)              0.00       0.32 f
  data arrival time                                   0.32

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  memory_reg[0][0]/CP (FD7HSP)             0.00      50.00 r
  library setup time                      -0.14      49.86
  data required time                                 49.86
  ----------------------------------------------------------
  data required time                                 49.86
  data arrival time                                  -0.32
  ----------------------------------------------------------
  slack (MET)                                        49.54


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_registers_data_wdth32_RxPorts4_ram_addr_wdth2_threadid_wdth2_loc
aladdr_wdth24
Version: 2002.05
Date   : Wed Jan 26 16:01:06 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              119
Number of nets:               231
Number of cells:              114
Number of references:          17

Combinational area:       8830.977539
Noncombinational area:    14417.909180
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          23248.896484
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_registers_data_wdth32_RxPorts4_ram_addr_wdth2_threadid_wdth2_loc
aladdr_wdth24
Version: 2002.05
Date   : Wed Jan 26 16:01:13 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: WriteAddr_i[1]
              (input port)
  Endpoint: ram_1/memory_reg[0][0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_registers_data_wdth32_RxPorts4_ram_addr_wdth2_threadid_wdth2_localaddr_
wdth24
                     maxarea_048000        CORELIB8DHS
  ram_data_wdth32_addr_wdth2_size4
                     maxarea_048000        CORELIB8DHS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock (input port clock) (rise edge)                    0.00       0.00
  input external delay                                    0.00       0.00 f
  WriteAddr_i[1] (in)                                     0.00       0.00 f
  U305/Z (AO20HSX05)                                      0.11       0.11 r
  U317/Z (F_ND4HS)                                        0.10       0.21 f
  U315/Z (NR3HSX05)                                       0.22       0.43 r
  U330/Z (M_IVHSP)                                        0.11       0.55 f
  U314/Z (M_ND3HSP)                                       0.06       0.61 r
  U364/Z (M_IVHSP)                                        0.07       0.68 f
  ram_1/WriteEnable_i (ram_data_wdth32_addr_wdth2_size4)
                                                          0.00       0.68 f
  ram_1/U187/Z (M_BFHSP)                                  0.14       0.83 f
  ram_1/U134/Z (M_BFHSP)                                  0.21       1.04 f
  ram_1/memory_reg[0][0]/E (FD7HSP)                       0.00       1.04 f
  data arrival time                                                  1.04

  clock Clk (rise edge)                                  50.00      50.00
  clock network delay (ideal)                             0.00      50.00
  ram_1/memory_reg[0][0]/CP (FD7HSP)                      0.00      50.00 r
  library setup time                                     -0.14      49.86
  data required time                                                49.86
  --------------------------------------------------------------------------
  data required time                                                49.86
  data arrival time                                                 -1.04
  --------------------------------------------------------------------------
  slack (MET)                                                       48.82


1
design_analyzer>
```

```
Current design is 'master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localadd
r_wdth24_RxPorts4_fifo_depth3_ram_addr_wdth2_threadid_wdth2'.
{"master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_RxPorts4
_fifo_depth3_ram_addr_wdth2_threadid_wdth2"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_R
xPorts4_fifo_depth3_ram_addr_wdth2_threadid_wdth2
Version: 2002.05
Date   : Tue Mar  1 11:42:05 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              289
Number of nets:               434
Number of cells:                4
Number of references:           4

Combinational area:       37662.554688
Noncombinational area:    53686.722656
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          91348.992188
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_R
xPorts4_fifo_depth3_ram_addr_wdth2_threadid_wdth2
Version: 2002.05
Date   : Tue Mar  1 11:42:05 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: ni_rx_1/fifo_1/count_reg[0]
              (rising edge-triggered flip-flop)
  Endpoint: MCmd_o[2] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_req_data_wdth32_addr_wdth32_burstlength_wdth8_localaddr_wdth24_RxPorts4
_fifo_depth3_ram_addr_wdth2_threadid_wdth2
                     maxarea_192000        CORELIB8DHS
  ni_rx_RxPorts4_data_wdth33_fifo_depth3
                     maxarea_192000        CORELIB8DHS
  master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2_lo
caladdr_wdth24_RxPorts4
                     maxarea_007680        CORELIB8DHS
```



```
  fifo_fifo_depth3_data_wdth33_2
                     maxarea_014080        CORELIB8DHS
  scheduler_data_wdth33_ports4
                     maxarea_007680        CORELIB8DHS

  Point                                                          Incr       Path
  ---------------------------------------------------------------------------
  ni_rx_1/fifo_1/count_reg[0]/CP (F_FD2QHS)                      0.00       0.00 r
  ni_rx_1/fifo_1/count_reg[0]/Q (F_FD2QHS)                       0.24       0.24 f
  ni_rx_1/fifo_1/U300/Z (M_ND2HSP)                               0.08       0.32 r
  ni_rx_1/fifo_1/U299/Z (M_IVHSP)                                0.05       0.38 f
  ni_rx_1/fifo_1/fifo_full_o (fifo_fifo_depth3_data_wdth33_2)
                                                                 0.00       0.38 f
  ni_rx_1/U11/Z (M_IVHSP)                                        0.07       0.44 r
  ni_rx_1/U7/Z (F_ND2AHSP)                                       0.13       0.57 f
  ni_rx_1/scheduler_1/ready_i[1] (scheduler_data_wdth33_ports4)
                                                                 0.00       0.57 f
  ni_rx_1/scheduler_1/U560/Z (M_IVHSP)                           0.17       0.74 r
  ni_rx_1/scheduler_1/U526/Z (F_ND2AHSP)                         0.08       0.82 f
  ni_rx_1/scheduler_1/U662/Z (AO25HS)                            0.10       0.92 r
  ni_rx_1/scheduler_1/U643/Z (F_ND2AHSP)                         0.27       1.18 r
  ni_rx_1/scheduler_1/U648/Z (M_IVHSP)                           0.12       1.30 f
  ni_rx_1/scheduler_1/U659/Z (AO12HS)                            0.49       1.79 r
  ni_rx_1/scheduler_1/data_o[32] (scheduler_data_wdth33_ports4)
                                                                 0.00       1.79 r
  ni_rx_1/NIData_o[32] (ni_rx_RxPorts4_data_wdth33_fifo_depth3)
                                                                 0.00       1.79 r
  master_req_control_1/NIData_i[32] (master_req_control_data_wdth32_addr_wdth32_
burstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                                 0.00       1.79 r
  master_req_control_1/U447/Z (M_IVHSP)                          0.14       1.93 f
  master_req_control_1/U401/Z (F_MUX21HSP)                       0.16       2.09 f
  master_req_control_1/U479/Z (F_AO4HS)                          0.22       2.31 r
  master_req_control_1/OCPReady_o (master_req_control_data_wdth32_addr_wdth32_bu
rstlength_wdth8_threadid_wdth2_localaddr_wdth24_RxPorts4)
                                                                 0.00       2.31 r
  master_req_ocp_1/ReqReady_i (master_req_ocp_data_wdth32_addr_wdth32_burstlengt
h_wdth8_threadid_wdth2)
                                                                 0.00       2.31 r
  master_req_ocp_1/U48/Z (F_AN2HSP)                              0.23       2.54 r
  master_req_ocp_1/U43/Z (F_AN2HSP)                              0.11       2.65 r
  master_req_ocp_1/MCmd_o[2] (master_req_ocp_data_wdth32_addr_wdth32_burstlength
_wdth8_threadid_wdth2)
                                                                 0.00       2.65 r
  MCmd_o[2] (out)                                                0.00       2.65 r
  data arrival time                                                         2.65
  ---------------------------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_
threadid_wdth2_localaddr_wdth24_RxPorts4'.
{"master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2_lo
caladdr_wdth24_RxPorts4"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_w
dth2_localaddr_wdth24_RxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:41:45 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              148
Number of nets:               292
Number of cells:              247
Number of references:          28

Combinational area:       3612.675293
Noncombinational area:    3780.605957
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          7393.279785
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_w
dth2_localaddr_wdth24_RxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:41:45 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[3]
              (rising edge-triggered flip-flop)
  Endpoint: NAAddr_o[5]
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_req_control_data_wdth32_addr_wdth32_burstlength_wdth8_threadid_wdth2_lo
caladdr_wdth24_RxPorts4
                     maxarea_007680        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  CurrentState_reg[3]/CP (F_FD2HS)         0.00       0.00 r
```



```
  CurrentState_reg[3]/QN (F_FD2HS)         0.31       0.31 f
  U460/Z (M_ND3HSP)                        0.13       0.44 r
  U543/Z (F_ND2AHSP)                       0.25       0.69 r
  U512/Z (M_ND3HSP)                        0.17       0.86 f
  U513/Z (M_IVHSP)                         0.20       1.06 r
  U498/Z (AO6NHSP)                         0.17       1.24 r
  NAAddr_o[5] (out)                        0.00       1.24 r
  data arrival time                                   1.24
  ----------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

Appendix C **master_resp.report** Page 1/7

```
Current design is 'master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_
wdth24_TxPorts4'.
{"master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4"}
design_analyzer> Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
        ni_tx_1/U48/A ni_tx_1/U48/Z ni_tx_1/U49/A ni_tx_1/U49/Z
Information: Timing loop detected. (OPT-150)
        ni_tx_1/U50/A ni_tx_1/U50/Z ni_tx_1/U51/A ni_tx_1/U51/Z
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U48'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U50'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U52'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U56'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U58'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U60'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U62'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U64'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U66'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U68'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U70'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U72'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U74'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U78'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U80'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U82'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U84'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U86'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U88'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U90'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U92'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U94'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U96'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U34'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U36'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U38'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U40'
         to break a timing loop (OPT-314)
```

Appendix C **master_resp.report** Page 2/7

```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U42'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U44'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U46'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U54'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U76'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U98'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U114'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U116'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U118'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U122'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U124'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U126'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U128'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U130'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U132'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U134'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U136'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U138'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U140'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U144'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U146'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U148'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U150'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U152'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U154'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U156'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U158'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U160'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U162'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U100'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U102'
         to break a timing loop (OPT-314)
```

```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U104'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U106'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U108'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U110'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U112'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U120'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U142'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U164'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U180'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U182'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U184'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U188'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U190'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U192'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U194'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U196'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U198'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U200'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U202'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U204'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U206'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U210'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U212'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U214'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U216'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U218'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U220'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U222'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U224'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U226'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U228'
         to break a timing loop (OPT-314)
```



```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U166'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U168'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U170'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U172'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U174'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U176'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U178'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U186'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U208'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U230'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U246'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U296'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U274'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U252'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U244'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U242'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U240'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U238'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U236'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U234'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U232'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U294'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U292'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U290'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U288'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U286'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U284'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U282'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U280'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U278'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U276'
         to break a timing loop (OPT-314)
```

```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U272'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U270'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U268'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U266'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U264'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U262'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U260'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U258'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U256'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U254'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U250'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U248'
         to break a timing loop (OPT-314)

****************************************
Report : area
Design : master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_wdth24_TxP
orts4
Version: 2002.05
Date   : Tue Mar  1 11:41:17 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              242
Number of nets:               351
Number of cells:                4
Number of references:           4

Combinational area:       17203.177734
Noncombinational area:    11575.287109
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          28778.496094
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_wdth24_TxP
orts4
Version: 2002.05
Date   : Tue Mar  1 11:41:17 2005
****************************************
```



```
Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: master_interrupt_1/CurrentState_reg[1]
              (rising edge-triggered flip-flop)
  Endpoint: MRespAccept_o
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_resp_data_wdth32_addr_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4
                     maxarea_048000        CORELIB8DHS
  master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4
                     maxarea_007680        CORELIB8DHS
  master_interrupt_data_wdth32_localaddr_wdth24
                     maxarea_000960        CORELIB8DHS
  ni_tx_TxPorts4_data_wdth33
                     maxarea_048000        CORELIB8DHS

  Point                                                            Incr       Path
  ------------------------------------------------------------------------------
  master_interrupt_1/CurrentState_reg[1]/CP (FD4QHSP)     0.00       0.00 r
  master_interrupt_1/CurrentState_reg[1]/Q (FD4QHSP)      0.26       0.26 f
  master_interrupt_1/U31/Z (EOHS)                         0.16       0.42 f
  master_interrupt_1/U30/Z (M_ND2HSP)                     0.08       0.50 r
  master_interrupt_1/InterruptReady_o (master_interrupt_data_wdth32_localaddr_wd
th24)
                                                          0.00       0.50 r
  master_resp_control_1/InterruptReady_i (master_resp_control_data_wdth32_thread
id_wdth2_localaddr_wdth24_TxPorts4)
                                                          0.00       0.50 r
  master_resp_control_1/U336/Z (F_ND2AHSP)                0.09       0.59 f
  master_resp_control_1/U240/Z (F_AN2HSP)                 0.10       0.70 f
  master_resp_control_1/U365/Z (AO23HS)                   0.08       0.77 r
  master_resp_control_1/U362/Z (AO17NHSP)                 0.17       0.94 r
  master_resp_control_1/NIPort_o[0] (master_resp_control_data_wdth32_threadid_wd
th2_localaddr_wdth24_TxPorts4)
                                                          0.00       0.94 r
  ni_tx_1/port_i[0] (ni_tx_TxPorts4_data_wdth33)          0.00       0.94 r
  ni_tx_1/U19/Z (M_IVHSP)                                 0.07       1.01 f
  ni_tx_1/U30/Z (M_ND2HSP)                                0.08       1.10 r
  ni_tx_1/U29/Z (M_IVHSX4)                                0.27       1.37 f
  ni_tx_1/U20/Z (F_AO10NHSP)                              0.28       1.64 f
  ni_tx_1/Done_o (ni_tx_TxPorts4_data_wdth33)             0.00       1.64 f
  master_resp_control_1/NIDone_i (master_resp_control_data_wdth32_threadid_wdth2
_localaddr_wdth24_TxPorts4)
                                                          0.00       1.64 f
  master_resp_control_1/U320/Z (F_AN2HSP)                 0.11       1.75 f
  master_resp_control_1/OCPDone_o (master_resp_control_data_wdth32_threadid_wdth
2_localaddr_wdth24_TxPorts4)
                                                          0.00       1.75 f
  master_resp_ocp_1/RespDone_i (master_resp_ocp_data_wdth32_addr_wdth32_threadid
_wdth2)
                                                          0.00       1.75 f
  master_resp_ocp_1/U13/Z (F_AN2HSP)                      0.08       1.83 f
  master_resp_ocp_1/MRespAccept_o (master_resp_ocp_data_wdth32_addr_wdth32_threa
did_wdth2)
                                                          0.00       1.83 f
  MRespAccept_o (out)                                     0.00       1.83 f
  data arrival time                                                  1.83
```

```
  ---------------------------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth
24_TxPorts4'.
{"master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts
4
Version: 2002.05
Date   : Tue Mar  1 11:40:45 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              172
Number of nets:               307
Number of cells:              171
Number of references:          27

Combinational area:       2686.975098
Noncombinational area:    2080.768555
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          4767.744141
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts
4
Version: 2002.05
Date   : Tue Mar  1 11:40:45 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[2]
              (rising edge-triggered flip-flop)
  Endpoint: InterruptDone_o
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_resp_control_data_wdth32_threadid_wdth2_localaddr_wdth24_TxPorts4
                     maxarea_007680        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  CurrentState_reg[2]/CP (F_FD2HS)         0.00       0.00 r
  CurrentState_reg[2]/QN (F_FD2HS)         0.30       0.30 f
  U314/Z (M_ND3HSP)                        0.11       0.41 r
```



```
  U336/Z (F_ND2AHSP)                       0.12       0.53 r
  U333/Z (M_IVHSP)                         0.22       0.75 f
  U258/Z (F_AN2HSP)                        0.13       0.88 f
  InterruptDone_o (out)                    0.00       0.88 f
  data arrival time                                   0.88
  ----------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2'.
{"master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2
Version: 2002.05
Date   : Tue Mar  1 11:41:31 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               79
Number of nets:                41
Number of cells:                2
Number of references:           2

Combinational area:         40.959999
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:            40.959999
Total area:                 undefined
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2
Version: 2002.05
Date   : Tue Mar  1 11:41:31 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: SResp_i[1] (input port)
  Endpoint: MRespAccept_o
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  master_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth2
                     maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  input external delay                     0.00       0.00 f
  SResp_i[1] (in)                          0.00       0.00 f
  U14/Z (AO7NHSP)                          0.12       0.12 f
  U13/Z (F_AN2HSP)                         0.08       0.20 f
  MRespAccept_o (out)                      0.00       0.20 f
  data arrival time                                   0.20
  ----------------------------------------------------------
```



```
  (Path is unconstrained)


1
design_analyzer>
```

```
****************************************
Report : area
Design : ni_rx_RxPorts4_data_wdth33_fifo_depth3
Version: 2002.05
Date   : Wed Jan 26 13:13:35 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              179
Number of nets:               467
Number of cells:               17
Number of references:          11

Combinational area:       28311.416016
Noncombinational area:    41382.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          69693.437500
Total area:                 undefined
1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ni_rx_RxPorts4_data_wdth33_fifo_depth3
Version: 2002.05
Date   : Wed Jan 26 13:13:27 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: fifo_1/count_reg[0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: fifo_3/count_reg[1]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ni_rx_RxPorts4_data_wdth33_fifo_depth3
                     maxarea_192000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_1
                     maxarea_048000        CORELIB8DHS
  scheduler_data_wdth33_ports4
                     maxarea_007680        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_2
                     maxarea_048000        CORELIB8DHS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock Clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  fifo_1/count_reg[0]/CP (F_FD2QHS)                       0.00       0.00 r
  fifo_1/count_reg[0]/Q (F_FD2QHS)                        0.23       0.23 f
  fifo_1/U800/Z (M_ND2HSP)                                0.10       0.32 r
  fifo_1/U799/Z (M_IVHSP)                                 0.06       0.39 f
  fifo_1/fifo_full_o (fifo_fifo_depth3_data_wdth33_1)     0.00       0.39 f
  U20/Z (M_IVHSP)                                         0.06       0.45 r
  U15/Z (F_ND2AHSP)                                       0.14       0.60 f
  scheduler_1/ready_i[1] (scheduler_data_wdth33_ports4)
                                                          0.00       0.60 f
  scheduler_1/U829/Z (M_IVHSP)                            0.17       0.77 r
  scheduler_1/U852/Z (AO27HSX05)                          0.21       0.97 f
  scheduler_1/U722/Z (F_ND2AHSP)                          0.14       1.11 f
  scheduler_1/U724/Z (M_IVHSP)                            0.04       1.15 r
  scheduler_1/U843/Z (AO17NHSP)                           0.10       1.25 r
  scheduler_1/done_o[3] (scheduler_data_wdth33_ports4)
                                                          0.00       1.25 r
  fifo_3/fifo_read_i (fifo_fifo_depth3_data_wdth33_2)     0.00       1.25 r
  fifo_3/U685/Z (M_ND2HSP)                                0.10       1.34 f
  fifo_3/U681/Z (EOHS)                                    0.20       1.54 f
  fifo_3/U694/Z (AO7NHSP)                                 0.14       1.68 f
  fifo_3/U870/Z (AO23HS)                                  0.09       1.77 r
  fifo_3/count_reg[1]/D (F_FD2QHS)                        0.00       1.77 r
  data arrival time                                                  1.77

  clock Clk (rise edge)                                  50.00      50.00
```



```
  clock network delay (ideal)                             0.00      50.00
  fifo_3/count_reg[1]/CP (F_FD2QHS)                       0.00      50.00 r
  library setup time                                     -0.23      49.77
  data required time                                                49.77
  --------------------------------------------------------------------------
  data required time                                                49.77
  data arrival time                                                 -1.77
  --------------------------------------------------------------------------
  slack (MET)                                                       48.00


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : ni_rx_port_data_wdth33
Version: 2002.05
Date   : Wed Jan 26 13:07:14 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               72
Number of nets:                45
Number of cells:                7
Number of references:           6

Combinational area:         53.248001
Noncombinational area:     204.800003
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           258.048004
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ni_rx_port_data_wdth33
Version: 2002.05
Date   : Wed Jan 26 13:07:24 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: CurrentState_reg
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ni_rx_port_data_wdth33
                     maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  CurrentState_reg/CP (F_FD2HS)            0.00       0.00 r
  CurrentState_reg/QN (F_FD2HS)            0.24       0.24 f
  U25/Z (F_AO6HS)                          0.06       0.31 r
  CurrentState_reg/D (F_FD2HS)             0.00       0.31 r
  data arrival time                                   0.31

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  CurrentState_reg/CP (F_FD2HS)            0.00      50.00 r
  library setup time                      -0.22      49.78
  data required time                                 49.78
  ----------------------------------------------------------
  data required time                                 49.78
  data arrival time                                  -0.31
  ----------------------------------------------------------
  slack (MET)                                        49.48


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
        U48/A U48/Z U49/A U49/Z
Information: Timing loop detected. (OPT-150)
        U50/A U50/Z U51/A U51/Z
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U48'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U50'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U52'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U56'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U58'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U60'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U62'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U64'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U66'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U68'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U70'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U72'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U74'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U78'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U80'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U82'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U84'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U86'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U88'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U90'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U92'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U94'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U96'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U34'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U36'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U38'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U40'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U42'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U44'
```



```
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U46'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U54'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U76'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U98'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U114'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U116'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U118'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U122'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U124'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U126'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U128'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U130'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U132'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U134'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U136'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U138'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U140'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U144'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U146'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U148'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U150'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U152'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U154'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U156'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U158'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U160'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U162'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U100'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U102'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U104'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U106'
```

```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U108'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U110'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U112'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U120'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U142'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U164'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U180'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U182'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U184'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U188'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U190'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U192'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U194'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U196'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U198'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U200'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U202'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U204'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U206'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U210'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U212'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U214'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U216'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U218'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U220'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U222'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U224'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U226'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U228'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U166'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U168'
```



```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U170'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U172'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U174'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U176'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U178'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U186'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U208'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U230'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U246'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U296'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U274'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U252'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U244'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U242'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U240'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U238'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U236'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U234'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U232'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U294'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U292'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U290'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U288'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U286'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U284'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U282'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U280'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U278'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U276'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U272'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U270'
```

```
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U268'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U266'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U264'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U262'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U260'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U258'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U256'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U254'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U250'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'U248'
         to break a timing loop (OPT-314)

****************************************
Report : area
Design : ni_tx
Version: 2002.05
Date   : Wed Jan 26 12:34:38 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              179
Number of nets:               502
Number of cells:              290
Number of references:          13

Combinational area:       15499.281250
Noncombinational area:    10854.391602
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          26353.664062
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ni_tx
Version: 2002.05
Date   : Wed Jan 26 12:34:50 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: fifo_1/wr_addr_reg[0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: fifo_1/fifo_reg[2][1]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ni_tx              maxarea_048000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33
                     maxarea_048000        CORELIB8DHS

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  fifo_1/wr_addr_reg[0]/CP (F_FD2QHS)      0.00       0.00 r
  fifo_1/wr_addr_reg[0]/Q (F_FD2QHS)       0.22       0.22 r
  fifo_1/U362/Z (M_IVHSP)                  0.14       0.36 f
  fifo_1/U212/Z (M_ND2HSP)                 0.10       0.46 r
  fifo_1/U374/Z (ND2AHS)                   0.16       0.63 r
  fifo_1/U373/Z (M_IVHSP)                  0.39       1.01 f
  fifo_1/U208/Z (F_MUX21HSP)               0.23       1.25 f
  fifo_1/fifo_reg[2][1]/D (FD7HSP)         0.00       1.25 f
  data arrival time                                   1.25

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  fifo_1/fifo_reg[2][1]/CP (FD7HSP)        0.00      50.00 r
  library setup time                      -0.14      49.86
  data required time                                 49.86
  -----------------------------------------------------------
  data required time                                 49.86
  data arrival time                                  -1.25
  -----------------------------------------------------------
  slack (MET)                                        48.61


1
design_analyzer>
```

```
****************************************
Report : area
Design : ni_tx_port
Version: 2002.05
Date   : Wed Jan 26 12:31:53 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               70
Number of nets:                45
Number of cells:                9
Number of references:           5

Combinational area:         69.632004
Noncombinational area:     188.416000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           258.048004
Total area:                 undefined
1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ni_tx_port
Version: 2002.05
Date   : Wed Jan 26 12:31:32 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: CurrentState_reg
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ni_tx_port         maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  CurrentState_reg/CP (F_FD2QHS)           0.00       0.00 r
  CurrentState_reg/Q (F_FD2QHS)            0.14       0.14 r
  U25/Z (M_IVHSP)                          0.04       0.18 f
  U24/Z (F_ND2AHSP)                        0.03       0.21 r
  U28/Z (F_AN2HSP)                         0.08       0.29 r
  CurrentState_reg/D (F_FD2QHS)            0.00       0.29 r
  data arrival time                                   0.29

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  CurrentState_reg/CP (F_FD2QHS)           0.00      50.00 r
  library setup time                      -0.20      49.80
  data required time                                 49.80
  ----------------------------------------------------------
  data required time                                 49.80
  data arrival time                                  -0.29
  ----------------------------------------------------------
  slack (MET)                                        49.51


1
design_analyzer>
```

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : scheduler
Version: 2002.05
Date   : Wed Jan 26 12:29:57 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              179
Number of nets:               314
Number of cells:              175
Number of references:          32

Combinational area:       4190.207031
Noncombinational area:     159.744003
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          4349.952148
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : scheduler
Version: 2002.05
Date   : Wed Jan 26 12:30:21 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[2]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: CurrentState_reg[2]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  scheduler          maxarea_007680        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  CurrentState_reg[2]/CP (F_FD2QHS)        0.00       0.00 r
  CurrentState_reg[2]/Q (F_FD2QHS)         0.24       0.24 r
  U593/Z (M_IVHSP)                         0.14       0.38 f
  U552/Z (M_ND2HSP)                        0.10       0.47 r
  U606/Z (F_ND2AHSP)                       0.14       0.62 r
  U522/Z (AO4NHSP)                         0.14       0.76 r
  U662/Z (AO27HSX05)                       0.08       0.84 f
  U519/Z (F_MUX21HSP)                      0.16       1.00 f
  U517/Z (AO1NHSP)                         0.11       1.11 f
  CurrentState_reg[2]/D (F_FD2QHS)         0.00       1.11 f
  data arrival time                                   1.11

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  CurrentState_reg[2]/CP (F_FD2QHS)        0.00      50.00 r
  library setup time                      -0.17      49.83
  data required time                                 49.83
  ----------------------------------------------------------
  data required time                                 49.83
  data arrival time                                  -1.11
  ----------------------------------------------------------
  slack (MET)                                        48.71


1
design_analyzer>
```

```
Warning: In design 'slave', there is 1 feedthrough. (LINT-30)
Warning: In design 'slave', there is 1 submodule connected to power or ground. (
LINT-30)
Warning: In design 'slave', there is 1 submodule with pins connected to the same
 net. (LINT-30)
Warning: In design 'slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_w
dth2_threadid_wdth3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEca
m_size16_BEcam_addr_wdth4_BEcam_tag_wdth8', there are 8 ports not connected to a
ny nets. (LINT-30)
Warning: In design 'slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_conn
id_wdth2_threadid_wdth3', there are 77 ports not connected to any nets. (LINT-30
)
Warning: In design 'ni_tx_port_data_wdth33_3', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_2', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_1', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_tx_port_data_wdth33_0', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth
32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4', there
is 1 port not connected to any nets. (LINT-30)
Warning: In design 'slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth
32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4', there
are 56 feedthroughs. (LINT-30)
Warning: In design 'lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GS
ram_size4_BEcam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8', there is 1 port not co
nnected to any nets. (LINT-30)
Warning: In design 'lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GS
ram_size4_BEcam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8', there is 1 feedthrough
. (LINT-30)
Warning: In design 'slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_f
ifo_depth3', there are 38 ports not connected to any nets. (LINT-30)
Warning: In design 'slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3', ther
e are 2 ports not connected to any nets. (LINT-30)
Warning: In design 'slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3', ther
e are 36 feedthroughs. (LINT-30)
Warning: In design 'ni_rx_port_data_wdth33_3', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_2', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_1', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'ni_rx_port_data_wdth33_0', there are 33 feedthroughs. (LINT-
30)
Warning: In design 'slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4', the
re are 32 feedthroughs. (LINT-30)

Information: Use the 'check_design' command for
         more information about warnings. (LINT-99)


****************************************
Report : power
        -hier
        -analysis_effort low
Design : slave
Version: 2002.05
Date   : Tue Mar  1 11:57:53 2005
****************************************
```



```
Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)


Operating Conditions:
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
slave                     maxarea_192000    CORELIB8DHS
slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_threadid_wdth3_
burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BEcam_addr_
wdth4_BEcam_tag_wdth8
                          maxarea_192000    CORELIB8DHS
slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_connid_wdth2_threadid_wd
th3
                          maxarea_000960    CORELIB8DHS
ni_tx_BEfifo_depth3_TxPorts4_data_wdth33
                          maxarea_048000    CORELIB8DHS
ni_tx_port_data_wdth33_3
                          maxarea_000960    CORELIB8DHS
ni_tx_port_data_wdth33_2
                          maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_4
                          maxarea_014080    CORELIB8DHS
ni_tx_port_data_wdth33_1
                          maxarea_000960    CORELIB8DHS
ni_tx_port_data_wdth33_0
                          maxarea_000960    CORELIB8DHS
slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth32_data_wdth32_GSram
_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4
                          maxarea_007680    CORELIB8DHS
lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GSram_size4_BEcam_size
16_BEcam_addr_wdth4_BEcam_tag_wdth8
                          maxarea_192000    CORELIB8DHS
cam_addr_width4_data_width32_tag_width8_size16
                          maxarea_192000    CORELIB8DHS
ram_data_wdth3_addr_wdth2_size4
                          maxarea_003840    CORELIB8DHS
slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fifo_depth3
                          maxarea_192000    CORELIB8DHS
slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3
                          maxarea_000960    CORELIB8DHS
ni_rx_RxPorts4_data_wdth33_fifo_depth3
                          maxarea_192000    CORELIB8DHS
ni_rx_port_data_wdth33_3
                          maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_3
                          maxarea_014080    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_2
                          maxarea_014080    CORELIB8DHS
ni_rx_port_data_wdth33_2
                          maxarea_000960    CORELIB8DHS
ni_rx_port_data_wdth33_1
                          maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_1
                          maxarea_014080    CORELIB8DHS
scheduler_data_wdth33_ports4
                          maxarea_007680    CORELIB8DHS
```

```
ni_rx_port_data_wdth33_0
                        maxarea_000960    CORELIB8DHS
fifo_fifo_depth3_data_wdth33_0
                        maxarea_014080    CORELIB8DHS
slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4
                        maxarea_003840    CORELIB8DHS


Global Operating Voltage = 1.6
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                     Switch   Int      Leak     Total
Hierarchy                            Power    Power    Power    Power    %
--------------------------------------------------------------------------------
slave                                 519.317   26.700 7.69e+06  546.024 100.0
  slave_resp_1                          1.601   11.355 2.56e+06   12.958   2.4
    slave_resp_control_1             3.05e-02    0.583 1.24e+05    0.614   0.1
    ni_rx_1                              1.568   10.770 2.43e+06   12.341   2.3
      fifo_0                             0.335    2.551 5.57e+05    2.887   0.5
      ni_rx_port_1                    6.29e-03 8.57e-02 1.20e+04 9.20e-02   0.0
      scheduler_1                        0.161    0.185 1.49e+05    0.346   0.1
      fifo_1                             0.351    2.567 5.57e+05    2.918   0.5
      ni_rx_port_0                    6.23e-03 8.55e-02 1.20e+04 9.17e-02   0.0
      ni_rx_port_2                    6.19e-03 8.52e-02 1.20e+04 9.14e-02   0.0
      fifo_3                             0.342    2.563 5.57e+05    2.906   0.5
      fifo_2                             0.343    2.559 5.57e+05    2.902   0.5
      ni_rx_port_3                    6.23e-03 8.55e-02 1.20e+04 9.17e-02   0.0
    slave_resp_ocp_1                  1.99e-03 1.38e-03 2.33e+03 3.37e-03   0.0
  slave_req_1                             4.193   15.345 5.13e+06   19.543   3.6
    lut_1                                 2.746   11.476 3.83e+06   14.225   2.6
      ram_1                           5.44e-02    0.263 6.69e+04    0.317   0.1
      cam_1                               1.163   10.827 3.62e+06   11.993   2.2
    slave_req_control_1                   0.591    0.565 1.77e+05    1.156   0.2
    ni_tx_1                               0.800    3.258 1.10e+06    4.059   0.7
      ni_tx_port_0                    2.64e-03 6.89e-02 1.33e+04 7.16e-02   0.0
      ni_tx_port_1                    2.68e-03 6.93e-02 1.33e+04 7.20e-02   0.0
      fifo_1                              0.265    2.474 5.58e+05    2.740   0.5
      ni_tx_port_3                    2.72e-03 6.94e-02 1.33e+04 7.21e-02   0.0
      ni_tx_port_2                    2.44e-03 6.83e-02 1.33e+04 7.08e-02   0.0
    slave_req_ocp_1                   5.21e-02 4.45e-02 1.63e+04 9.66e-02   0.0
```

```
Information: Updating design information... (UID-85)
Warning: Design 'slave' contains 1 high-fanout nets. A fanout number of 1000 wil
l be used for delay calculations involving these nets. (TIM-134)
Information: Timing loop detected. (OPT-150)
        slave_req_1/ni_tx_1/U48/A slave_req_1/ni_tx_1/U48/Z slave_req_1/ni_tx_1/
U49/A slave_req_1/ni_tx_1/U49/Z
Information: Timing loop detected. (OPT-150)
        slave_req_1/ni_tx_1/U50/A slave_req_1/ni_tx_1/U50/Z slave_req_1/ni_tx_1/
U51/A slave_req_1/ni_tx_1/U51/Z
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U48'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U50'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U52'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U56'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U58'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U60'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U62'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U64'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U66'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U68'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U70'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U72'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U74'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U78'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U80'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U82'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U84'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U86'
```



```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U88'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U90'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U92'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U94'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U96'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U34'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U36'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U38'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U40'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U42'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U44'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U46'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U54'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U76'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U98'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U114'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U116'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U118'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U122'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U124'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
```

```
x_1/U126'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U128'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U130'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U132'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U134'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U136'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U138'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U140'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U144'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U146'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U148'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U150'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U152'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U154'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U156'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U158'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U160'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U162'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U100'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U102'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U104'
        to break a timing loop (OPT-314)
```



```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U106'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U108'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U110'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U112'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U120'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U142'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U164'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U180'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U182'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U184'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U188'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U190'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U192'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U194'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U196'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U198'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U200'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U202'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U204'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U206'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U210'
```

```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U212'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U214'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U216'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U218'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U220'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U222'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U224'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U226'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U228'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U166'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U168'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U170'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U172'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U174'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U176'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U178'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U186'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U208'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U230'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U296'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
```



```
x_1/U274'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U252'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U244'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U242'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U240'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U238'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U236'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U234'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U232'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U294'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U292'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U290'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U288'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U286'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U284'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U282'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U280'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U278'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U276'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U272'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U270'
        to break a timing loop (OPT-314)
```

```
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U268'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U266'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U264'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U262'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U260'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U258'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U256'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U254'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U250'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U248'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'slave_req_1/ni_t
x_1/U246'
        to break a timing loop (OPT-314)

****************************************
Report : area
Design : slave
Version: 2002.05
Date   : Tue Mar  1 11:06:32 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              454
Number of nets:               511
Number of cells:                2
Number of references:           2

Combinational area:       78512.007812
Noncombinational area:    104228.351562
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          182738.937500
Total area:                 undefined
1

1
design_analyzer>
****************************************
```



```
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave
Version: 2002.05
Date   : Tue Mar  1 11:07:06 2005
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: slave_req_1/lut_1/cam_1/cam_table_reg[13][TAG][0]
              (rising edge-triggered flip-flop clocked by OCPClk)
  Endpoint: slave_req_1/ni_tx_1/fifo_1/fifo_reg[0][0]
            (rising edge-triggered flip-flop clocked by OCPClk)
  Path Group: OCPClk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave              maxarea_192000        CORELIB8DHS
  cam_addr_width4_data_width32_tag_width8_size16
                     maxarea_192000        CORELIB8DHS
  slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_threadid_wdth
3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BEcam_add
r_wdth4_BEcam_tag_wdth8
                     maxarea_192000        CORELIB8DHS
  ni_tx_BEfifo_depth3_TxPorts4_data_wdth33
                     maxarea_048000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_4
                     maxarea_014080        CORELIB8DHS

  Point                                                          Incr       Path
  ----------------------------------------------------------------------------
  clock OCPClk (rise edge)                                       0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  slave_req_1/lut_1/cam_1/cam_table_reg[13][TAG][0]/CP (FD7HSP)
                                                                 0.00 #     0.00 r
  slave_req_1/lut_1/cam_1/cam_table_reg[13][TAG][0]/Q (FD7HSP)
                                                                 0.21       0.21 f
  slave_req_1/lut_1/cam_1/U2883/Z (EOHS)                         0.18       0.38 f
  slave_req_1/lut_1/cam_1/U3918/Z (OR8HS)                        0.24       0.62 f
  slave_req_1/lut_1/cam_1/U3812/Z (F_AN2HSP)                     0.17       0.79 f
  slave_req_1/lut_1/cam_1/U3809/Z (AN3HS)                        0.29       1.08 f
  slave_req_1/lut_1/cam_1/U3810/Z (AN3HS)                        0.31       1.39 f
  slave_req_1/lut_1/cam_1/U3029/Z (M_ND2HSP)                     0.20       1.58 r
  slave_req_1/lut_1/cam_1/U3028/Z (M_IVHSP)                      0.24       1.82 f
  slave_req_1/lut_1/cam_1/U3823/Z (F_ND3HSX4)                    0.35       2.18 r
  slave_req_1/lut_1/cam_1/U3891/Z (M_IVHSP)                      0.14       2.32 f
  slave_req_1/lut_1/cam_1/U3896/Z (M_ND3HSP)                     0.36       2.68 r
  slave_req_1/lut_1/cam_1/U3895/Z (M_BFHSP)                      0.41       3.09 r
  slave_req_1/lut_1/cam_1/match_o (cam_addr_width4_data_width32_tag_width8_size1
6)
                                                                 0.00       3.09 r
  slave_req_1/lut_1/match_o (lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data
_wdth3_GSram_size4_BEcam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8)
                                                                 0.00       3.09 r
  slave_req_1/slave_req_control_1/LUTValid_i (slave_req_control_threadid_wdth3_b
urstlength_wdth8_addr_wdth32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_conn
```

```
id_wdth2_TxPorts4)
                                                  0.00       3.09 r
  slave_req_1/slave_req_control_1/U966/Z (AO26NHS)        0.41       3.50 r
  slave_req_1/slave_req_control_1/NIReady_o (slave_req_control_threadid_wdth3_bu
rstlength_wdth8_addr_wdth32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_conni
d_wdth2_TxPorts4)
                                                  0.00       3.50 r
  slave_req_1/ni_tx_1/Ready_i (ni_tx_BEfifo_depth3_TxPorts4_data_wdth33)
                                                  0.00       3.50 r
  slave_req_1/ni_tx_1/U319/Z (F_AN2HSP)           0.16       3.66 r
  slave_req_1/ni_tx_1/fifo_1/fifo_write_i (fifo_fifo_depth3_data_wdth33_4)
                                                  0.00       3.66 r
  slave_req_1/ni_tx_1/fifo_1/U591/Z (M_ND2HSP)    0.06       3.72 f
  slave_req_1/ni_tx_1/fifo_1/U771/Z (M_ND2HSP)    0.28       4.00 r
  slave_req_1/ni_tx_1/fifo_1/U766/Z (M_IVHSP)     0.20       4.20 f
  slave_req_1/ni_tx_1/fifo_1/U767/Z (M_IVHSP)     0.25       4.45 r
  slave_req_1/ni_tx_1/fifo_1/fifo_reg[0][0]/E (FD7HSP)
                                                  0.00       4.45 r
  data arrival time                                          4.45

  clock OCPClk (rise edge)                        5.00       5.00
  clock network delay (ideal)                     0.00       5.00
  slave_req_1/ni_tx_1/fifo_1/fifo_reg[0][0]/CP (FD7HSP)
                                                  0.00       5.00 r
  library setup time                             -0.17       4.83
  data required time                                         4.83
  ------------------------------------------------------------------------
  data required time                                         4.83
  data arrival time                                         -4.45
  ------------------------------------------------------------------------
  slack (MET)                                                0.38


1
design_analyzer>
```

Appendix C **slave_ram.area** Page 1/1

```
Information: Updating design information... (UID-85)

****************************************
Report : area
Design : ram_data_wdth3_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 14:34:33 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               12
Number of nets:                60
Number of cells:               39
Number of references:           6

Combinational area:        675.839966
Noncombinational area:     983.039856
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          1658.880005
Total area:                 undefined
1
design_analyzer>
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ram_data_wdth3_addr_wdth2_size4
Version: 2002.05
Date   : Wed Jan 26 14:34:42 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: memory_reg[0][0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: memory_reg[0][0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ram_data_wdth3_addr_wdth2_size4
                     maxarea_003840        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  memory_reg[0][0]/CP (FD7HSP)             0.00       0.00 r
  memory_reg[0][0]/Q (FD7HSP)              0.17       0.17 f
  U38/Z (F_MUX21HSP)                       0.15       0.32 f
  memory_reg[0][0]/D (FD7HSP)              0.00       0.32 f
  data arrival time                                   0.32

  clock Clk (rise edge)                   50.00      50.00
  clock network delay (ideal)              0.00      50.00
  memory_reg[0][0]/CP (FD7HSP)             0.00      50.00 r
  library setup time                      -0.14      49.86
  data required time                                 49.86
  ----------------------------------------------------------
  data required time                                 49.86
  data arrival time                                  -0.32
  ----------------------------------------------------------
  slack (MET)                                        49.54


1
design_analyzer>
```

Appendix C **slave_req.report** Page 1/7

```
Current design is 'slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wd
th2_threadid_wdth3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam
_size16_BEcam_addr_wdth4_BEcam_tag_wdth8'.
{"slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_threadid_wdth
3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BEcam_add
r_wdth4_BEcam_tag_wdth8"}
design_analyzer> Information: Updating design information... (UID-85)
Information: Timing loop detected. (OPT-150)
        ni_tx_1/U48/A ni_tx_1/U48/Z ni_tx_1/U49/A ni_tx_1/U49/Z
Information: Timing loop detected. (OPT-150)
        ni_tx_1/U50/A ni_tx_1/U50/Z ni_tx_1/U51/A ni_tx_1/U51/Z
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U48'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U50'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U52'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U56'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U58'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U60'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U62'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U64'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U66'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U68'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U70'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U72'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U74'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U78'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U80'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U82'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U84'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U86'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U88'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U90'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U92'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U94'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U96'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U34'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U36'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U38'
```

Appendix C **slave_req.report** Page 2/7

```
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U40'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U42'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U44'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U46'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U54'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U76'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U98'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U114'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U116'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U118'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U122'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U124'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U126'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U128'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U130'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U132'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U134'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U136'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U138'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U140'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U144'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U146'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U148'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U150'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U152'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U154'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U156'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U158'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U160'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U162'
         to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U100'
```

```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U102'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U104'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U106'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U108'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U110'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U112'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U120'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U142'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U164'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U180'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U182'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U184'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U188'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U190'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U192'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U194'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U196'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U198'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U200'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U202'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U204'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U206'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U210'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U212'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U214'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U216'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U218'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U220'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U222'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U224'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U226'
```



```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U228'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U166'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U168'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U170'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U172'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U174'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U176'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U178'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U186'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U208'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U230'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U296'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U274'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U252'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U244'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U242'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U240'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U238'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U236'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U234'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U232'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U294'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U292'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U290'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U288'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U286'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U284'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U282'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U280'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U278'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U276'
```

```
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U272'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U270'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U268'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U266'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U264'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U262'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U260'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U258'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U256'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U254'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U250'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U248'
        to break a timing loop (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'ni_tx_1/U246'
        to break a timing loop (OPT-314)

****************************************
Report : area
Design : slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_thread
id_wdth3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BE
cam_addr_wdth4_BEcam_tag_wdth8
Version: 2002.05
Date   : Tue Mar  1 11:09:19 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              301
Number of nets:               378
Number of cells:                7
Number of references:           6

Combinational area:       54189.968750
Noncombinational area:    66200.273438
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          120389.632812
Total area:                 undefined

1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_thread
```



```
id_wdth3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BE
cam_addr_wdth4_BEcam_tag_wdth8
Version: 2002.05
Date   : Tue Mar  1 11:09:20 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: lut_1/cam_1/cam_table_reg[13][TAG][0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: ni_tx_1/fifo_1/fifo_reg[0][0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_req_data_wdth32_addr_wdth32_local_addr_wdth24_connid_wdth2_threadid_wdth
3_burstlength_wdth8_TxPorts4_GSram_data_wdth3_GSram_size4_BEcam_size16_BEcam_add
r_wdth4_BEcam_tag_wdth8
                     maxarea_192000        CORELIB8DHS
  cam_addr_width4_data_width32_tag_width8_size16
                     maxarea_192000        CORELIB8DHS
  ni_tx_BEfifo_depth3_TxPorts4_data_wdth33
                     maxarea_048000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_4
                     maxarea_014080        CORELIB8DHS

  Point                                                                 Incr       Path
  ------------------------------------------------------------------------------------
  clock Clk (rise edge)                                                 0.00       0.00
  clock network delay (ideal)                                           0.00       0.00
  lut_1/cam_1/cam_table_reg[13][TAG][0]/CP (FD7HSP)                     0.00       0.00 r
  lut_1/cam_1/cam_table_reg[13][TAG][0]/Q (FD7HSP)                      0.21       0.21 f
  lut_1/cam_1/U2883/Z (EOHS)                                            0.18       0.38 f
  lut_1/cam_1/U3918/Z (OR8HS)                                           0.24       0.62 f
  lut_1/cam_1/U3812/Z (F_AN2HSP)                                        0.17       0.79 f
  lut_1/cam_1/U3809/Z (AN3HS)                                           0.29       1.08 f
  lut_1/cam_1/U3810/Z (AN3HS)                                           0.31       1.39 f
  lut_1/cam_1/U3029/Z (M_ND2HSP)                                        0.20       1.58 r
  lut_1/cam_1/U3028/Z (M_IVHSP)                                         0.24       1.82 f
  lut_1/cam_1/U3823/Z (F_ND3HSX4)                                       0.35       2.18 r
  lut_1/cam_1/U3891/Z (M_IVHSP)                                         0.14       2.32 f
  lut_1/cam_1/U3896/Z (M_ND3HSP)                                        0.36       2.68 r
  lut_1/cam_1/U3895/Z (M_BFHSP)                                         0.41       3.09 r
  lut_1/cam_1/match_o (cam_addr_width4_data_width32_tag_width8_size16)
                                                                        0.00       3.09 r
  lut_1/match_o (lut_addr_wdth24_data_wdth32_connid_wdth2_GSram_data_wdth3_GSram
_size4_BEcam_size16_BEcam_addr_wdth4_BEcam_tag_wdth8)
                                                                        0.00       3.09 r
  slave_req_control_1/LUTValid_i (slave_req_control_threadid_wdth3_burstlength_w
dth8_addr_wdth32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxP
orts4)
                                                                        0.00       3.09 r
  slave_req_control_1/U966/Z (AO26NHS)                                  0.41       3.50 r
  slave_req_control_1/NIReady_o (slave_req_control_threadid_wdth3_burstlength_wd
th8_addr_wdth32_data_wdth32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPo
rts4)
                                                                        0.00       3.50 r
  ni_tx_1/Ready_i (ni_tx_BEfifo_depth3_TxPorts4_data_wdth33)
                                                                        0.00       3.50 r
```

```
  ni_tx_1/U319/Z (F_AN2HSP)                                0.16       3.66 r
  ni_tx_1/fifo_1/fifo_write_i (fifo_fifo_depth3_data_wdth33_4)
                                                           0.00       3.66 r
  ni_tx_1/fifo_1/U591/Z (M_ND2HSP)                         0.06       3.72 f
  ni_tx_1/fifo_1/U771/Z (M_ND2HSP)                         0.28       4.00 r
  ni_tx_1/fifo_1/U766/Z (M_IVHSP)                          0.20       4.20 f
  ni_tx_1/fifo_1/U767/Z (M_IVHSP)                          0.25       4.45 r
  ni_tx_1/fifo_1/fifo_reg[0][0]/E (FD7HSP)                 0.00       4.45 r
  data arrival time                                                   4.45

  clock Clk (rise edge)                                   10.00      10.00
  clock network delay (ideal)                              0.00      10.00
  ni_tx_1/fifo_1/fifo_reg[0][0]/CP (FD7HSP)                0.00      10.00 r
  library setup time                                      -0.17       9.83
  data required time                                                  9.83
  ------------------------------------------------------------------------
  data required time                                                  9.83
  data arrival time                                                  -4.45
  ------------------------------------------------------------------------
  slack (MET)                                                        5.38


1
design_analyzer>
```

```
Current design is 'slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth3
2_data_wdth32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4'.
{"slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth32_data_wdth32_GSr
am_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth32_data_wdt
h32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:17:43 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              220
Number of nets:               299
Number of cells:              158
Number of references:          25

Combinational area:       3522.560791
Noncombinational area:    1056.767944
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          4579.328125
Total area:                 undefined

1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth32_data_wdt
h32_GSram_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:17:45 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[3][0]
              (rising edge-triggered flip-flop clocked by Clk)
  Endpoint: CurrentState_reg[0][0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_req_control_threadid_wdth3_burstlength_wdth8_addr_wdth32_data_wdth32_GSr
am_data_wdth3_local_addr_wdth24_connid_wdth2_TxPorts4
                     maxarea_007680        CORELIB8DHS

  Point                                   Incr       Path
  ------------------------------------------------------------
```



```
  clock Clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  CurrentState_reg[3][0]/CP (F_FD2HS)      0.00       0.00 r
  CurrentState_reg[3][0]/QN (F_FD2HS)      0.21       0.21 r
  U1005/Z (AO12HS)                         0.18       0.39 f
  U897/Z (F_ND2AHSP)                       0.09       0.48 f
  U947/Z (M_IVHSP)                         0.06       0.54 r
  U946/Z (M_ND2HSP)                        0.06       0.60 f
  U959/Z (M_IVHSP)                         0.04       0.64 r
  U945/Z (M_ND3HSP)                        0.08       0.72 f
  U951/Z (M_IVHSP)                         0.05       0.76 r
  U1002/Z (M_ND3HSP)                       0.08       0.84 f
  U872/Z (AO7NHSP)                         0.15       0.99 f
  U906/Z (F_AO39HS)                        0.22       1.21 r
  U922/Z (F_MUX21HSP)                      0.17       1.38 r
  CurrentState_reg[0][0]/D (F_FD2HS)       0.00       1.38 r
  data arrival time                                   1.38

  clock Clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  CurrentState_reg[0][0]/CP (F_FD2HS)      0.00      10.00 r
  library setup time                      -0.20       9.80
  data required time                                  9.80
  ------------------------------------------------------------
  data required time                                  9.80
  data arrival time                                  -1.38
  ------------------------------------------------------------
  slack (MET)                                         8.42


1
design_analyzer>
```

```
Current design is 'slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_conni
d_wdth2_threadid_wdth3'.
{"slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_connid_wdth2_threadid_
wdth3"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_connid_wdth2_th
readid_wdth3
Version: 2002.05
Date   : Tue Mar  1 11:04:52 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              102
Number of nets:                35
Number of cells:               17
Number of references:           9

Combinational area:        303.104004
Noncombinational area:     135.167999
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           438.272003
Total area:                 undefined

1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_connid_wdth2_th
readid_wdth3
Version: 2002.05
Date   : Tue Mar  1 11:04:53 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg
              (rising edge-triggered flip-flop)
  Endpoint: MThreadID_o[2]
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_req_ocp_data_wdth32_addr_wdth32_burstlength_wdth8_connid_wdth2_threadid_
wdth3
                     maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ------------------------------------------------------------
```



```
  CurrentState_reg/CP (F_FD2HS)            0.00       0.00 r
  CurrentState_reg/Q (F_FD2HS)             0.27       0.27 f
  U53/Z (F_MUX21HSP)                       0.16       0.43 f
  MThreadID_o[2] (out)                     0.00       0.43 f
  data arrival time                                   0.43
  ------------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fi
fo_depth3'.
{"slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fifo_depth3"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fifo_depth3
Version: 2002.05
Date   : Tue Mar  1 11:05:54 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              277
Number of nets:               283
Number of cells:                3
Number of references:           3

Combinational area:       24321.933594
Noncombinational area:    38027.335938
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          62349.312500
Total area:                 undefined
1

design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fifo_depth3
Version: 2002.05
Date   : Tue Mar  1 11:06:05 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: ni_rx_1/fifo_3/count_reg[0]
              (rising edge-triggered flip-flop)
  Endpoint: SData_o[27]
            (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_resp_data_wdth32_addr_wdth32_threadid_wdth3_RxPorts4_fifo_depth3
                     maxarea_192000        CORELIB8DHS
  fifo_fifo_depth3_data_wdth33_2
                     maxarea_014080        CORELIB8DHS
  ni_rx_RxPorts4_data_wdth33_fifo_depth3
                     maxarea_192000        CORELIB8DHS
  scheduler_data_wdth33_ports4
                     maxarea_007680        CORELIB8DHS
```



```
  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  ni_rx_1/fifo_3/count_reg[0]/CP (F_FD2QHS)               0.00       0.00 r
  ni_rx_1/fifo_3/count_reg[0]/Q (F_FD2QHS)                0.24       0.24 f
  ni_rx_1/fifo_3/U505/Z (M_ND2HSP)                        0.09       0.33 r
  ni_rx_1/fifo_3/U504/Z (M_IVHSP)                         0.06       0.39 f
  ni_rx_1/fifo_3/fifo_full_o (fifo_fifo_depth3_data_wdth33_2)
                                                          0.00       0.39 f
  ni_rx_1/U21/Z (M_IVHSP)                                 0.06       0.45 r
  ni_rx_1/U15/Z (F_ND2AHSP)                               0.13       0.58 f
  ni_rx_1/scheduler_1/ready_i[3] (scheduler_data_wdth33_ports4)
                                                          0.00       0.58 f
  ni_rx_1/scheduler_1/U727/Z (M_IVHSP)                    0.12       0.69 r
  ni_rx_1/scheduler_1/U692/Z (M_ND2HSP)                   0.09       0.79 f
  ni_rx_1/scheduler_1/U718/Z (M_IVHSP)                    0.10       0.89 r
  ni_rx_1/scheduler_1/U818/Z (F_AO6HS)                    0.09       0.98 f
  ni_rx_1/scheduler_1/U834/Z (AO22NHSP)                   0.18       1.15 f
  ni_rx_1/scheduler_1/U823/Z (AO3HS)                      0.31       1.47 r
  ni_rx_1/scheduler_1/U821/Z (M_BFHSP)                    0.32       1.78 r
  ni_rx_1/scheduler_1/U772/Z (F_AO10NHSP)                 0.22       2.00 r
  ni_rx_1/scheduler_1/data_o[27] (scheduler_data_wdth33_ports4)
                                                          0.00       2.00 r
  ni_rx_1/NIData_o[27] (ni_rx_RxPorts4_data_wdth33_fifo_depth3)
                                                          0.00       2.00 r
  slave_resp_ocp_1/SData_i[27] (slave_resp_ocp_data_wdth32_addr_wdth32_threadid_
wdth3)
                                                          0.00       2.00 r
  slave_resp_ocp_1/SData_o[27] (slave_resp_ocp_data_wdth32_addr_wdth32_threadid_
wdth3)
                                                          0.00       2.00 r
  SData_o[27] (out)                                       0.00       2.00 r
  data arrival time                                                  2.00
  ------------------------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4'.
{"slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:05:23 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:              104
Number of nets:               108
Number of cells:               67
Number of references:          17

Combinational area:        573.439880
Noncombinational area:    2592.768066
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          3166.208008
Total area:                 undefined
1
design_analyzer> Warning: In design 'slave_resp_control_data_wdth33_threadid_wdt
h3_RxPorts4', there are 32 feedthroughs. (LINT-30)



1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4
Version: 2002.05
Date   : Tue Mar  1 11:05:24 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: CurrentState_reg[1]
              (rising edge-triggered flip-flop)
  Endpoint: NIDone_o (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_resp_control_data_wdth33_threadid_wdth3_RxPorts4
                     maxarea_003840        CORELIB8DHS

  Point                                    Incr       Path
  ----------------------------------------------------------
  CurrentState_reg[1]/CP (F_FD2QHS)        0.00       0.00 r
```



```
  CurrentState_reg[1]/Q (F_FD2QHS)         0.15       0.15 r
  U105/Z (M_IVHSP)                         0.05       0.21 f
  U91/Z (M_ND2HSP)                         0.07       0.27 r
  U89/Z (F_ND2AHSP)                        0.09       0.36 r
  U88/Z (M_IVHSP)                          0.05       0.41 f
  U80/Z (AO8NHSP)                          0.11       0.52 f
  NIDone_o (out)                           0.00       0.52 f
  data arrival time                                   0.52
  ----------------------------------------------------------
  (Path is unconstrained)


1
design_analyzer>
```

```
Current design is 'slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3'.
{"slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3"}
design_analyzer> Information: Updating design information... (UID-85)

****************************************
Report : area
Design : slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3
Version: 2002.05
Date   : Tue Mar  1 11:22:40 2005
****************************************

Library(s) Used:

    CORELIB8DHS (File: /ult/DK_HCMOS8_3.3/CORELIB8DHS_HCMOS8D_3.1.a/SYNOPSYS_DP/
bc_1.60V_m40C/CORELIB8DHS.db)

Number of ports:               81
Number of nets:                43
Number of cells:                3
Number of references:           2

Combinational area:         53.248001
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:            53.248001
Total area:                 undefined
1

design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3
Version: 2002.05
Date   : Tue Mar  1 11:22:40 2005
****************************************

Operating Conditions:
Wire Load Model Mode: enclosed

  Startpoint: SResp_i[1] (input port)
  Endpoint: SResp_o[1] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  slave_resp_ocp_data_wdth32_addr_wdth32_threadid_wdth3
                     maxarea_000960        CORELIB8DHS

  Point                                    Incr       Path
  ------------------------------------------------------------
  input external delay                     0.00       0.00 f
  SResp_i[1] (in)                          0.00       0.00 f
  U38/Z (F_AN2HSP)                         0.07       0.07 f
  SResp_o[1] (out)                         0.00       0.07 f
  data arrival time                                   0.07
  ------------------------------------------------------------
  (Path is unconstrained)
```



```
1
design_analyzer>
```

APPENDIX D

Wave-plots

The wave-plot of the ModelSim simulations can be found at

`http://www.student.dtu.dk/~s961394/files/appendix.zip`

The wave-plot are save in `.wlf` format for viewing in ModelSim or `.vcd` for viewing in out own favorite wave diagram viewer.