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# Modeling and Power Evaluation of On-Chip Router Components in Spintronics

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# Agenda



- **Spintronics**
  - Motivation
  - Overview
- **Magnetic Tunnel Junction (MTJ)**
  - Theory
  - Research status
  - Reading and Writing MTJs
  - Switching energy
  - Simulation model
- **Results for on-chip routers components**
  - Buffers
  - Crossbars

# Spintronics & MTJ

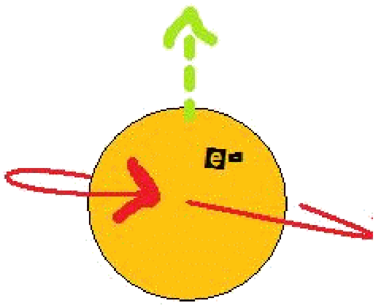
Magnetic Tunnel Junction

# Spintronics ?



- **Motivations:**
  - o CMOS drawbacks
    - Static current
    - High dynamic current
  - o Routers become essentials
    - Power consuming

**A new technology is required**

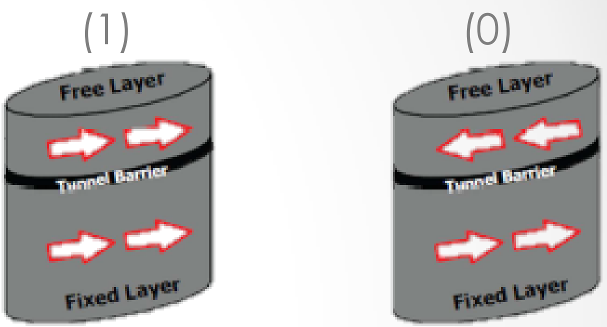


- **Spintronics:**
  - o Tunneling effect
  - o Spin and magnetic moment of the electron vs charge
  - o Potential applications : Memory, Logic elements, …

# Magnetic Tunnel Junction (MTJ)



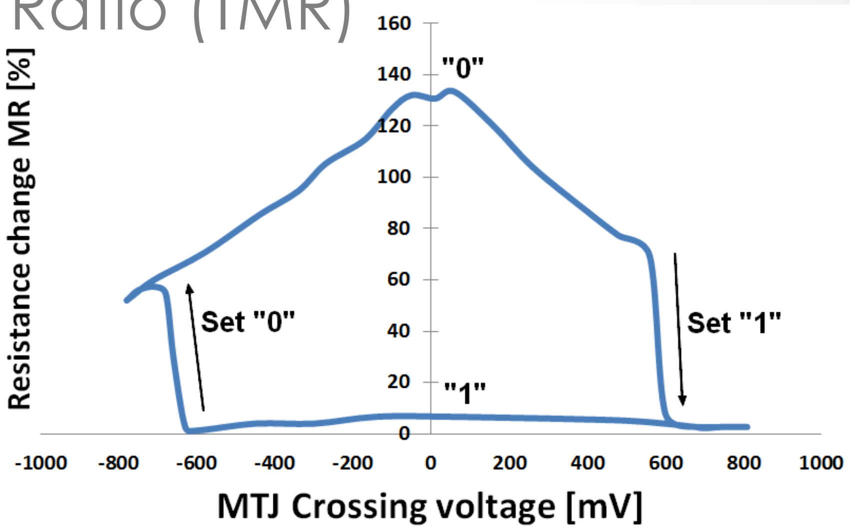
- **Sandwich structure:**
  - o Ferromagnetic/Insulator/Ferromagnetic
- **2 States:**
  - o Parallel & Anti-parallel (resp. 1 & 0)
  - o 2 Resistances (High & Low)




- **Main parameter:**
  - o Tunnel Magnetoresistance Ratio (TMR)

$$TMR = \frac{R_{AP} - RP}{R_P}$$

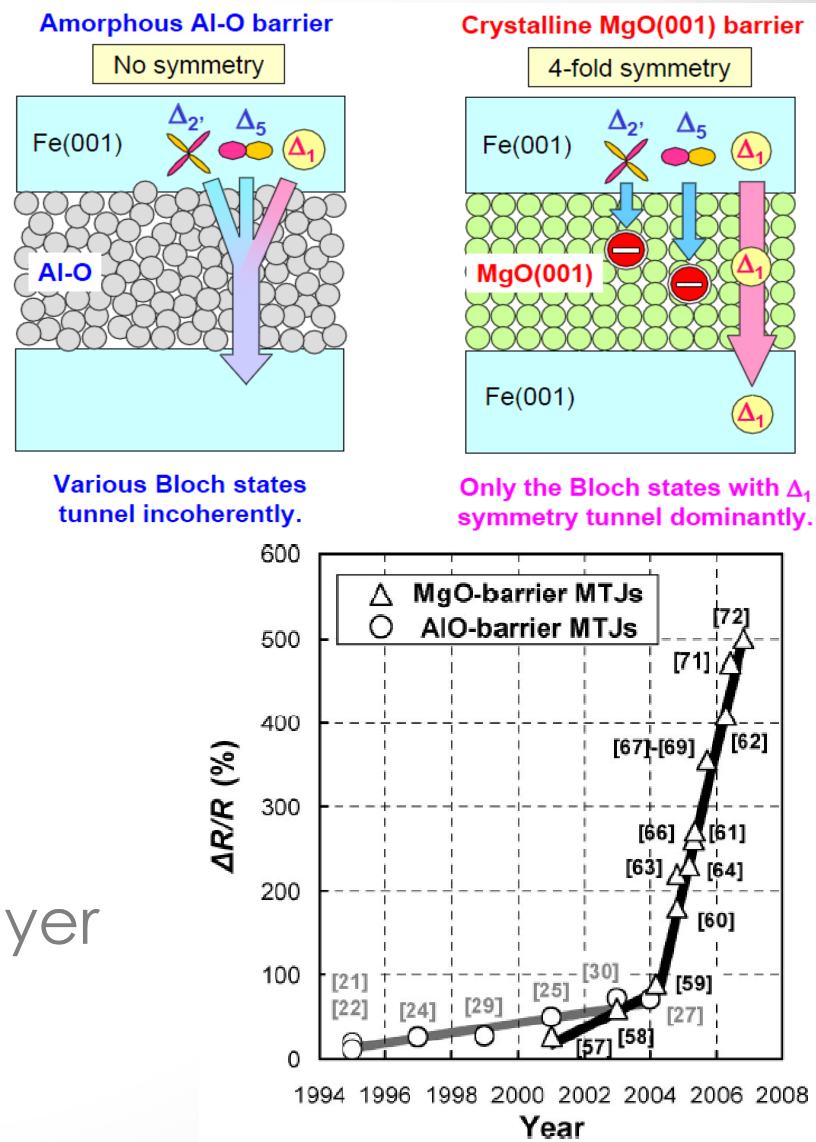
- Voltage dependency on the resistance values



# MTJ: State of the Art



- **TMR up to 600%**
- **Material:**
  - Amorphous *AlO* barrier
  - *MgO* crystal barrier
- **Main parameters:**
  - Thickness of the free layer
  - Thickness of the insulated layer



# Pros & Cons

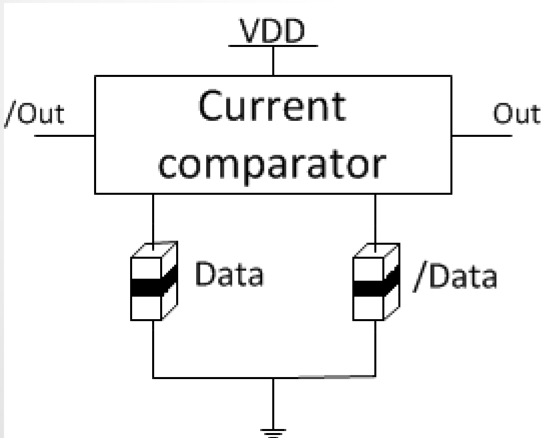


| Advantages | Drawbacks |
|---|---|
| *Good integration*<br>*Good scalability*<br>*Power failure safe*<br>*No static current*<br>*Power stand-by* | *Perturbations at high concentration rate (MRAM)*<br>*High switching (write) energy* |

# MTJ: Read circuitry

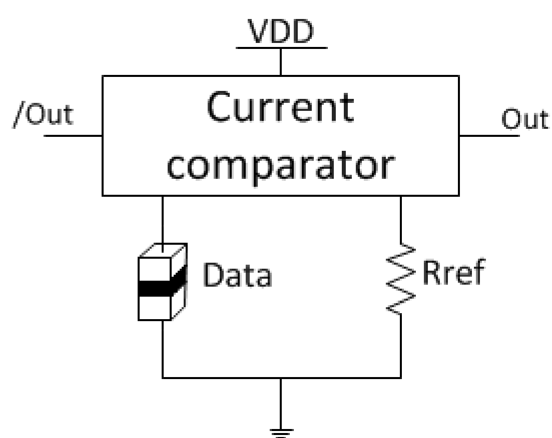


- **2 implementations:**
  - 2 MTJs
  - 1 MTJ & 1 reference resistor

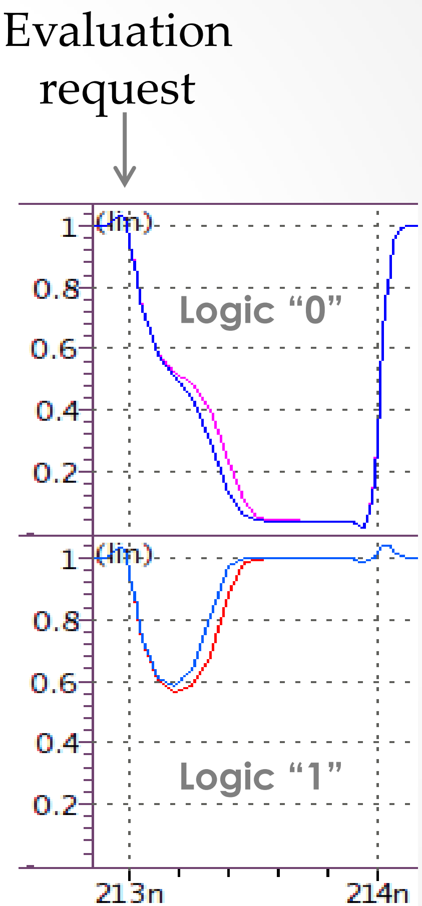



2 MTJ Design

$$R_{REF} = \frac{R_{AP} + R_P}{2}$$




1MTJ + 1 Reference Resistor Design

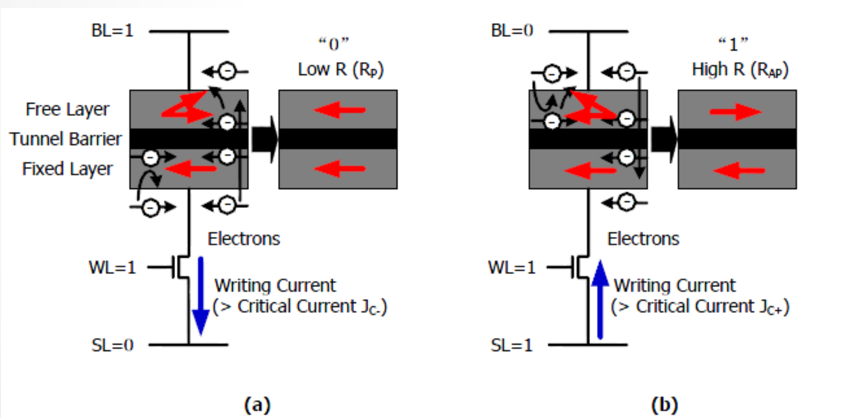


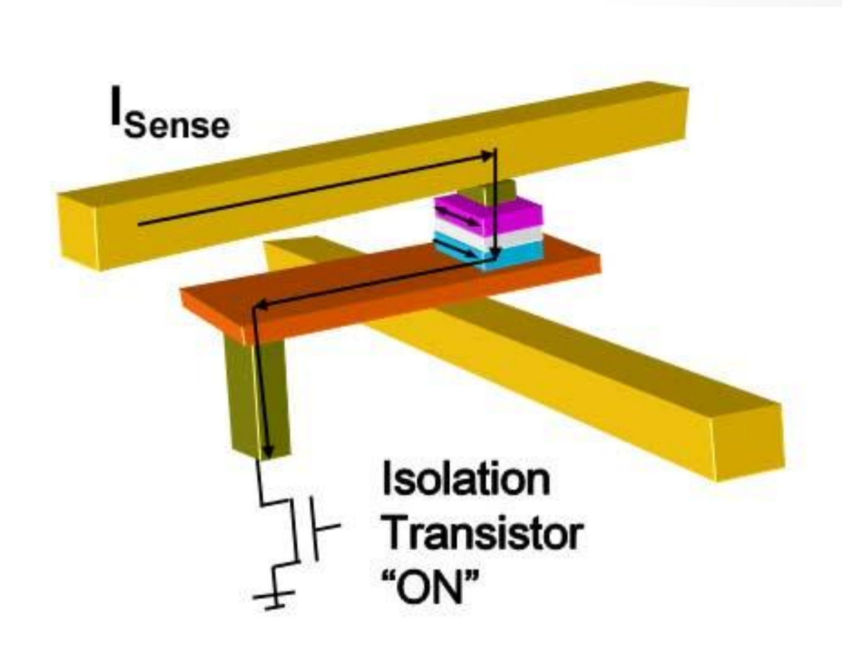

**2 MTJ**
**Mixed 1MTJ-1Resistor**

# MTJ: Write (Switching) circuitry



- **Different switching methods:**
  - Spin-Torque Transfer (STT)
  - Perpendicular magnetization

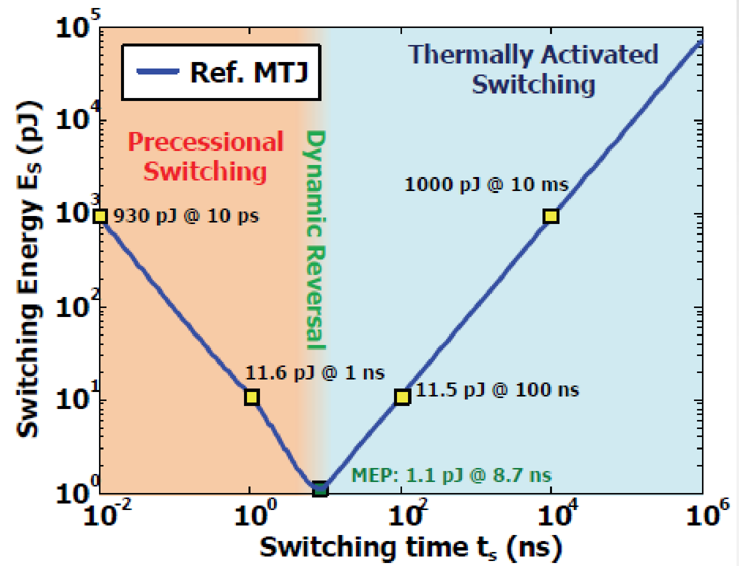


# Switching energy



- **3 types of switching:**
  - Precessional Switching
  - Dynamic Reversal
  - Thermally Activated Switching




- **2011 results :**

| Direction | Energy | Time |
|---|---|---|
| Anti-parallel state to parallel state | 0.286pJ | 1.54ns |
| Parallel state to Antiparallel state | 0.706pJ | 0.68ns |

**Switching power at 500MHz:**
- Actual: **125μW**
- Actual CMOS: **8μW**
- Expected: **0.1μW**

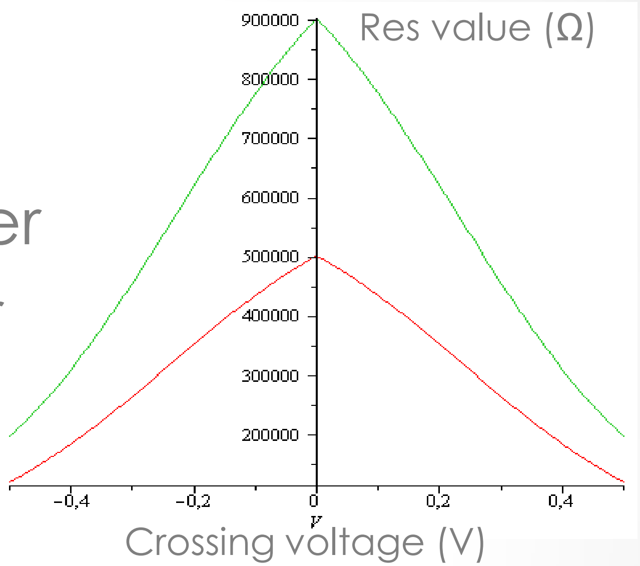
# Simulation models and results

When applied to On-Chip Routers components

# MTJ Model



- **Simulation choices:**
  - Reading power only
  - Total power = reading power + writing power

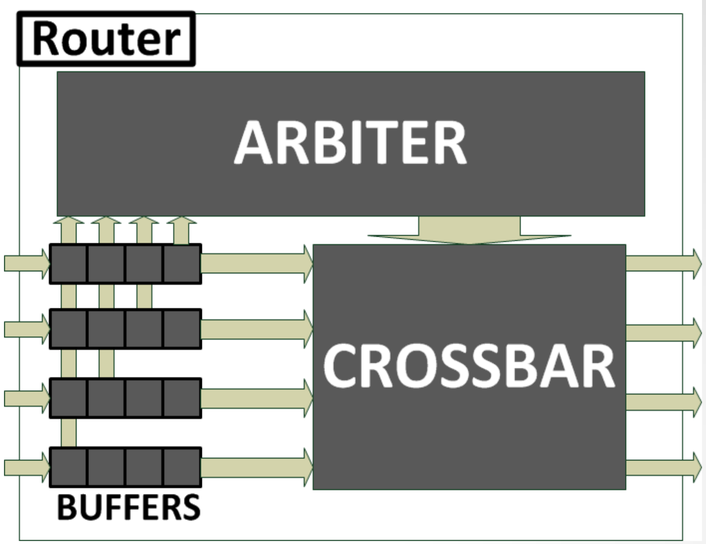



- **Reading model:**
  - Simple model : Variable resistance
  - Corrected model : $\frac{1}{R} = \frac{1}{c} + \frac{1}{a * \exp(-\mathrm{b.V})}$
- **Writing power computation:**
  - Extrapolated from 1fJ/switching

# On-chip router components

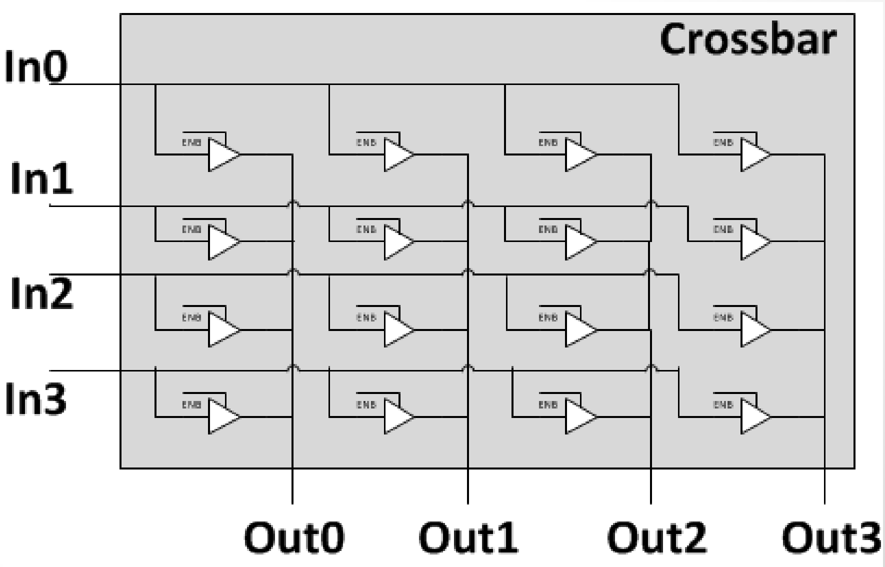


- **3 main parts:**
  - Arbiter
  - Buffers
  - Crossbar




- **Speed:**
  - 500MHz – 2GHz

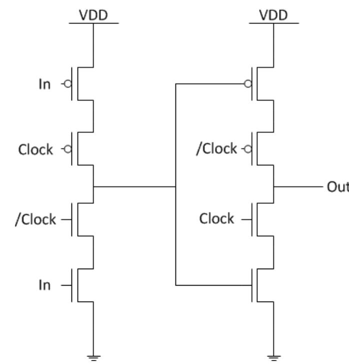
- **Data width:**
  - Up to 128 bits



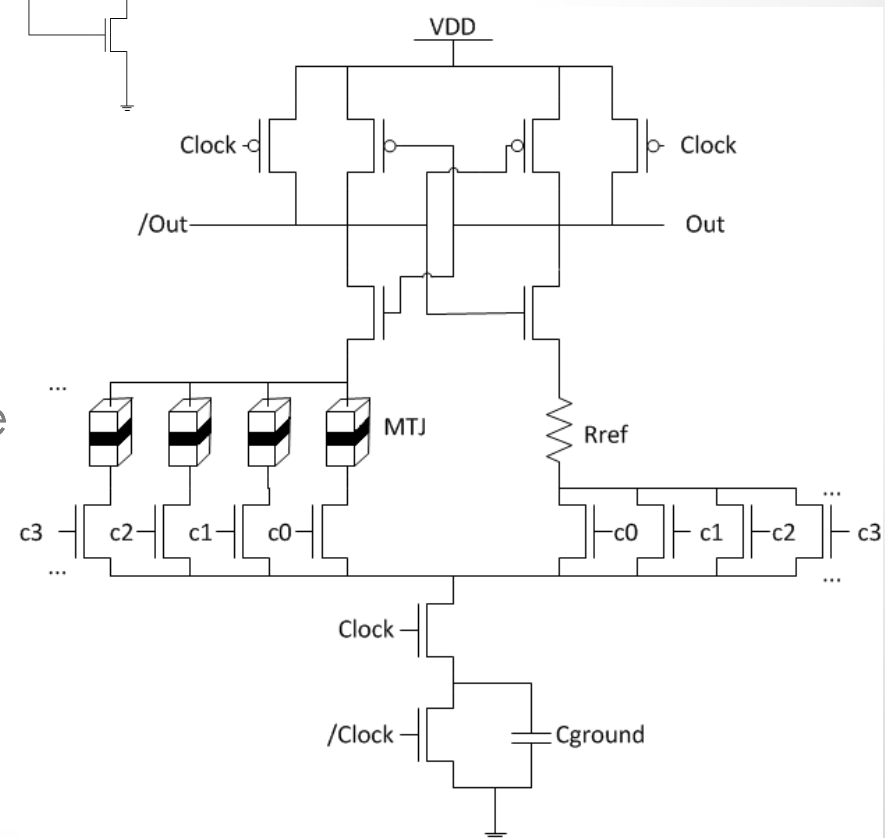
# Buffer implementation



- **CMOS Flip-flops**
  - Classic flip-flop model

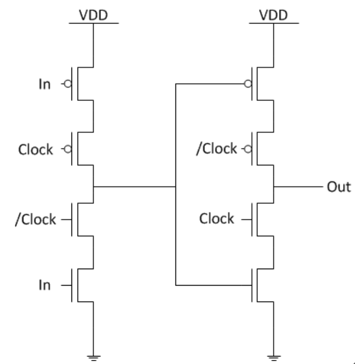



- **MTJ reader circuitry**
  - Random Access Type
  - Only 1evaluation circuit/module
  - 1 MTJ to store a each state



# Buffer implementation



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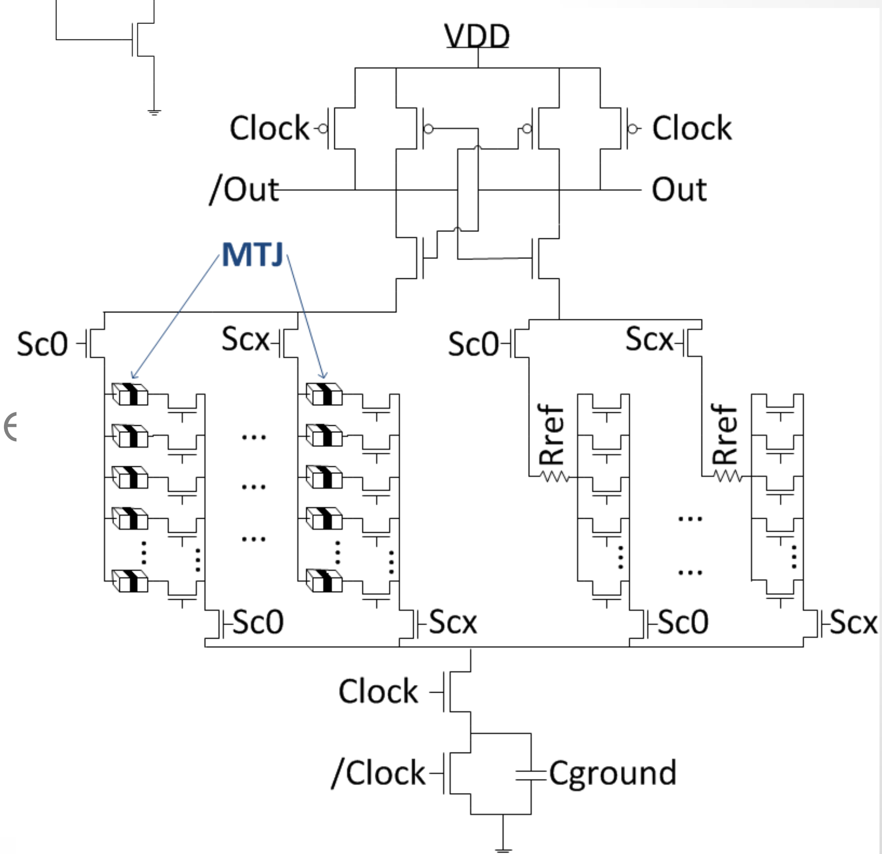



- **MTJ reader circuitry**
  - Random Access Type
  - Only 1evaluation circuit/module
  - 1 MTJ to store a each state
  - Branch transistor for **depth>50**

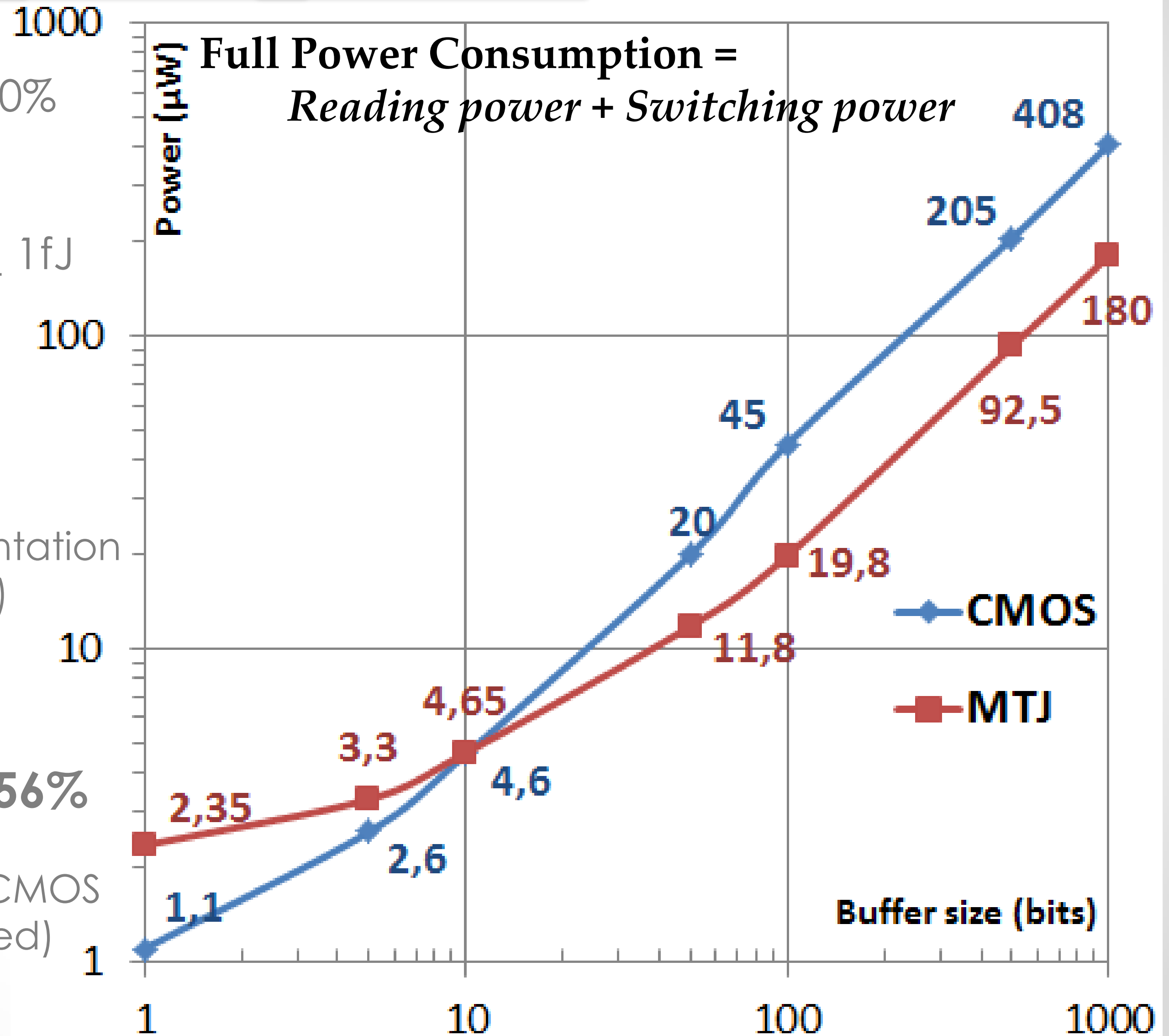
# Buffer implementation: Results



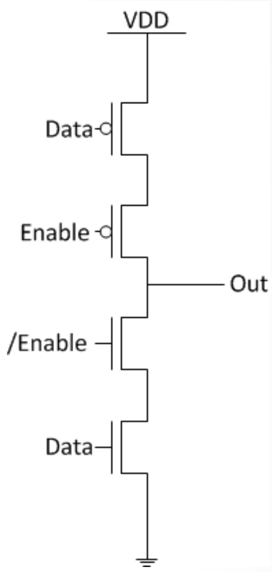
Switching probability: 50%
Frequency: 250MHz
Duty Cycle: 25%
Switching energy (est.): 1fJ

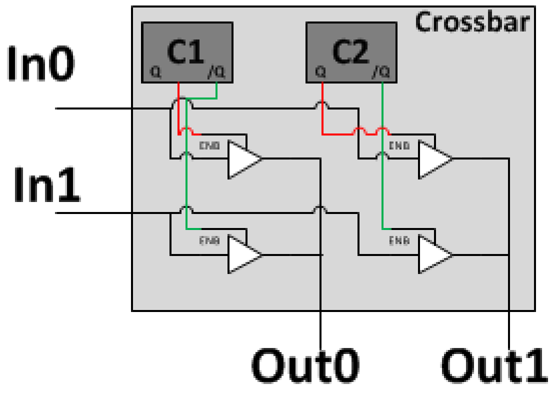
**Key depth = 10**
(over which the MTJ implementation is less power consuming)

**Power saving = up to -56%**
(Trend for deep buffer implementation, 56% of the CMOS power consumption is saved)



- **CMOS implementation:**
  - Tri-state buffers
  - CMOS Flip-flop for the control bits
- **MTJ implementation 1:**
  - Tri-state buffers
  - MTJ reader for the control bits

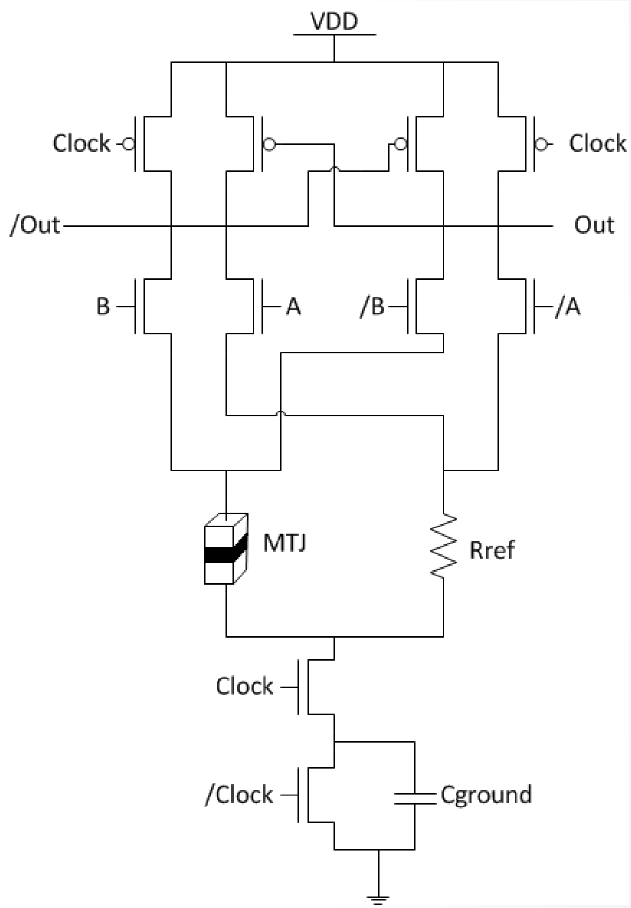


# Crossbar implementation



- **MTJ implementation 2:**
  - No CMOS tri-state buffer
  - Logic-in-Memory device




- CMOS Flip-flop: **0.6uW**
- MTJ reader: **2.27uW**
- Logic-In-Memory Mux: **2.5uW**

# Conclusion



- **Spintronics**
  - About electron's spin, not charge
- **MTJ switching methods**
  - Energy magnitude vs. Switching speed
- **MTJ reader concepts**
  - Resistance value comparison
- **Buffer MTJ implementation**
  - Very scalable
  - Power efficient
- **Crossbar MTJ Implementation**
  - Hardly scalable
  - Not yet power efficient
- **Extensions**
  - Router Arbiter with MTJ
  - Scalable Logic-in-Memory Multiplexer structure (Crossbar)

# Questions



**Thank you for your attention!**

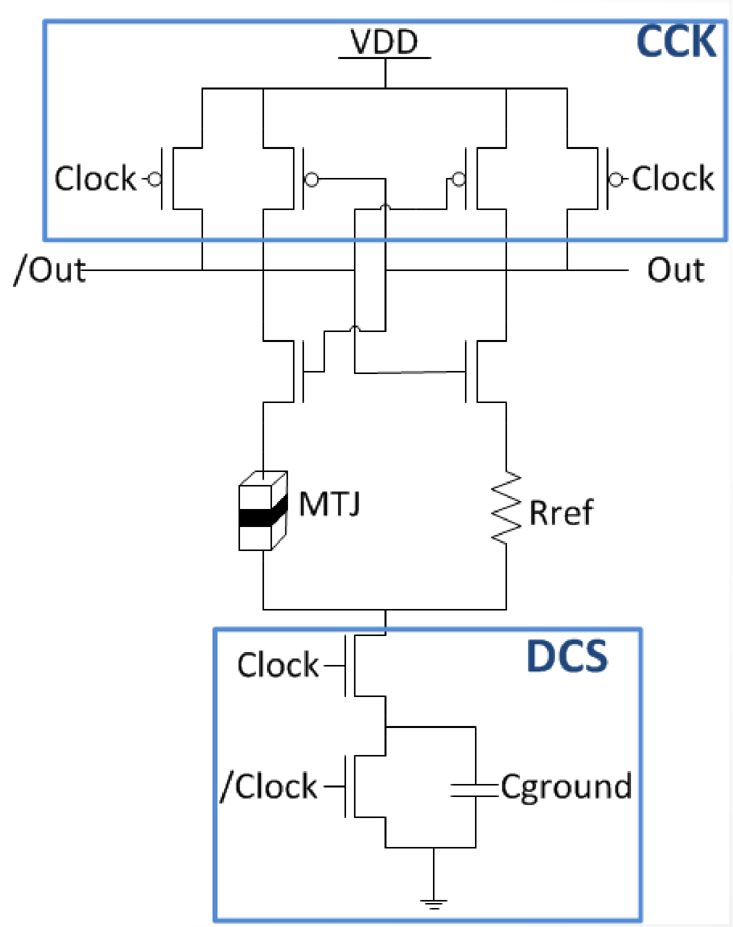
**Any questions ?**

# Annexes

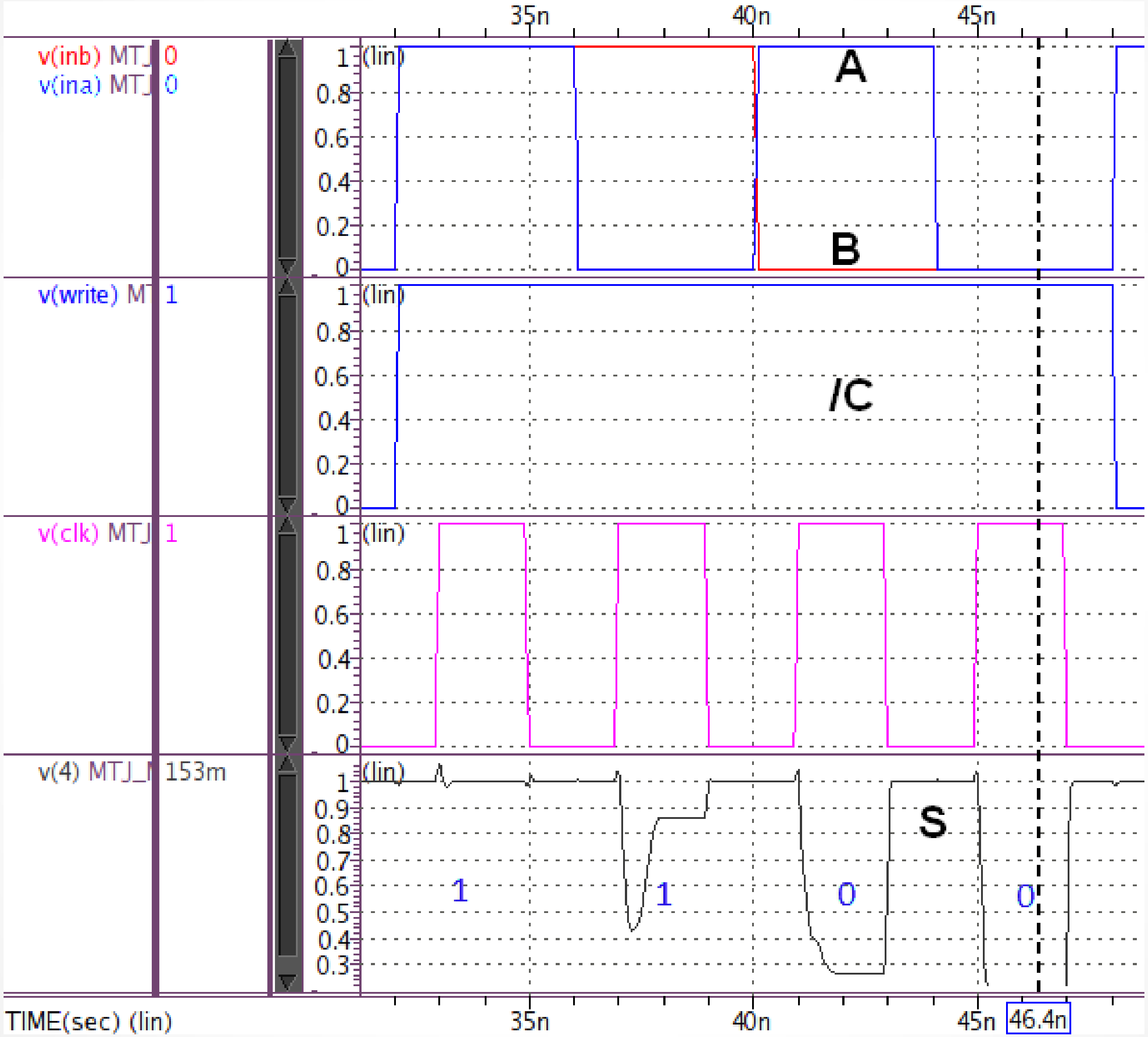
Magnetic Tunnel Junction

# Annex: MTJ Reader DyCML

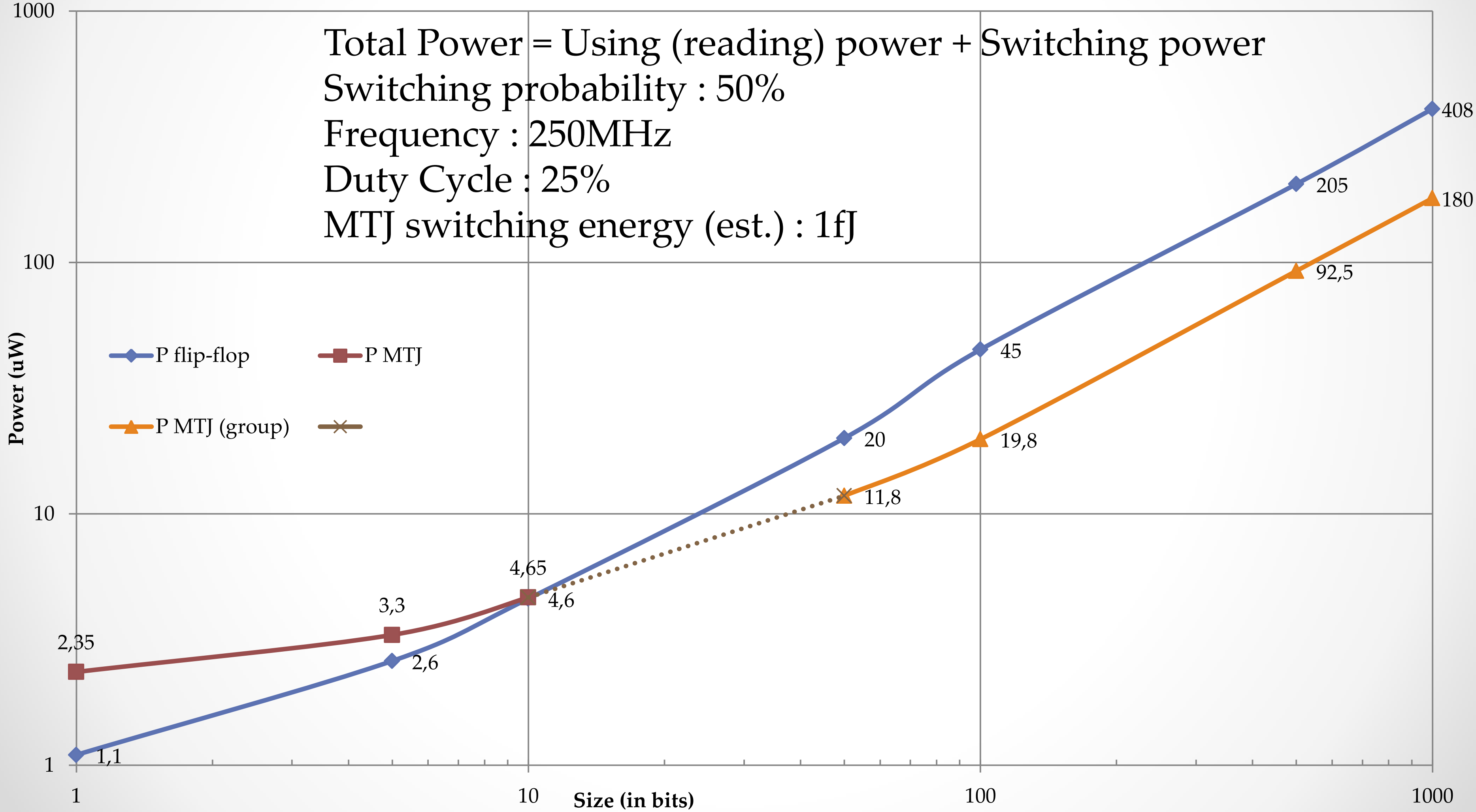
- **DyCML:**
  - Dynamic Current Model Logic
- **CCK:**
  - Cross-Coupled Keeper
- **DCS:**
  - Dynamic current source



# Annex: Crossbar Logic-in-Memory



# Annex: Buffer impl. results



# Annex: Extensions

- MTJ Arbiters
- Switching energy enhancements
- Resizing buffers more power efficiently
- Scalable Logic-in-Memory Multiplexer