

Oticon

NOCs in
highly optimized
commercial chipsets
for hearing aids.

Mogens Cash Balsby

Sr. Director Silicon Engines



oticon
PEOPLE FIRST

the introduction
the challenges
the design choices
the implementation

Agenda

the introduction

your presenter

your Hearing Aid manufacturer

the hearing aid

Introduction

Your presenter

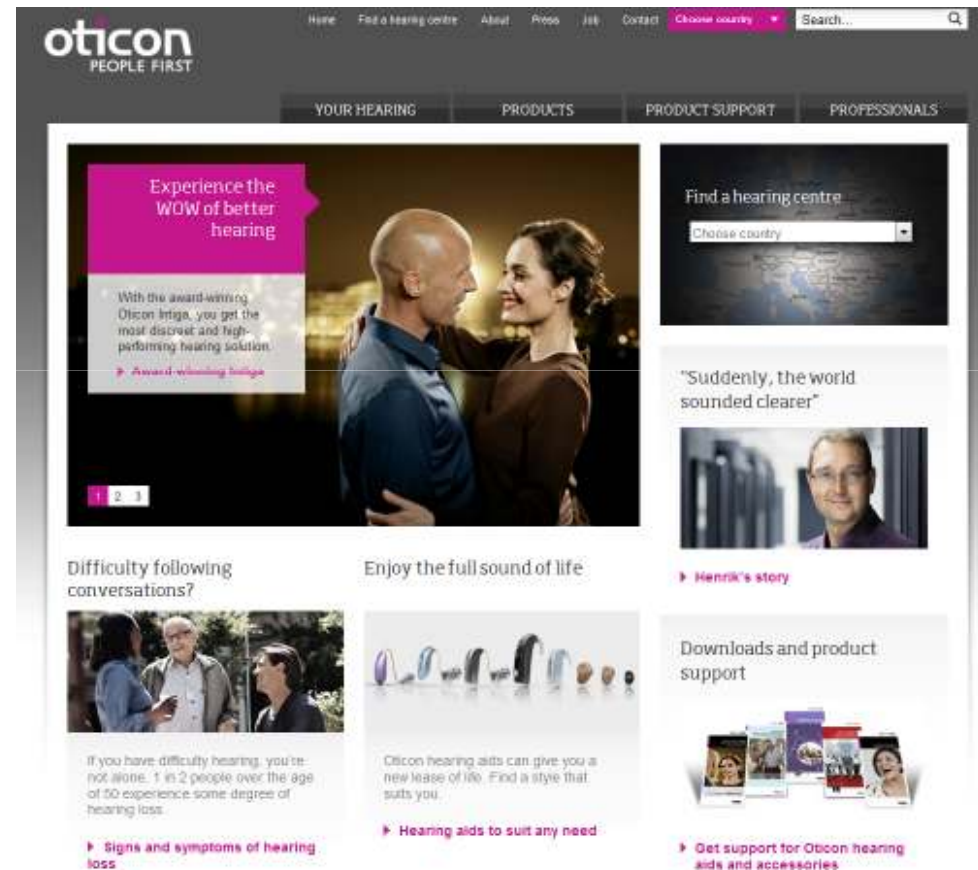
- Sr. Director Silicon Engines in Oticon
- B.Sc.E.E
- PCB → ASIC designer
- Networking
- MIPS processors
- Hearing Instruments



Oticon

Your hearing aid manufacturer

- Oticon part of William Demant
- World leading manufacturer
- 1,5 B\$
 - 5.000 people
 - 1.400 in Denmark
- 400 in R&D
 - In Denmark and Switzerland



The Oticon history

- Founded in 1904 by Hans Demant
- Hans wanted to help his deaf wife
- H.D. died in 1910
- His son, William, took over the business
- The 20's and 30's: Sales in Europe



H. Demant,
Symaskine- & Cyklefabrik,
57, Kongensgade 57,
Odense.

The Oticon story

➤ The 40's

Own production

➤ The 60's

Own distribution network in Europe

➤ The 70's

The world's leading hearing aid producer with a market share of 15%



Oticon Product Breakthroughs

- **MultiFocus**, 1991, world's first fully automatic
- **DigiFocus**, 1996, world's **first fully digital** at ear-level
- **Adapto**, 2001, world's first with voice recognition
- **Oticon Syncro**, 2004, world's first with artificial intelligence
- **Oticon Delta**, 2006, revolutionary design
- **Oticon Epoq**, 2007, world's first truly binaural with spatial sound
- **Oticon Dual**, 2008, outstanding beauty & brains
- **Oticon ConnectLine**, 2009, world's first low-latency high quality audio streaming
- **Oticon Agil**, 2010, world's first cognitive friendly hearing system



1991
MultiFocus



1996
DigiFocus



2001
Adapto



2004
Oticon Syncro



2006
Oticon Delta



2007
Oticon Epoq



2008
Oticon Dual



2009
Oticon ConnectLine



2010
Oticon Agil

Oticon Product Breakthrough 2011

World smallest fully wireless HI





The hearing aid industry

Characterized by...

- Small market size ~10M units/y
- 6 big players
- No standardization
- High degree of design optimizations

the challenges

Discreteness

Power

Sound

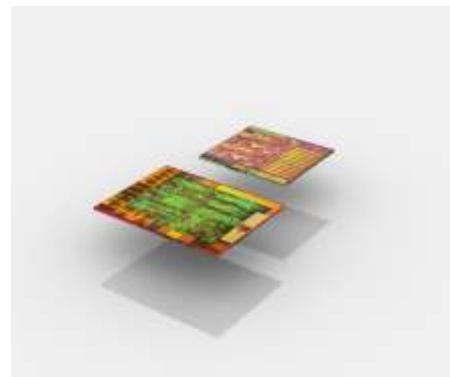
One chipset

multiple brands, products, styles

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bernafon
Your hearing • Our passion

SONIC
Everyday Sounds Better



Few Chipsets

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The mechanical challenge

discreetness




The mechanical challenge


discreetness

NEW INVISIBLE INTIGA¹

Designed to keep hearing loss
Out of sight... and out of mind

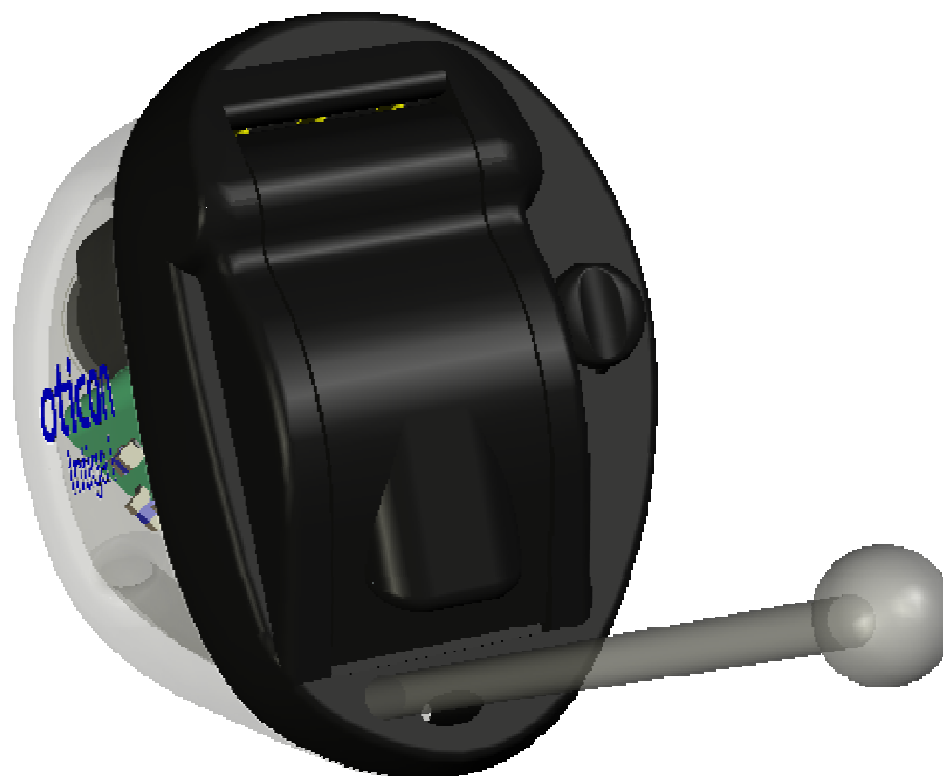


Completely
unnoticeable



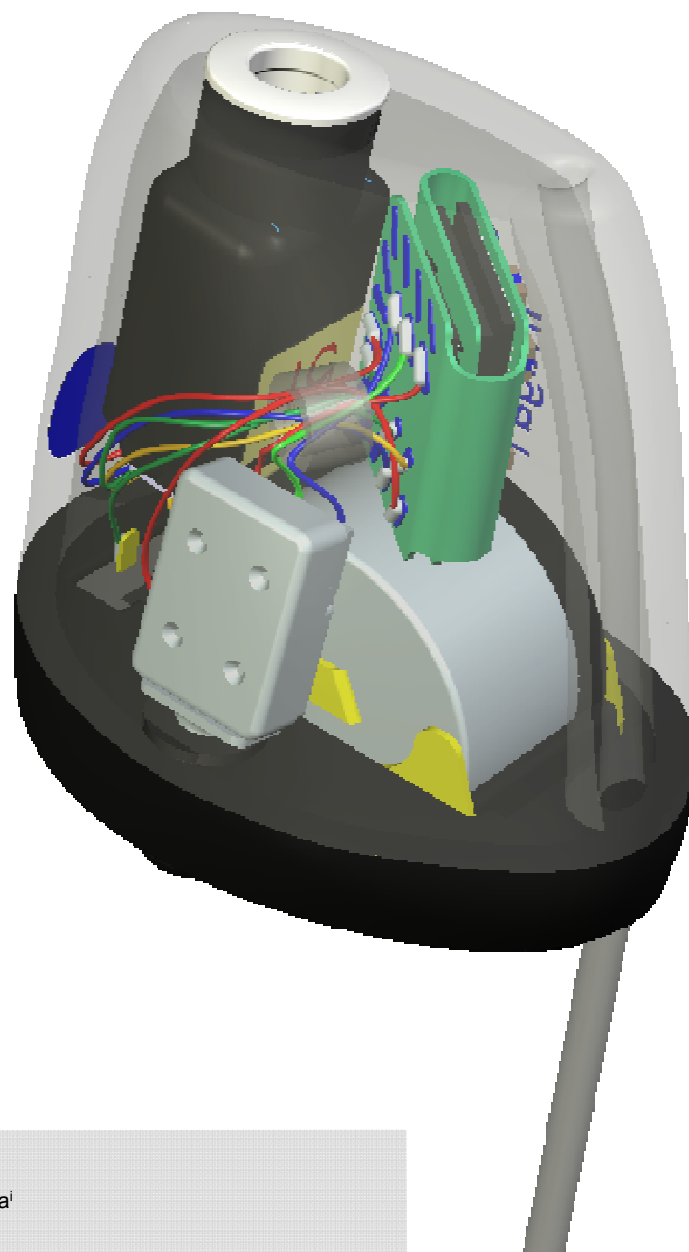
Oticon | Intiga¹

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New Invisible Intigaⁱ

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PEOPLE FIRST



New Invisible Intigaⁱ

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Miniature speaker

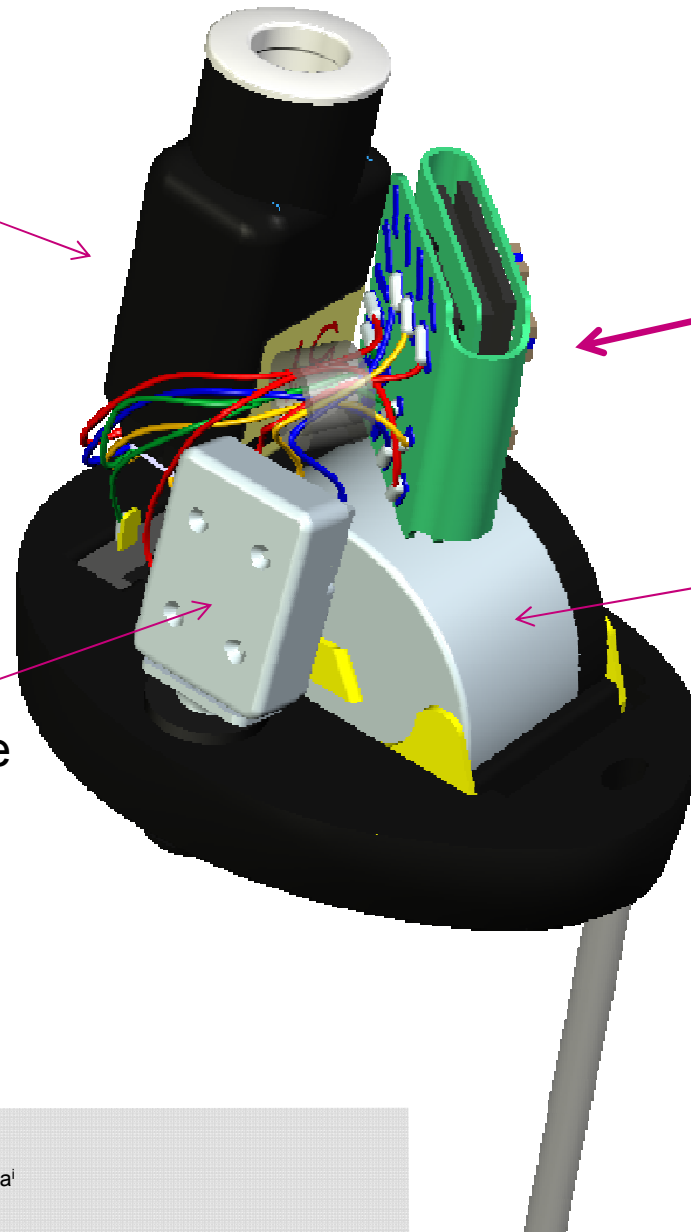
Compact **low power**
RISE 2 amplifier

Standard 10A
battery

Miniature microphone

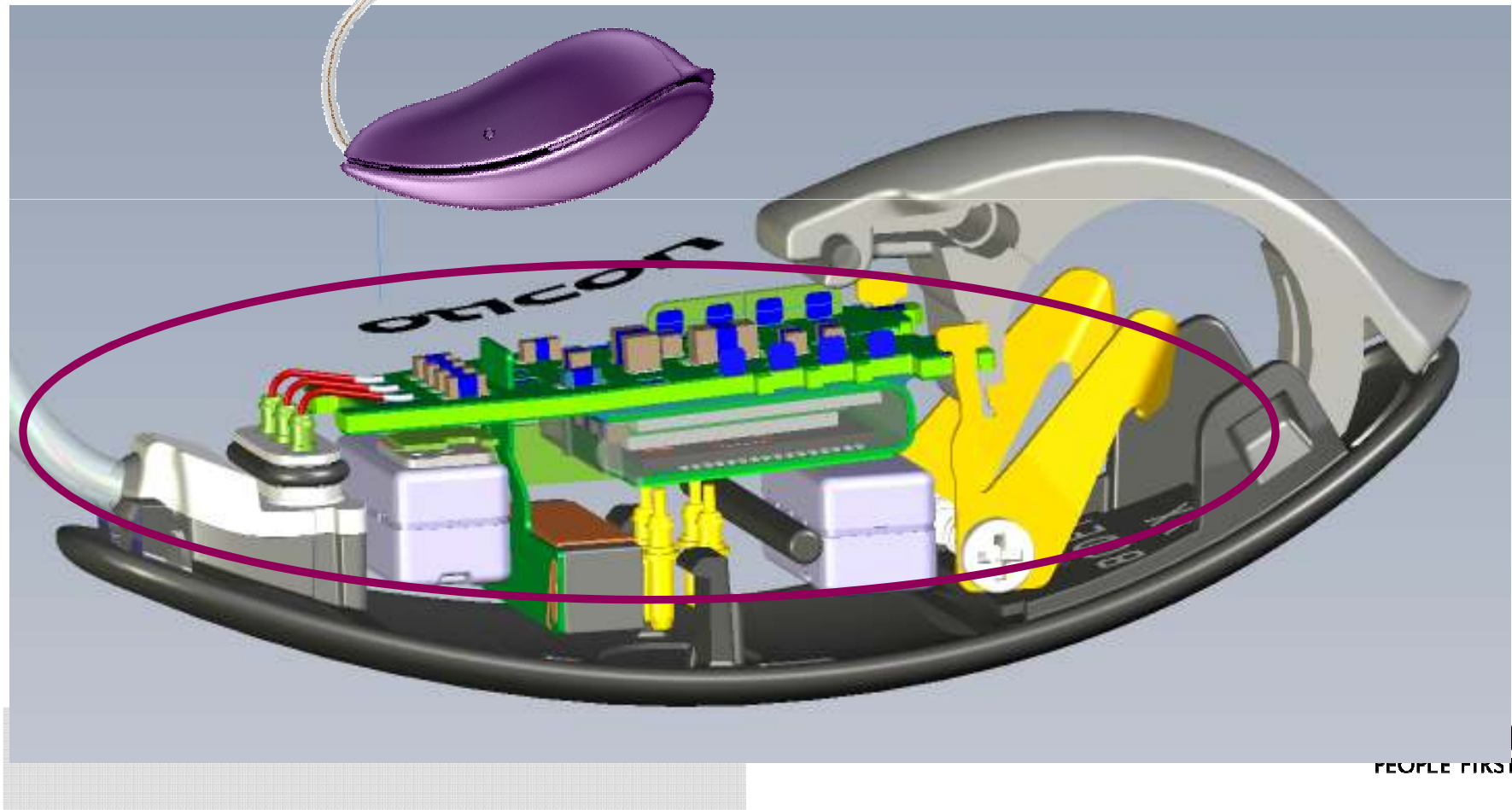
New Invisible Intigaⁱ

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The mechanical challenge

discreetness



The power challenge

we save on everything

Battery type	Capacity	Consumption in 1 week
13	~260 mAh	2,0 mA
312	~130 mAh	1,0 mA
10A	~70mAh	0,5 mA



- Always on
- Wireless streaming



The sound processing challenge

lots of compute power

Q

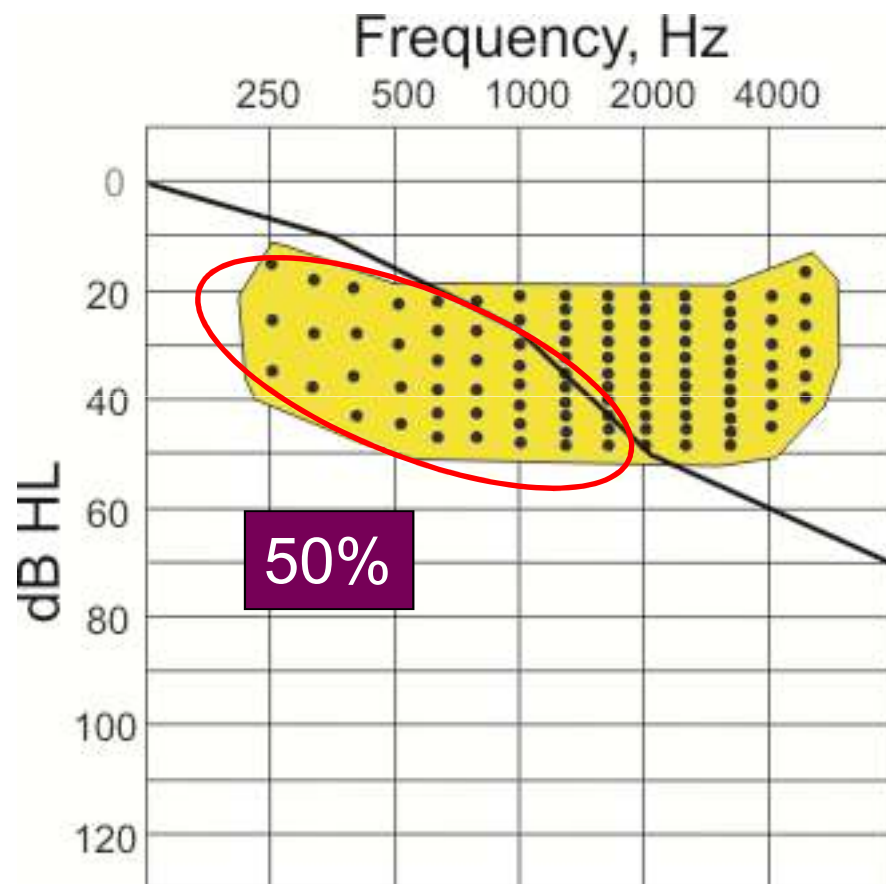
W E

R T Y U

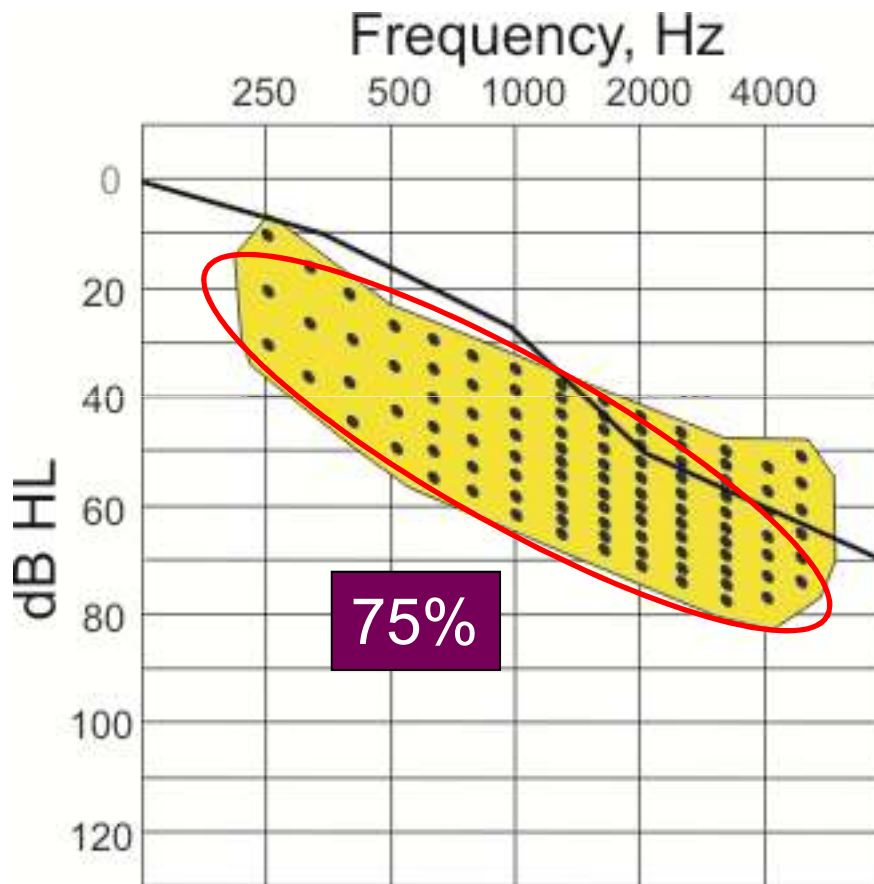
I O A S D F G H

The sound processing challenge

lots of compute power



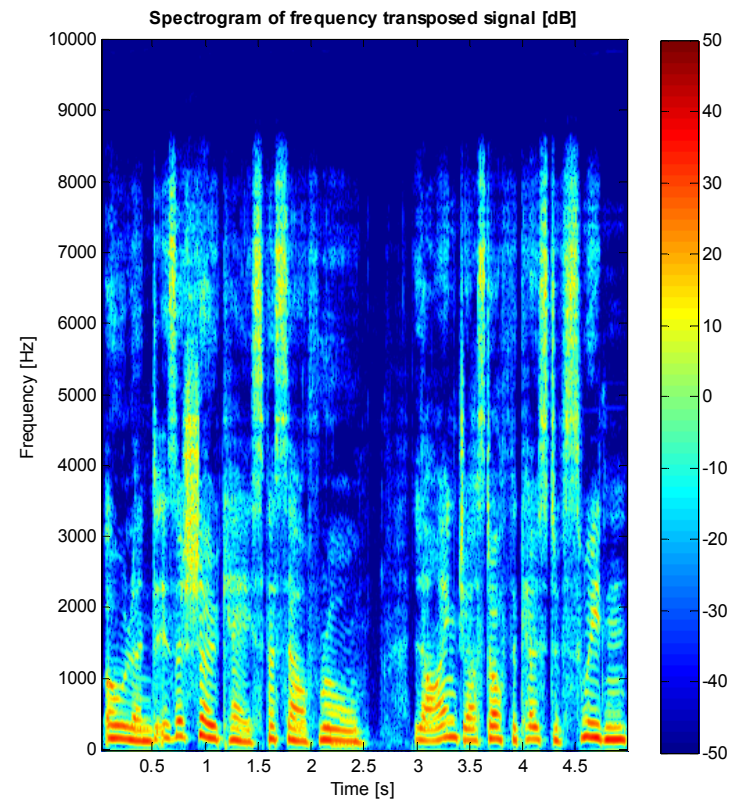
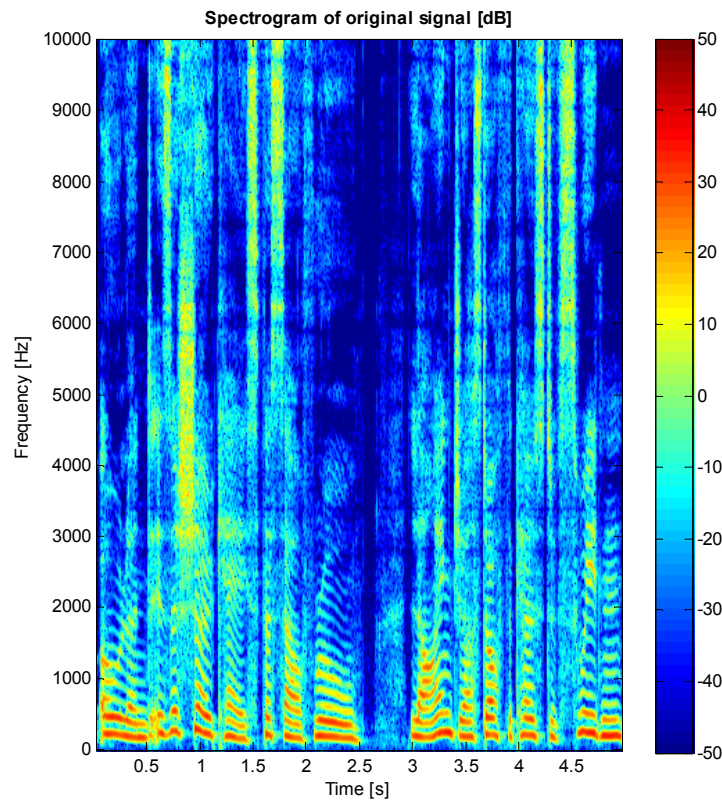
No surrounding noise, no aid



No surrounding noise, aided

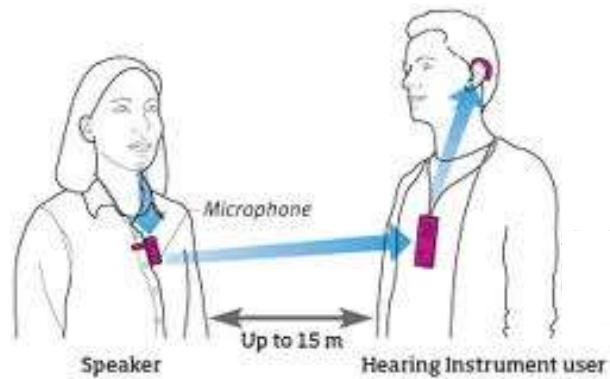
The sound processing challenge

frequency transposition



The connectivity challenge

wireless connection



- Audio streaming
- Ear to ear
- Phone
- TV
- Partner microphone

the design choices

Voltage²

Multiprocessor

NOC

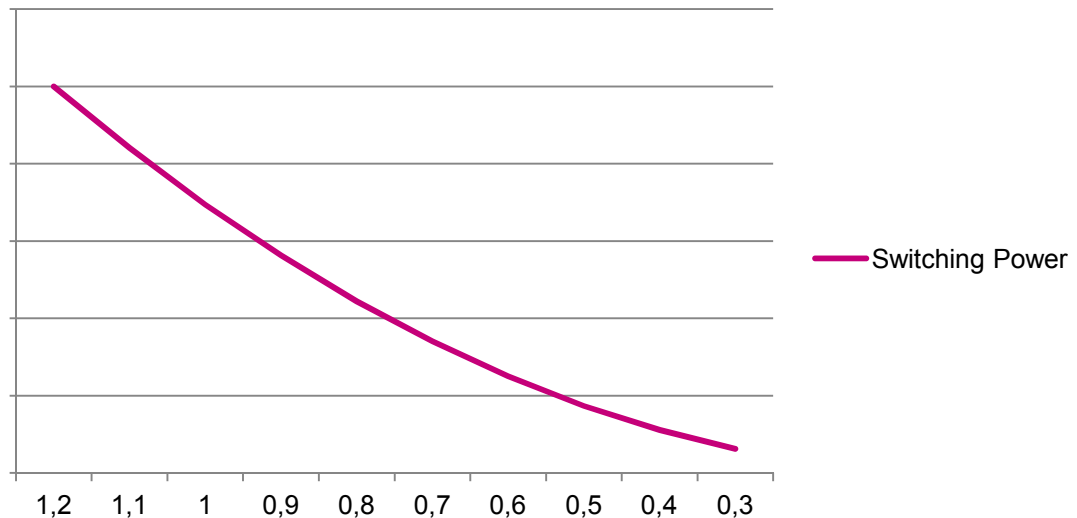
Voltage²

The best way to save power

- Switching power follows $P = V^2/R$
- Lower operating voltage -> lower power

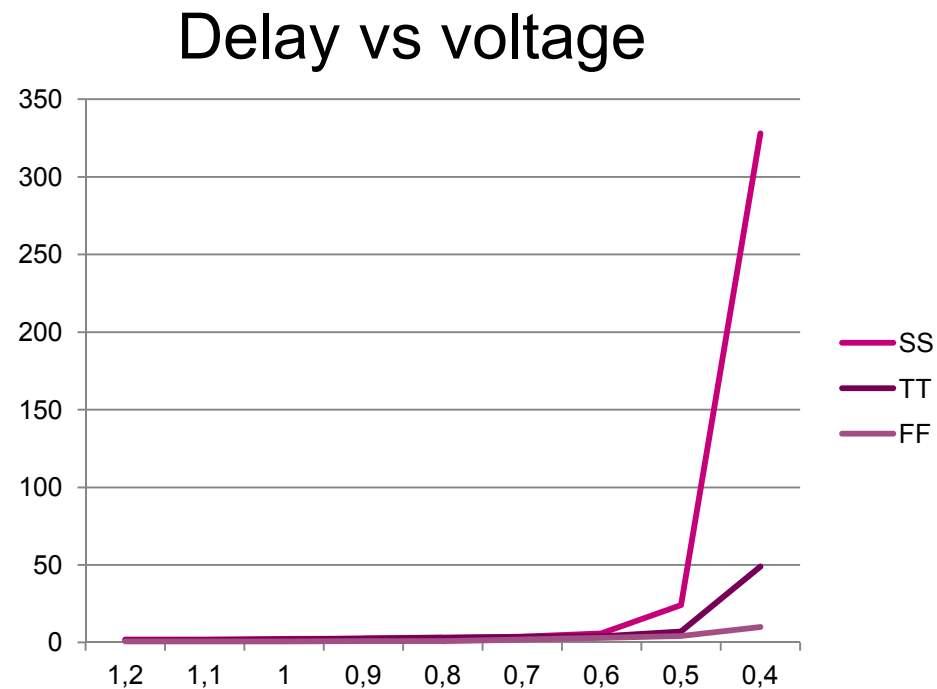


Switching Power



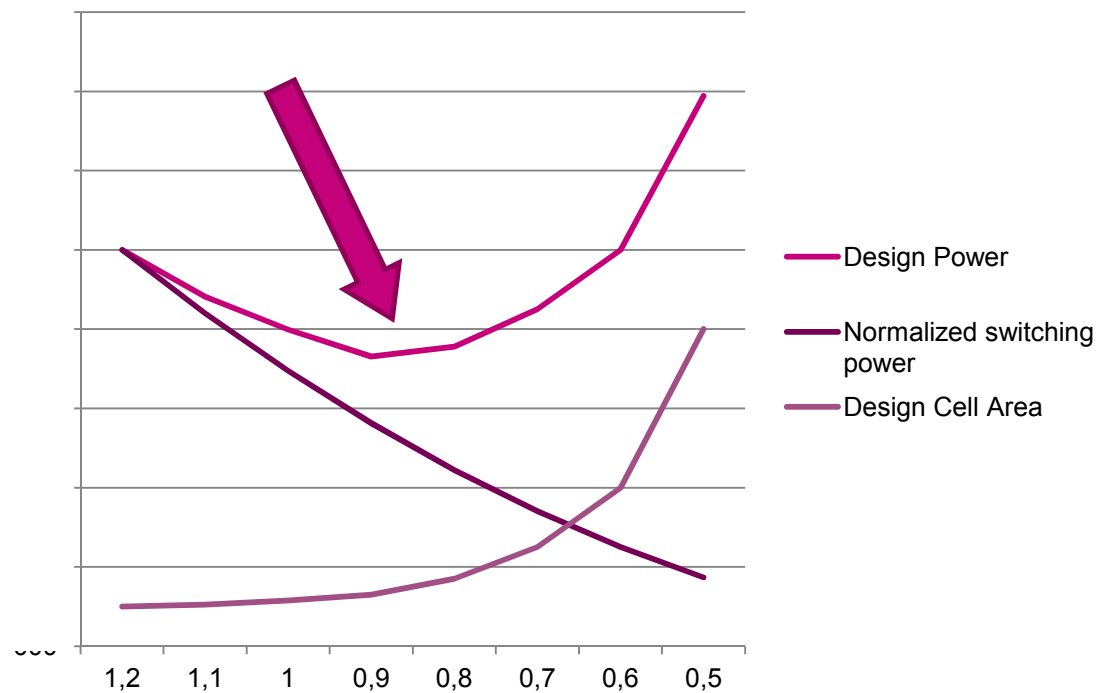
The 2Vt wall

- Approaching 2 Vt (NVt + PVt) the cell delay becomes very non linear



Optimal operating voltage

- Sweet spot between speed and power



Delay range

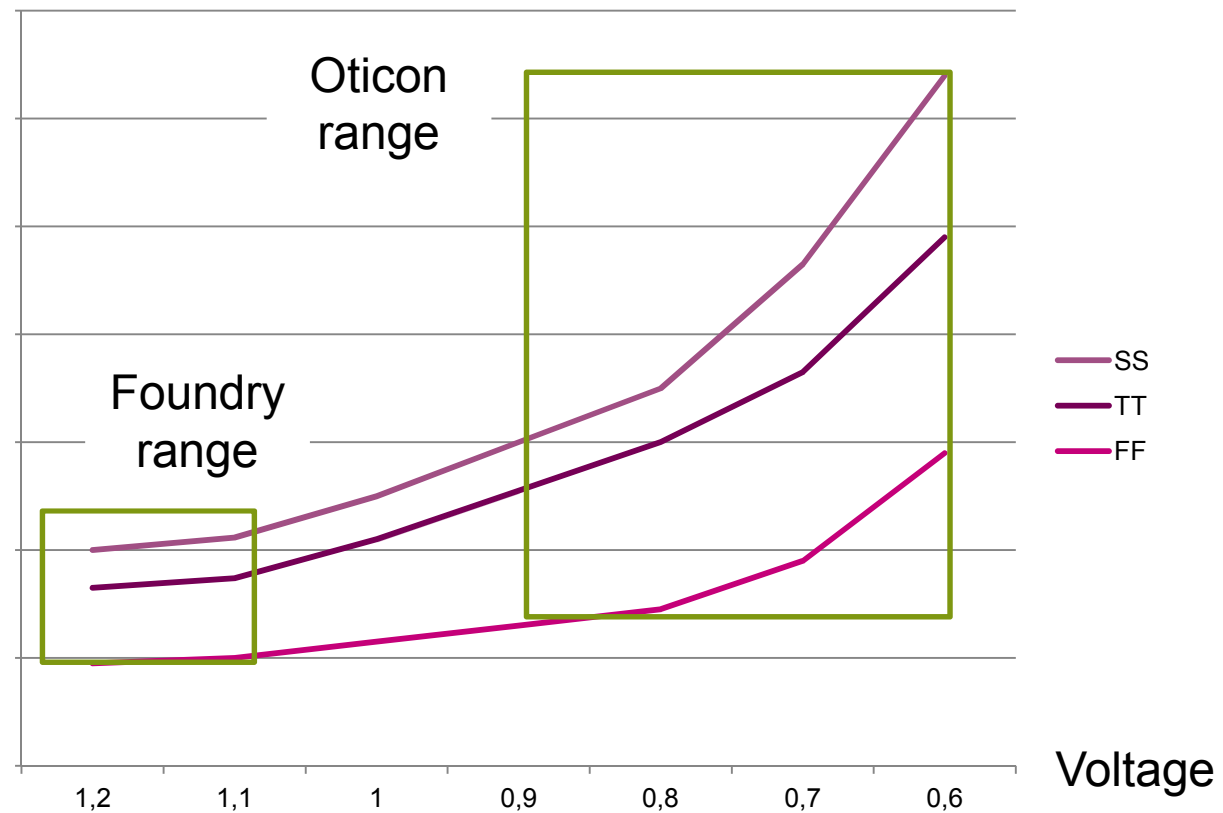
over Voltage, Silicon and Temperature

➤ Foundry range:

➤ Factor ~2

➤ Oticon range:

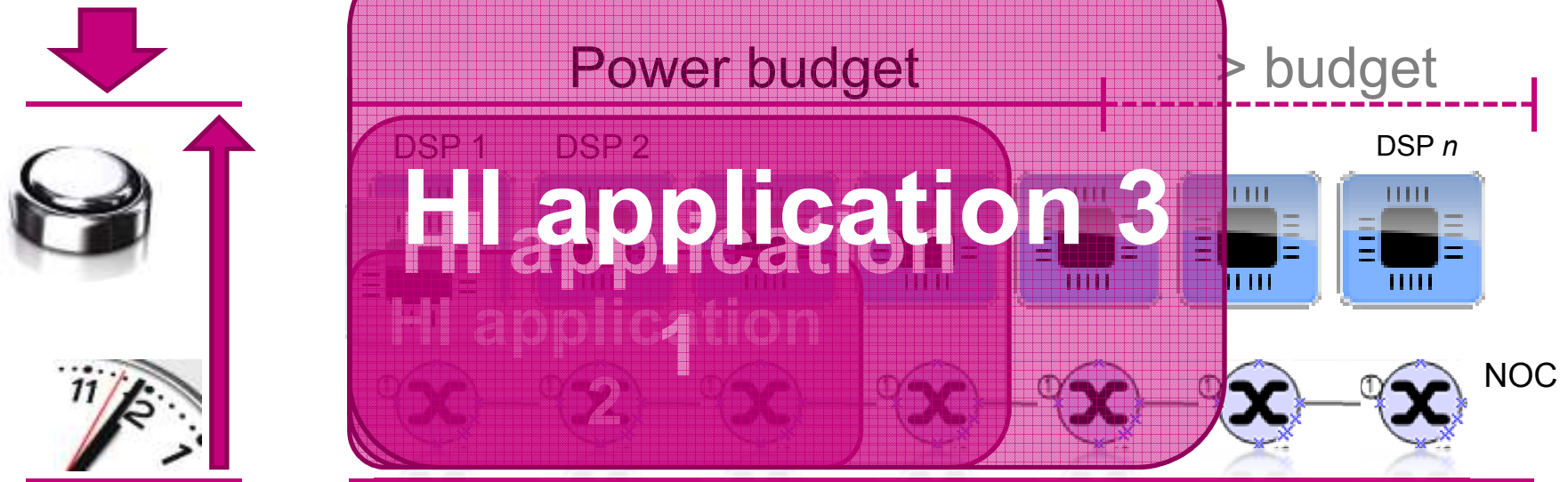
➤ Factor ~10



Constraint scenarios

- **Functional modes** : 3
- **Silicon** : 3
- **Voltage** : 5
- **Temperature** : 3
- **Parasitic – R + C** : 5
 - Sample Scenario : **mode_normal_ss_0v95_n20c_rcmin**
- Number of Scenarios to signoff : $5 * 3 * 3 * 5 * 3$ = 675
- Some can be excluded – reducing the 675 to appr. = 250
- Applying human judgment, no. of scenarios = 24

The design choices



the implementation

the processors

the NOC

the chipset

Low-power Multi-processor design

➤ Scalability

- Scalable solution to easily change number of DSP processors in future designs



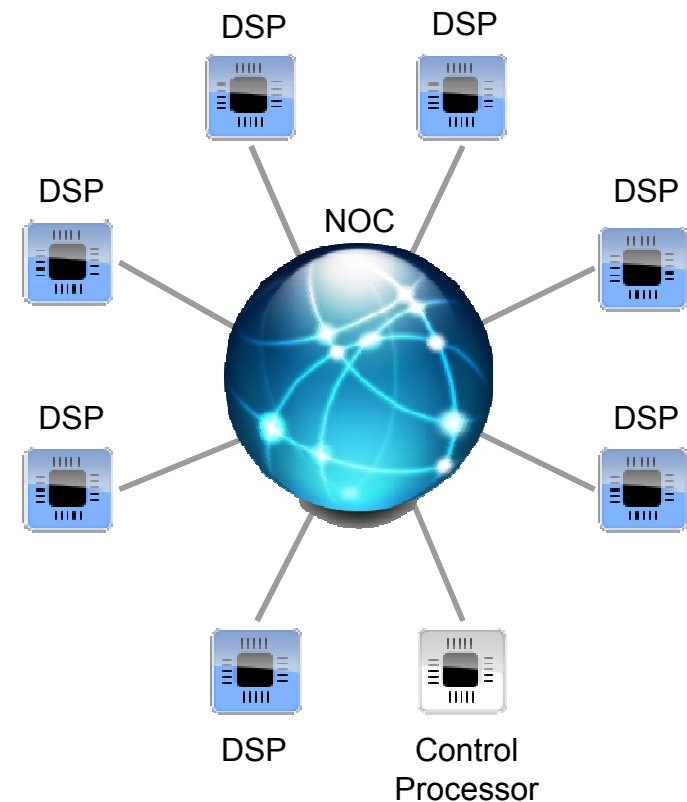
➤ Algorithm development

- Current algorithms "easily" distributed onto parallel DSP processors
 - Algorithms running on each processor can be developed and verified independently
 - Well-defined algorithm interfaces, which separate processing from communication



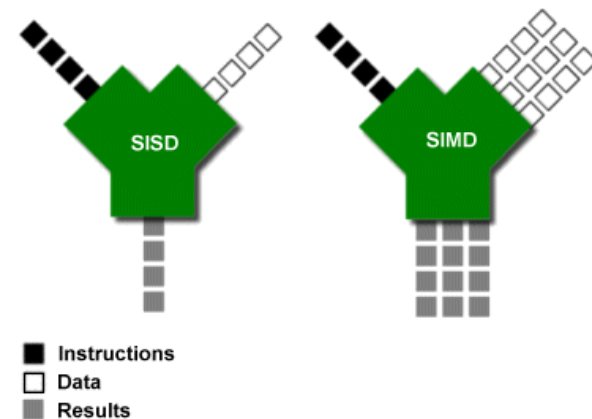
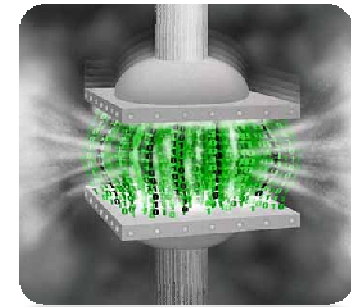
Multi-processor system

- Multi-processor platform
 - Platform based on set of DSP processors
 - Each DSP processors individually tailored for specific algorithms:
 - Same base processor (ISA) extended with different set of custom hardware accelerators
 - Different amount of dedicated data and program memory
- Control processor
 - Handles system setup and control
 - Select algorithms to be run on DSPs
 - Handles wired/wireless communication



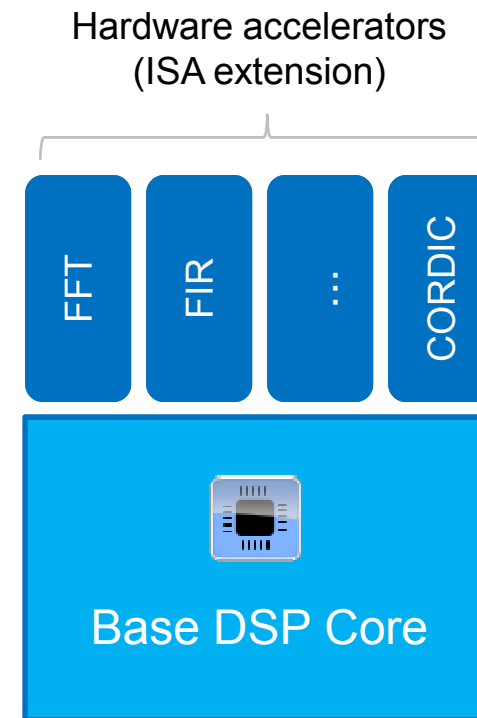
Low-power DSP processors design

- DSP Processor requirements:
 - High efficiency – “Compute power / Watt”
 - Real-time requirements
 - High code density
- Created from algorithm C source code
- DSP Processor features:
 - Vector processing datapath
 - Custom hardware accelerators
 - Parallel instructions
 - Variable instruction length



Hardware acceleration for DSP processing

- Reduce power and cycle count
 - Accelerating commonly used functionality using hardware accelerators
 - Identifying *control-intense* code
 - Identifying *compute-intense* code
- Hardware accelerators
 - Implemented as extensions to the instruction set for the base DSP core
 - Single-cycle accelerators (small)
 - Complex valued arithmetic, wide accumulators, data normalization etc
 - Multi-cycle accelerators (large)
 - FFT, FIR, CORDIC, LOG/EXP, Decoders etc





Multi-processor software development

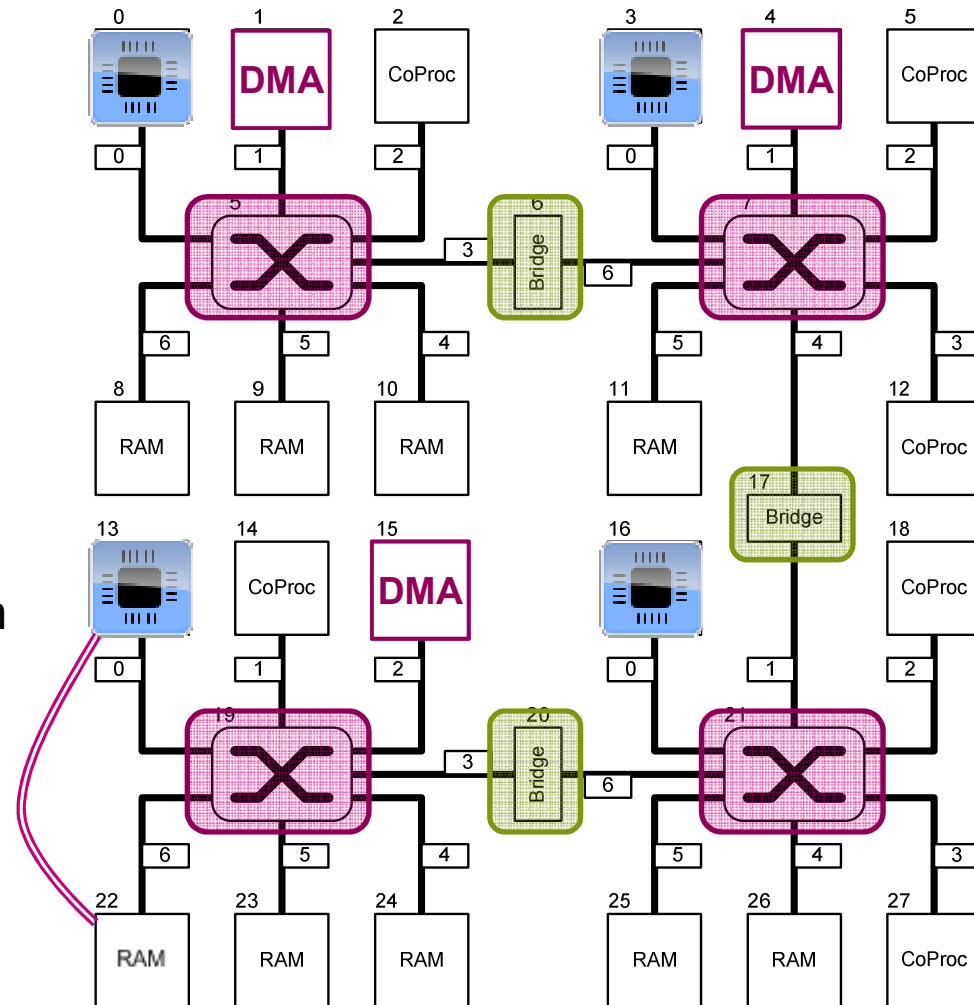
- All algorithms developed in C
 - Great advantage for developing and debugging platform/architecture independent code
- Software optimizations
 - Vector processing
 - Requires consideration about data alignment, data storage, data permutations, and memory access patterns
 - Pragmas to guide the compiler
 - Restricted data areas, software pipelining, annotated loop iteration and branch probability
- Software challenges
 - Algorithm partitioning (manual)

15X

Network on Chip

the NOC

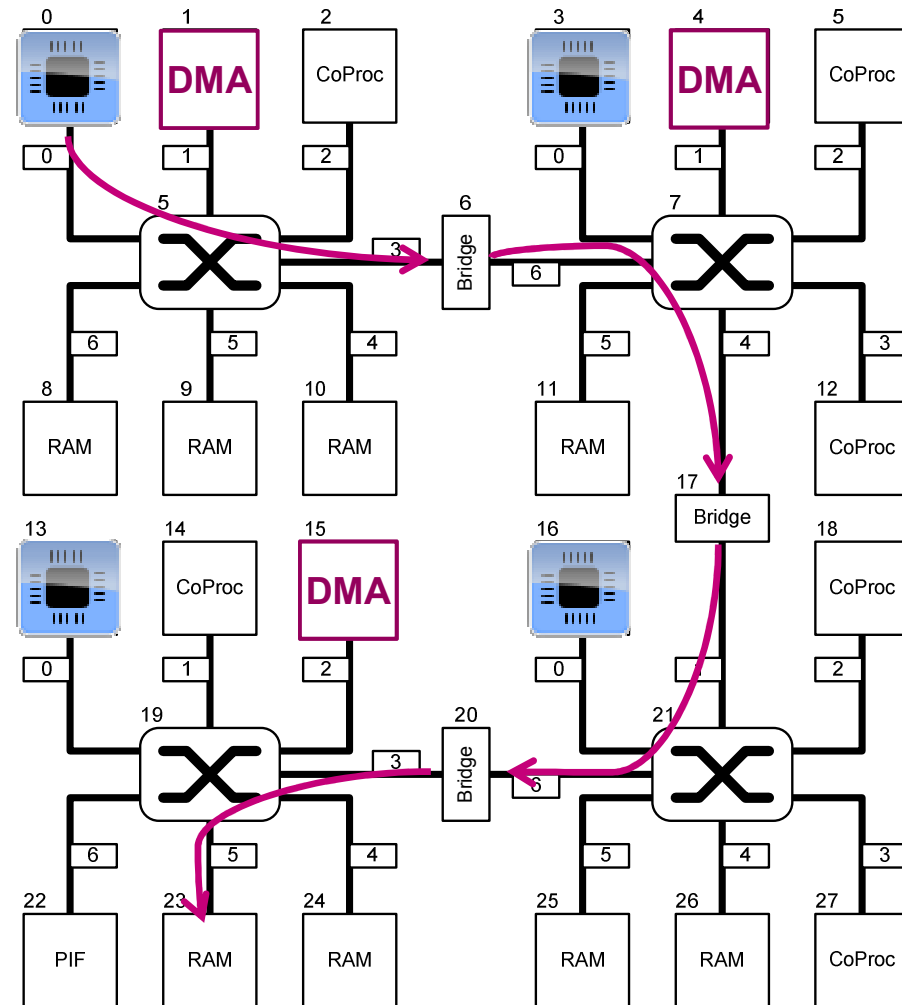
- Switch is asynchronous
- Bridge is synchronous
- Best effort, with prioritization
- No guaranteed service
- Processor has direct connection to RAM



Network on Chip

the connection

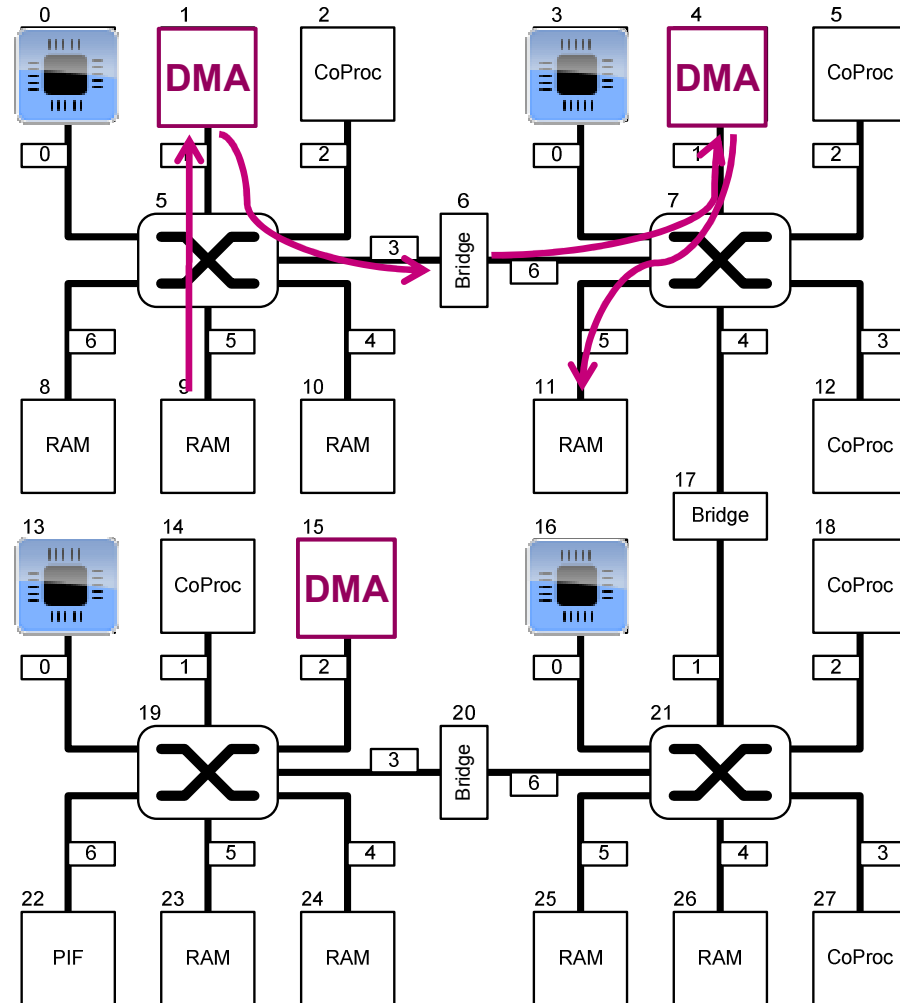
- The Control Processor can configure the routes directly
- “Connect cells” can establish route



Network on Chip

the DMA

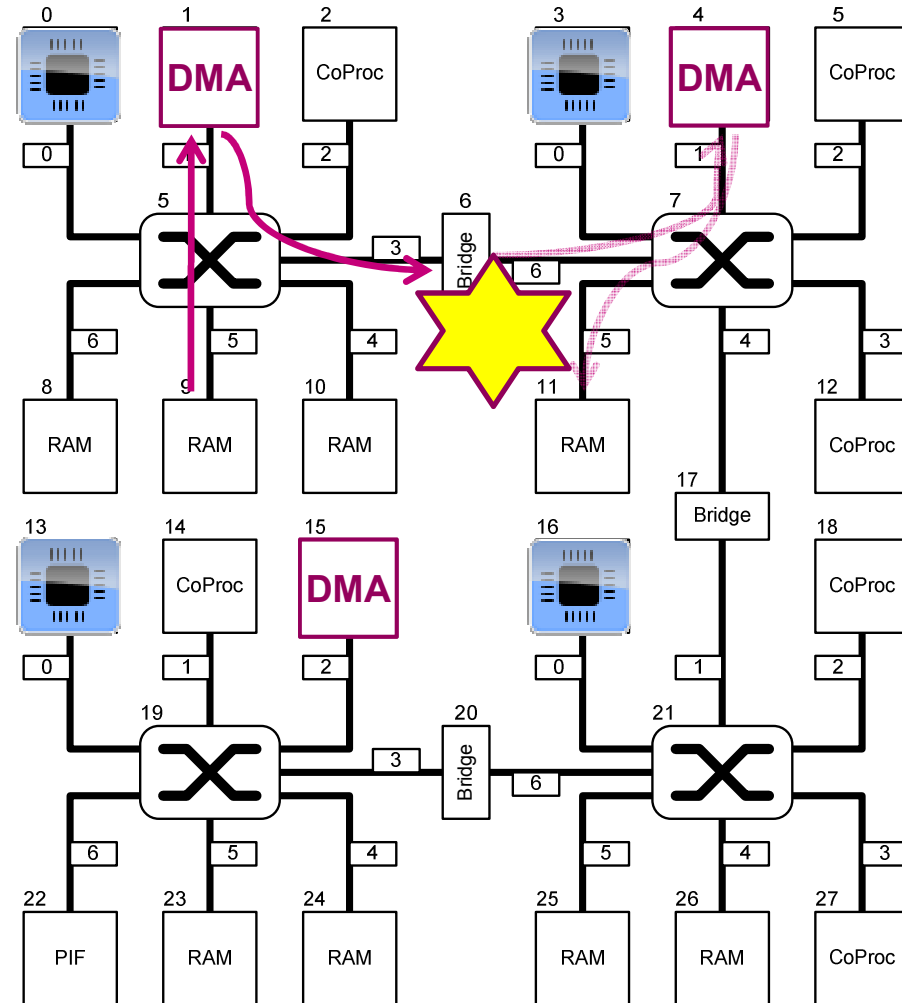
- DMA 2 DMA streams
- Reuse of DMA setup
- Interrupt on completion



Network on Chip

error handling

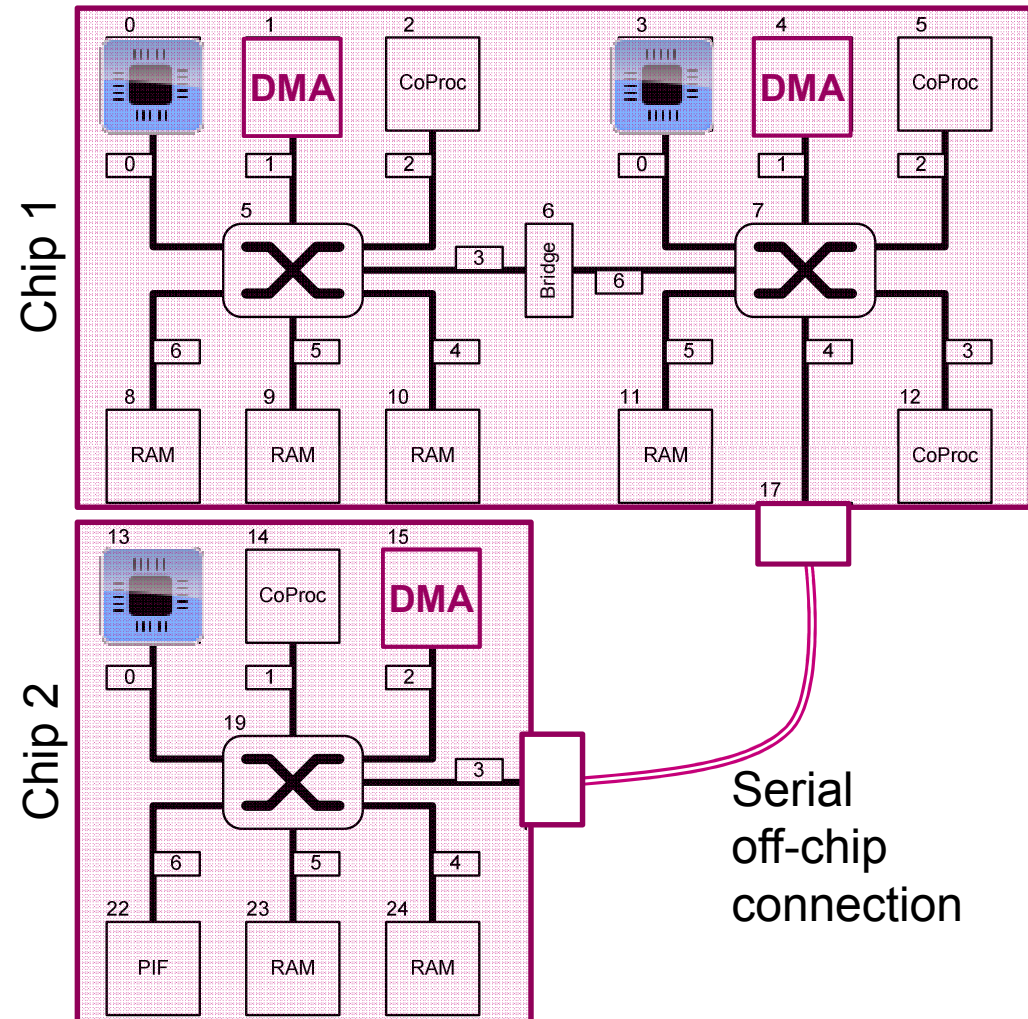
- Timeout of stalled transactions
- Debug information stored
- Different recovery options
 - Fail gracefully



Network on Chip

long connections

- NOC between chips



The chipset

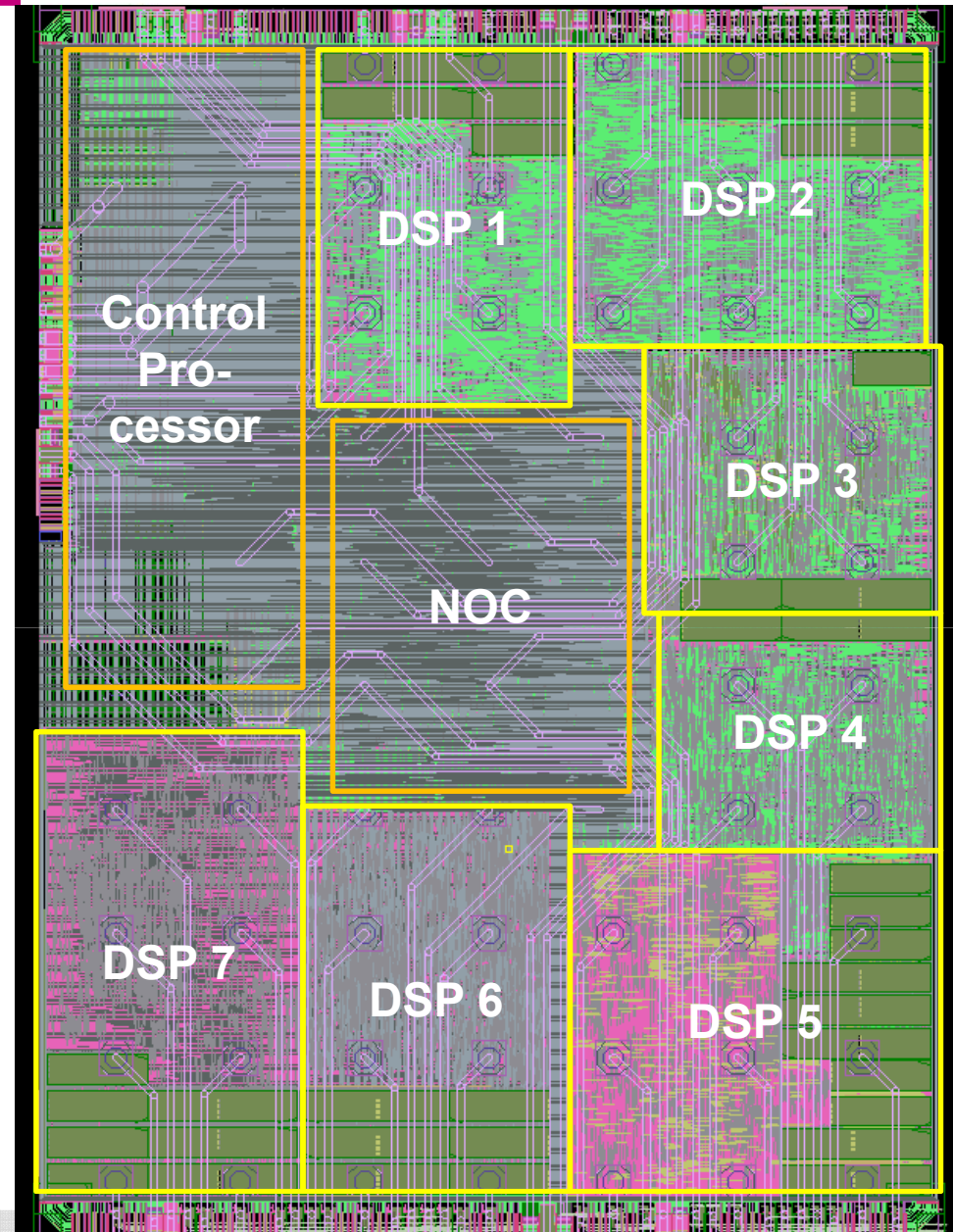
$2,75 \times 3,74 = 10,2\text{mm}^2$

35M transistors

8½M gates

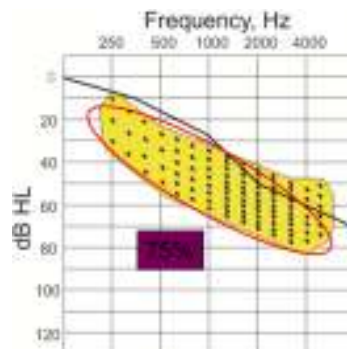
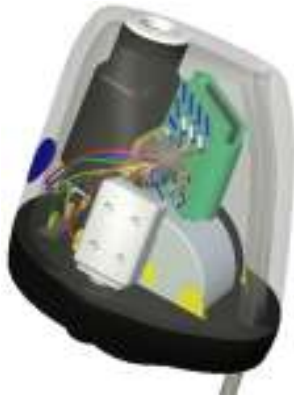
1,3M wires

52m total wire length



summary

Summary



- So much room for improvement
- So much more to learn
- Keep researching
- We need talent



the end

thanks for listening