Self Synchronous Circuits for Error Robust Operation in Sub-100nm Processes

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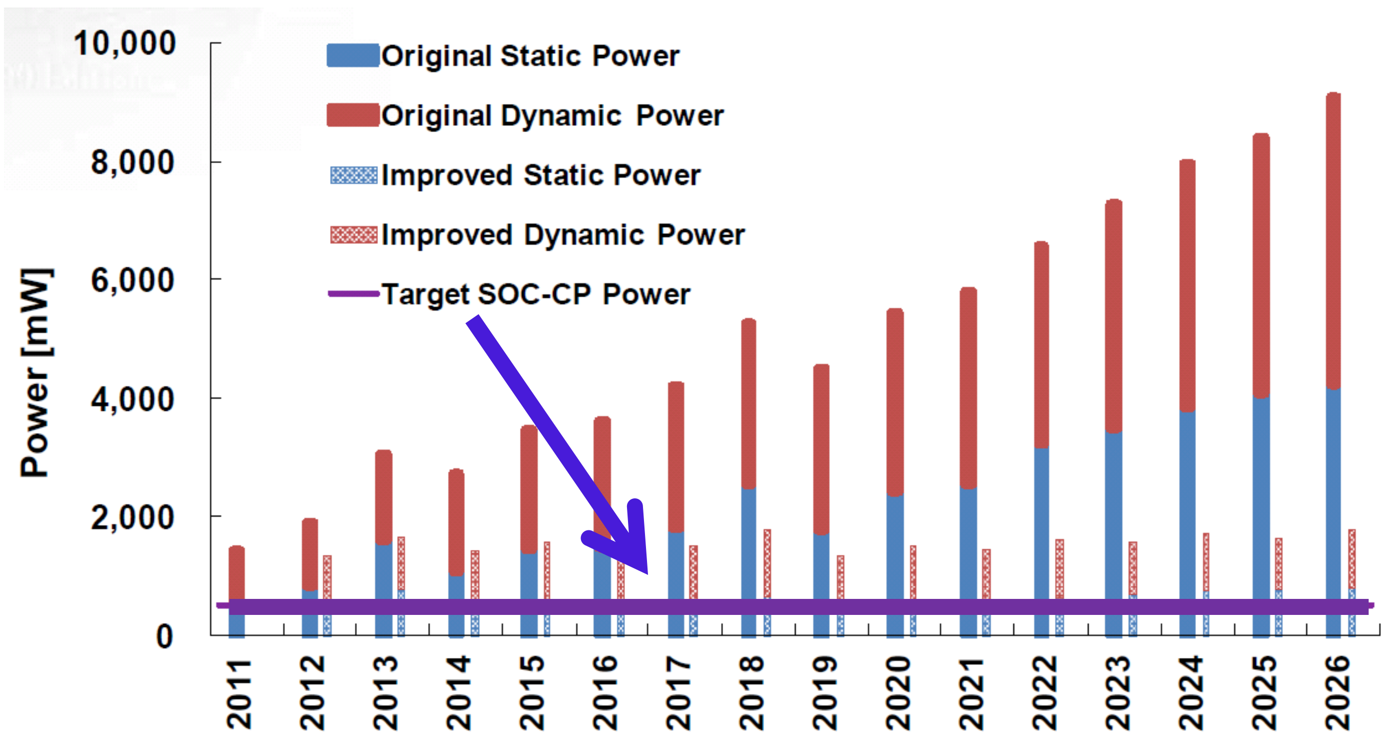
Overview

- Motivation
- Self Synchronous Circuits
  - Self Synchronous Circuit Failure Modes
  - Self Synchronous FPGA Architecture
- Error Robustness Techniques and Measurements
  - 65nm – Watchdog error detection
  - 40nm – Pipeline disabling after error detection
  - Programmable Redundancy
- Analysis of Robustness to SEUs
- Conclusions

Motivation – Low Power Designs

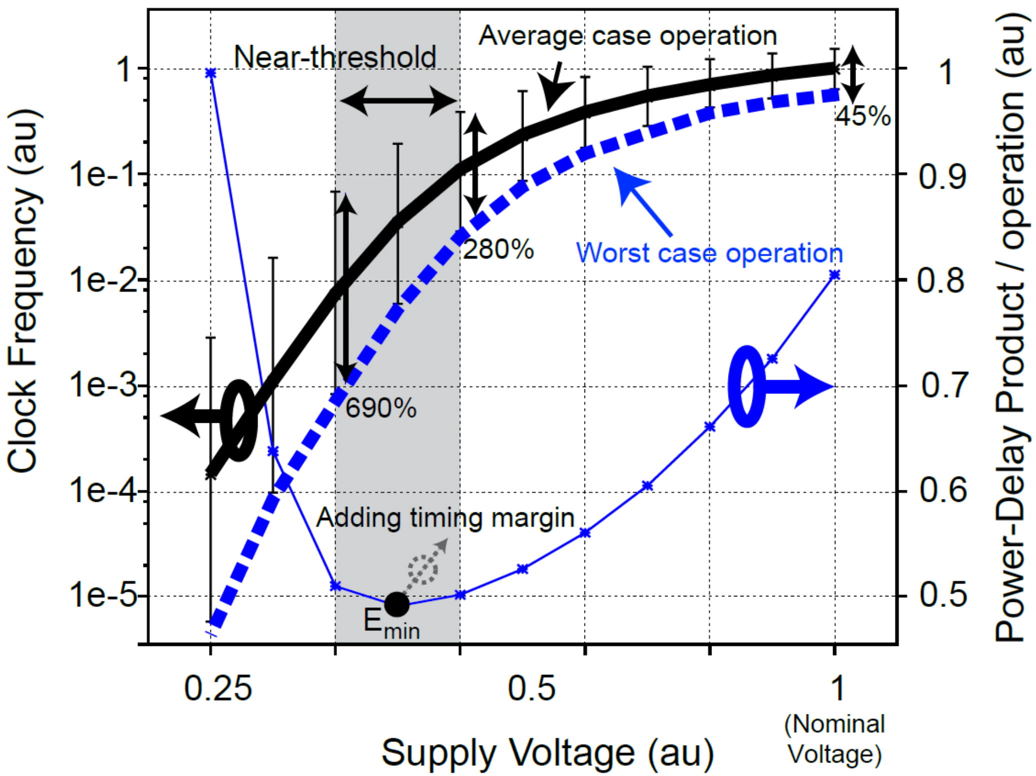
- ITRS report shows need for low power designs
  - Still 2x over target with techniques such as frequency islands, low voltage, power aware software, many core development software
  - Process scaling and Voltage scaling are popular



[ITRS 2011 Winter Public Conference]

Motivation – Coping with Variation

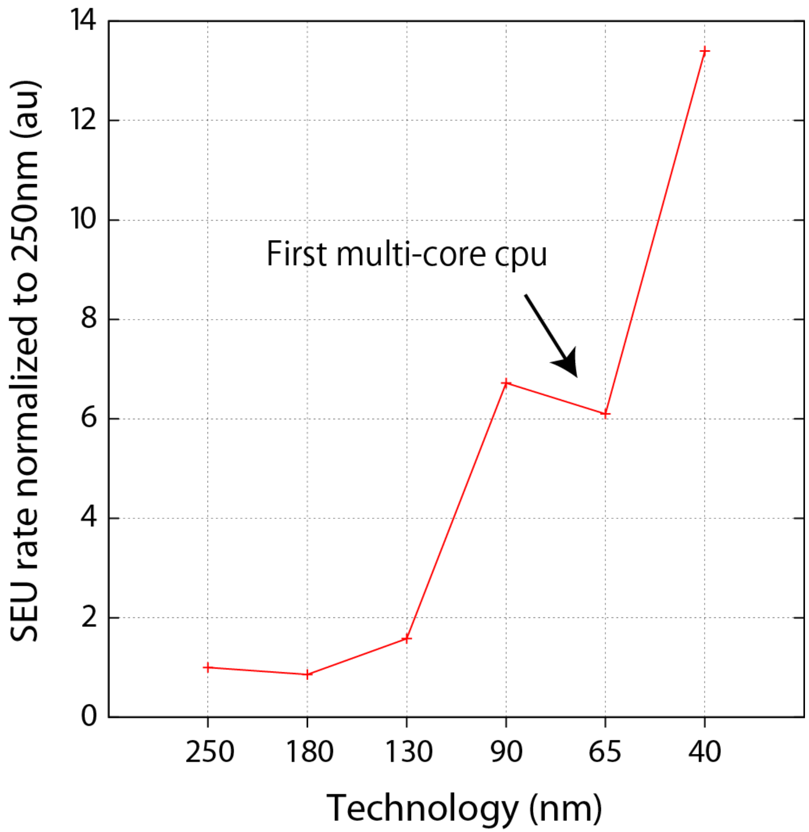
- <u>Low voltage synchronous systems require large design effort</u>
  - "A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS" **ISSCC 2012**
    - o Programmable delay
    - o Programmable level shifters
    - o All devices <2x minimum gate width removed
  - "A 200mV 32b Sub-threshold Processor with Adaptive Supply Voltage Control" **ISSCC 2012**
    - o Control loops
    - o Voltage regulators
    - o Configurable ring oscillators

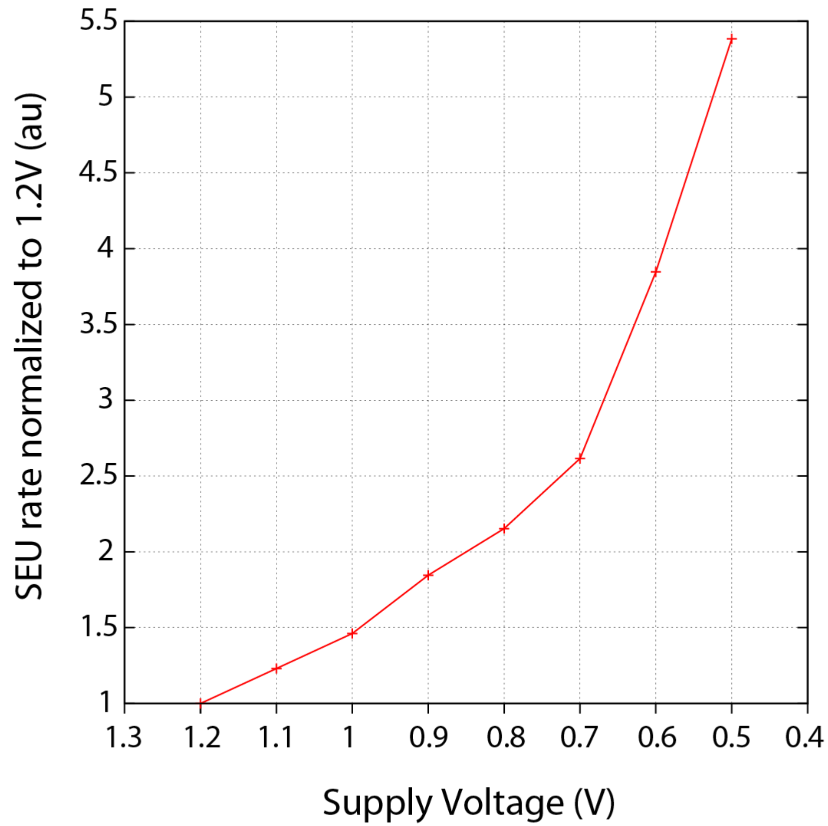


(65nm Post-layout simulation results of a self synchronous buffer)

Motivation – SEU Increase

- Single event upsets (SEU) causes logic errors [1]
  - Which is becoming worse with process and voltage scaling





[1] A. Dixit, A. Wood, "The impact of new technology on soft error rates", IEEE Reliability Physics Symposium 2011

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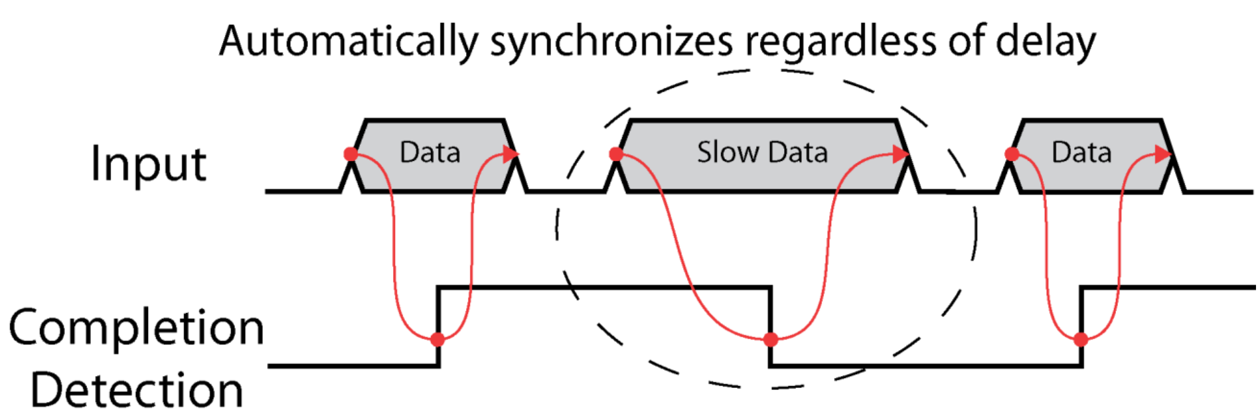
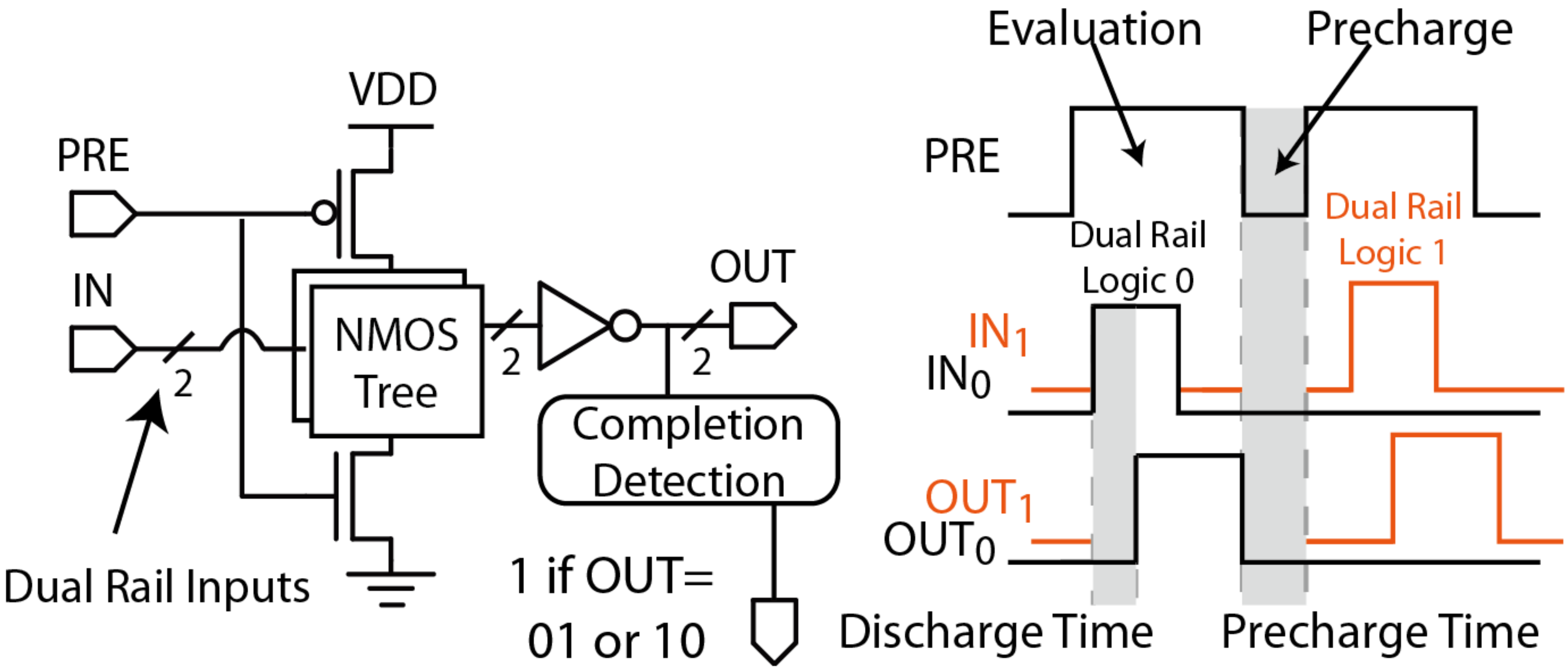
Self Synchronous Circuits

- Self synchronous circuits are asynchronous circuits with bit-level completion detection circuits for qdi operation
  - Gate Level Self Synchronous circuits can provide reliable operation within PVT (Process, Voltage, Temperature) variations compared to Synchronous circuits
  - No need for timing margins, ideal for low voltage operation
  - Dynamic circuits, dual rail, 2 phase signaling



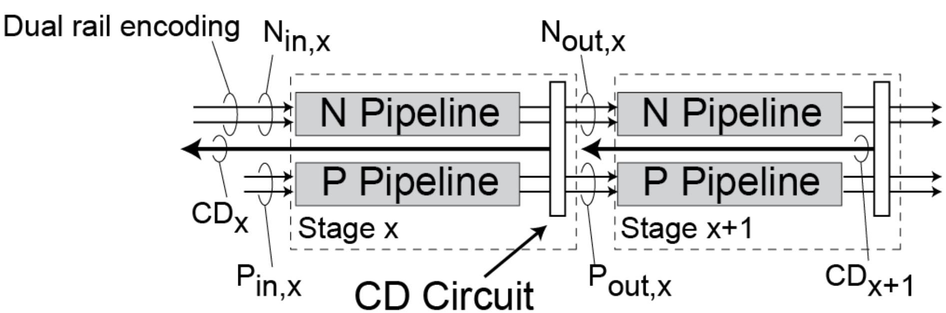
Dynamic Self Synchronous Circuits

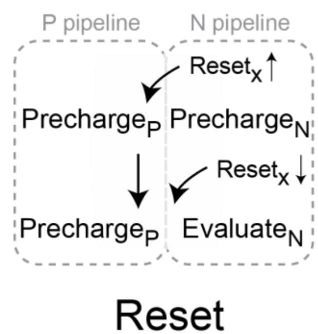
- DCVSL for high throughput
- Precharge and Evaluation cycle Evaluation is fast but precharging takes time!
  - o Can we conceal this time wastage??

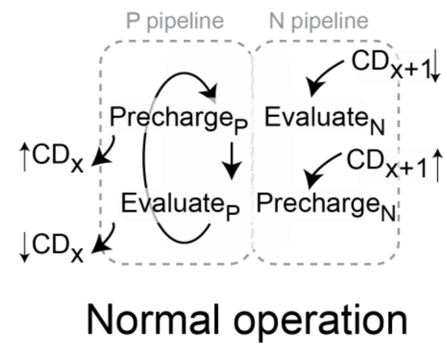


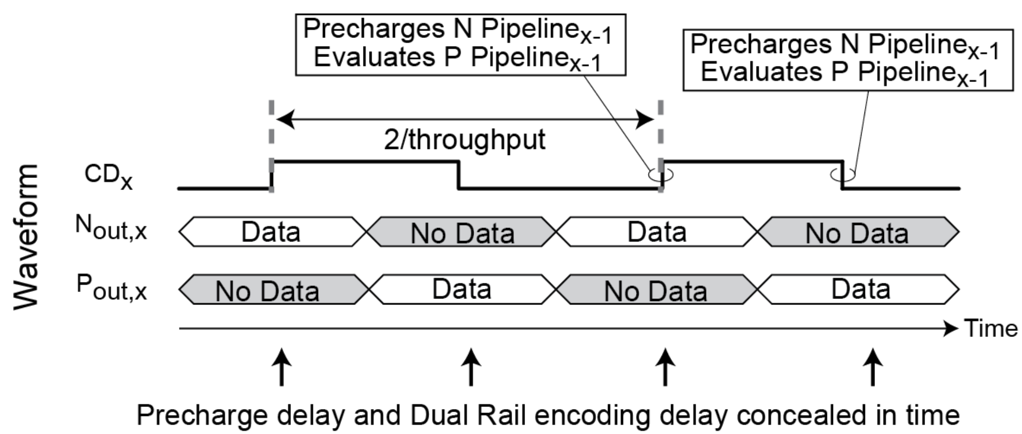
Self Synchronous Dual Pipeline

- Gate-level pipeline stages controlled with completion detection (CD) circuits
- Dual pipeline increases throughput
- Dual rail returns to zero due to CD_{x+1}



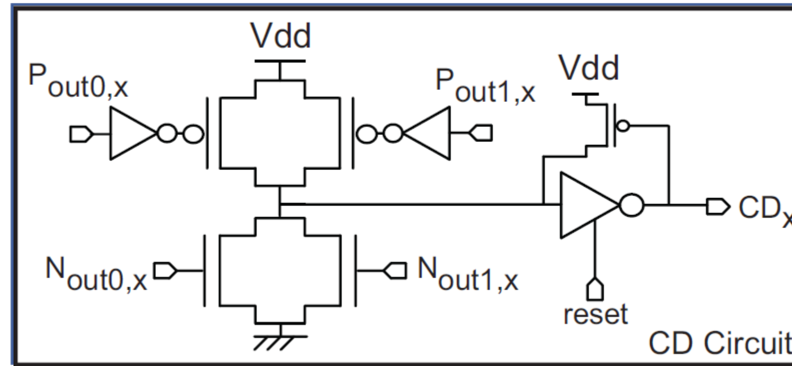


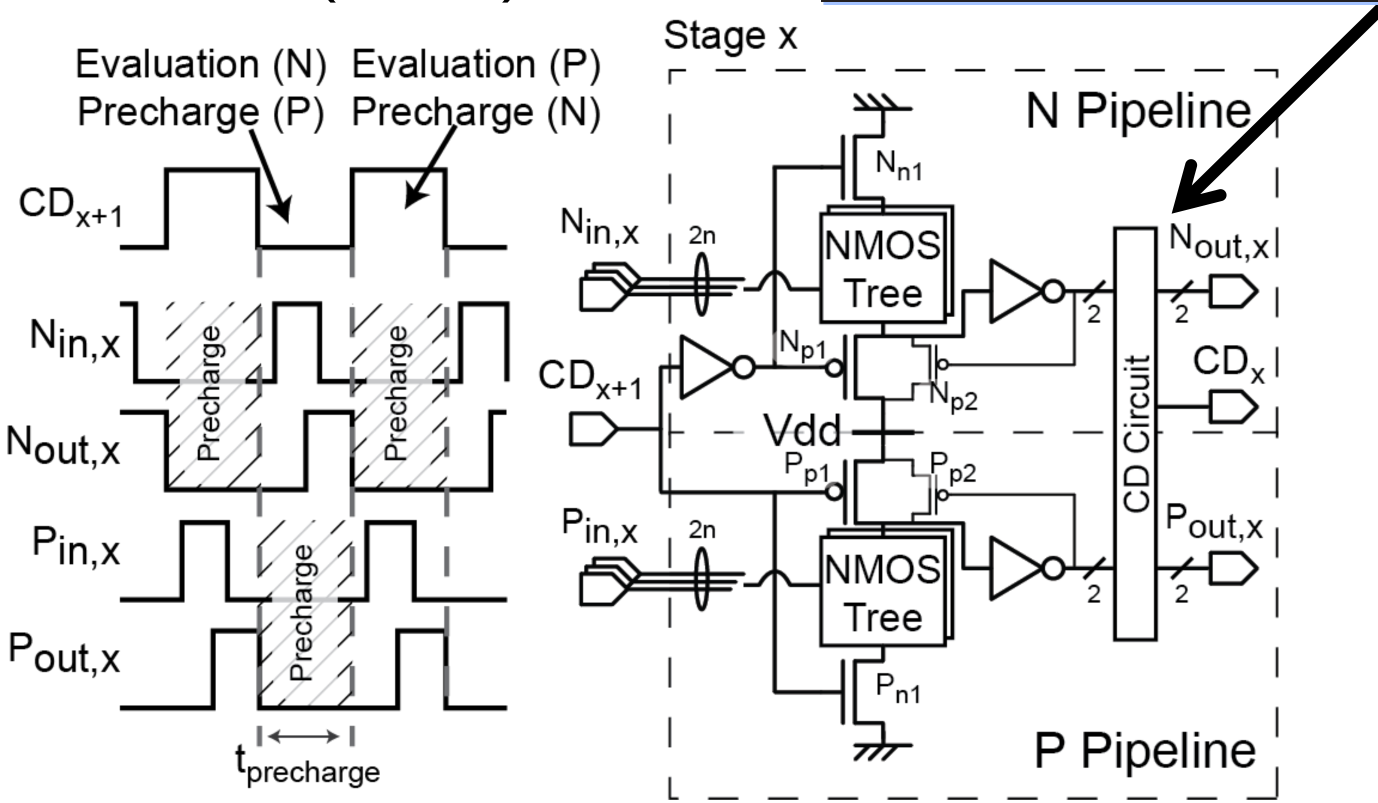




Circuit Diagram of Dual Pipeline and CD

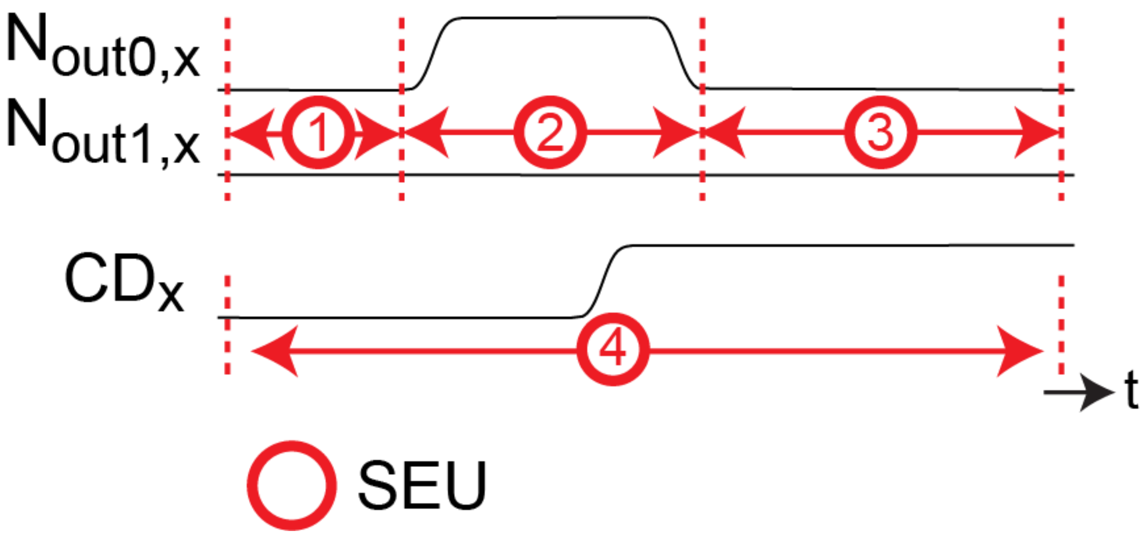
- + Precharge time is concealed
- + Small CD delay
- + No explicit latches
- - Area overhead (~66%)





Self Synchronous Failure Modes (N)

- Dual-rail dual-pipeline circuits are almost self-checking [1], some cases where SEU could occur are:
  1. Depending on timing - CD_x will toggle, freezing operation, or undetected "10", "01" will pass (not self checking)
  2. "11" error
  3. Blocked
  4. Operation freezes

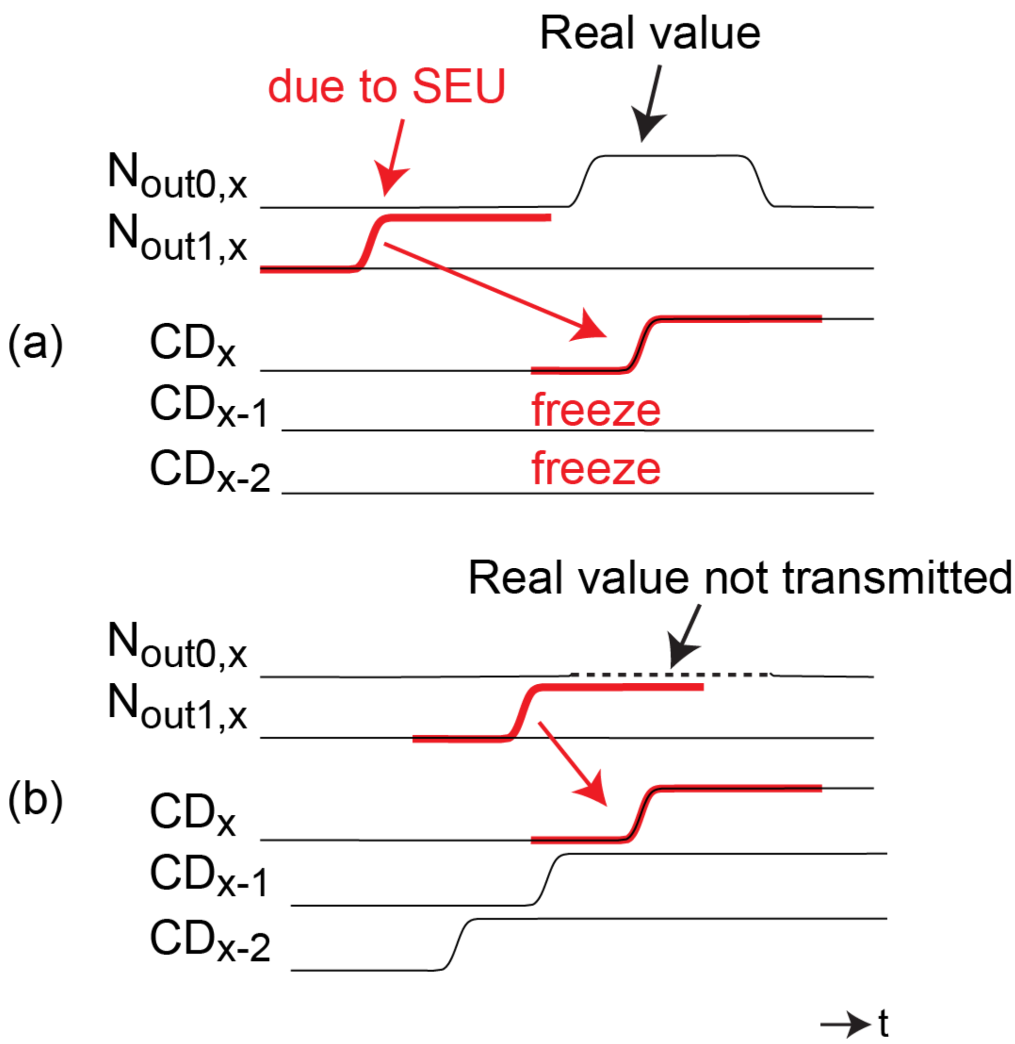


[1] I. David, R. Ginosar, and M. Yoeli, "Self-timed is self-checking," *Journal of Electronic Testing*, vol. 6, pp. 219–228, 1995.

Undetectable error in ①

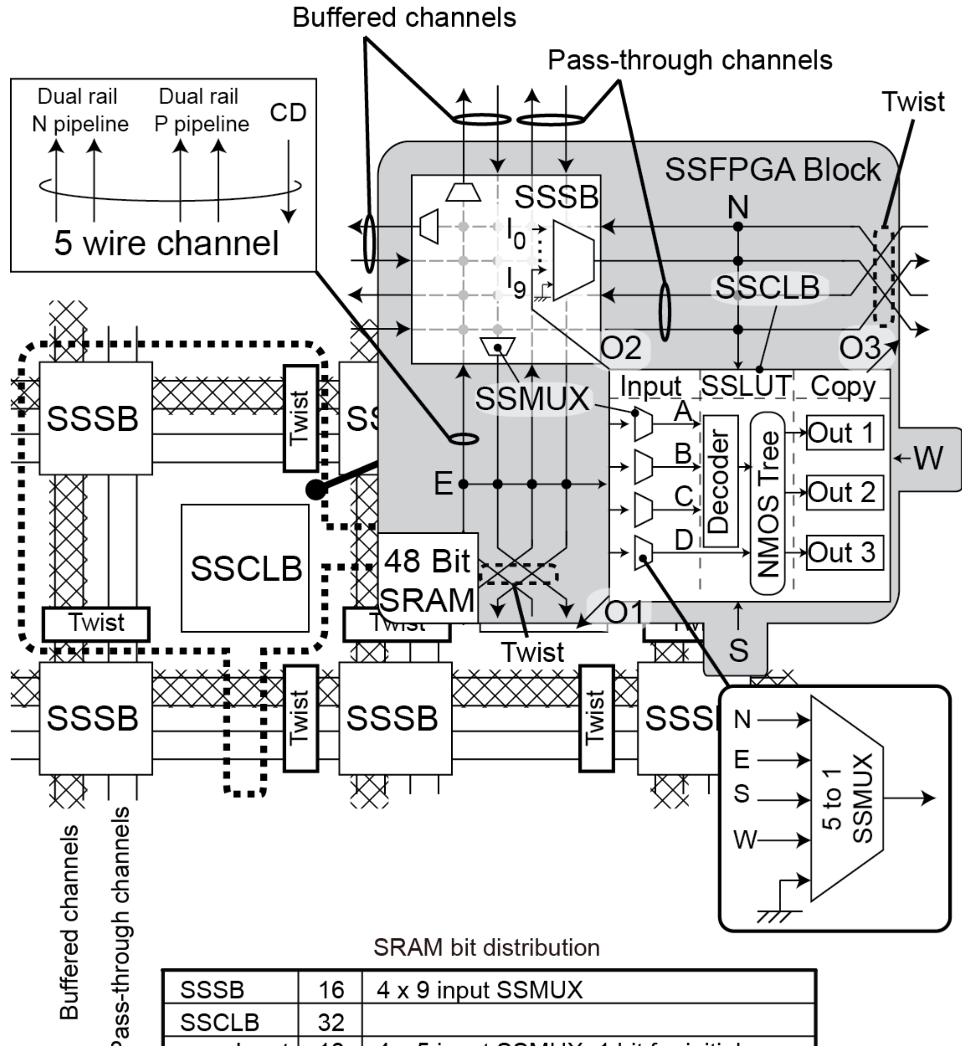
a. If a SEU causes N_{out} to toggle before $CD_{x-1,x-2}$, the pipeline will freeze

b. If a SEU causes N_{out} to toggle after $CD_{x-1,x-2}$, the pipeline will not freeze and an error can propagate undetected



Implemented Architecture - Self Synchronous FPGA

- Self Synchronous Switch Block (SSSB)
- Self Synchronous Configurable Logic Block (SSCLB)
- Self Synchronous MUX's are used as gate-level buffers
- All blocks are dual pipeline DCVSL
- Used as base for robustness circuits



SRAM bit distribution

SSSB	16	4 x 9 input SSMUX
SSCLB	32	
Input	13	4 x 5 input SSMUX, 1 bit for initial_gen
SSLUT	16	4 input SSLUT
Copy	3	3 copy blocks
Total bits	48	

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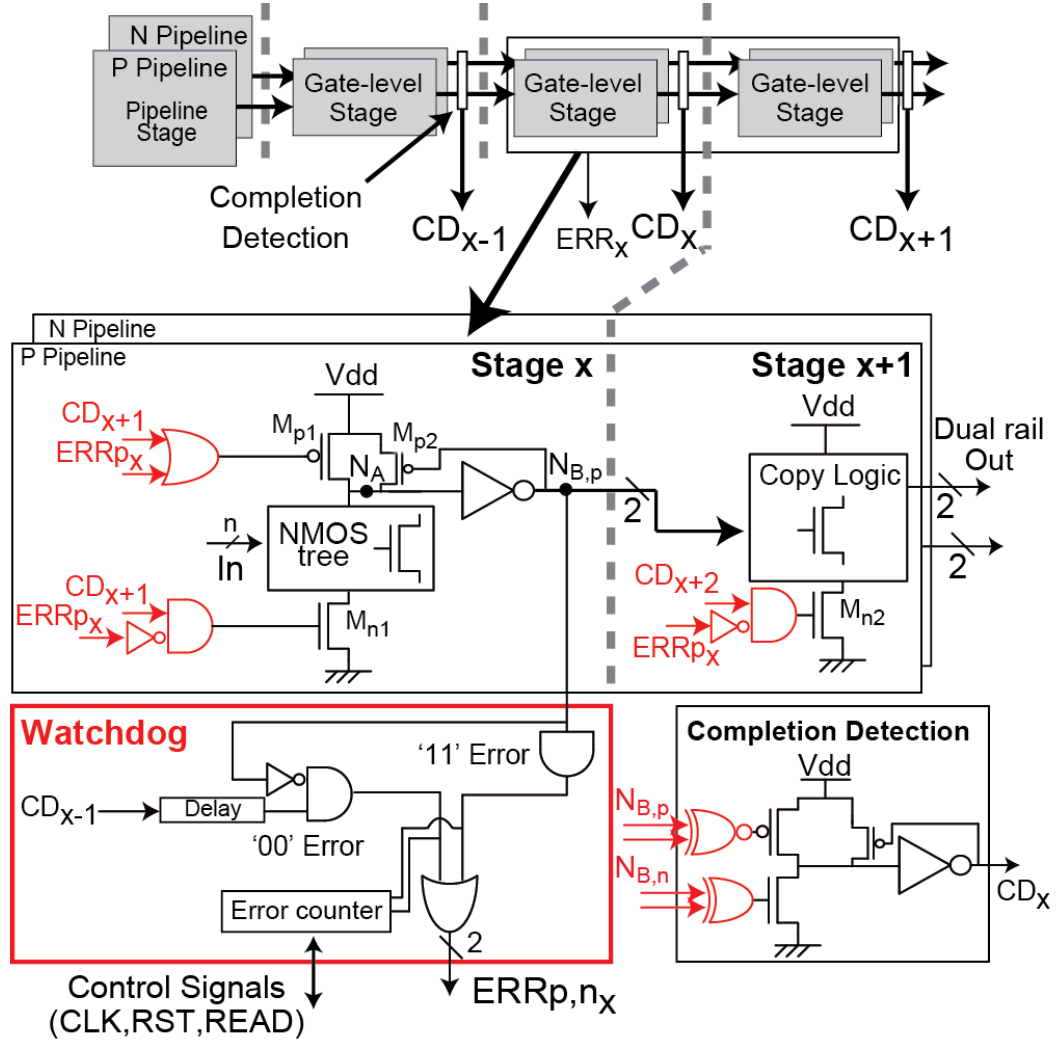
Watchdog Circuit

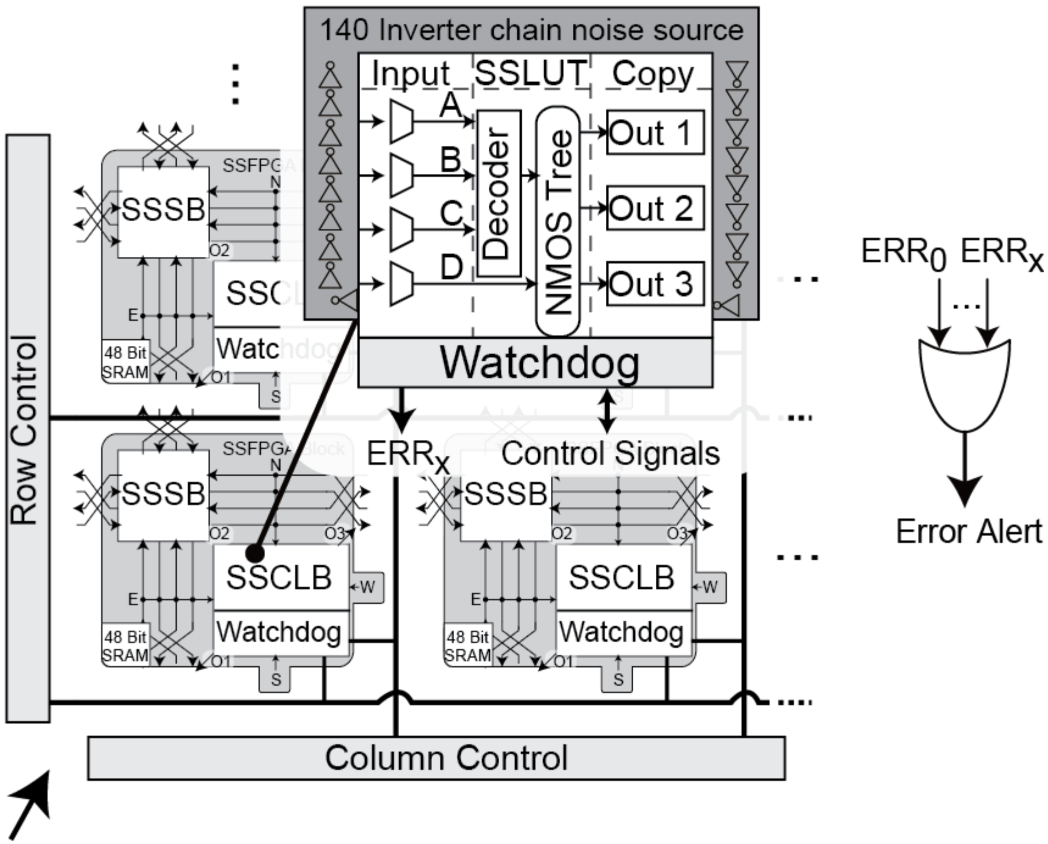
- '11' and '00' Error detection
- Error propagation prevented
- Operation is autonomously re-performed
- Watchdog circuit monitors number of errors in each gate-level stage
- Conventional method in black, additional circuits in red



[1] Devlin, B.; Ikeda, M.; Asada, K., " Gate-Level Autonomous Watchdog Circuit for Error Robustness Based on a 65nm Self Synchronous System," ICECS 2011

Chip Implementation

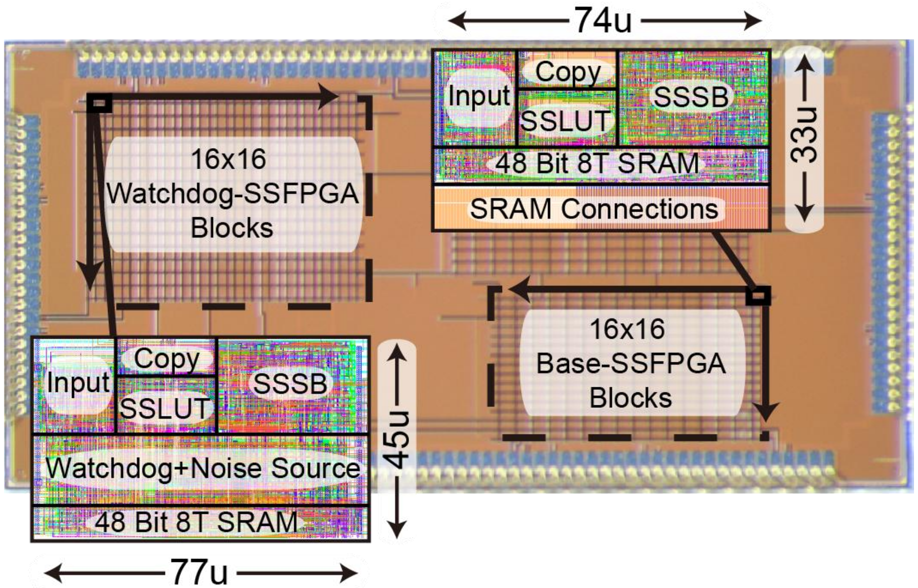
- Watchdog implemented in every SSFPGA block with 140 inverter noise source

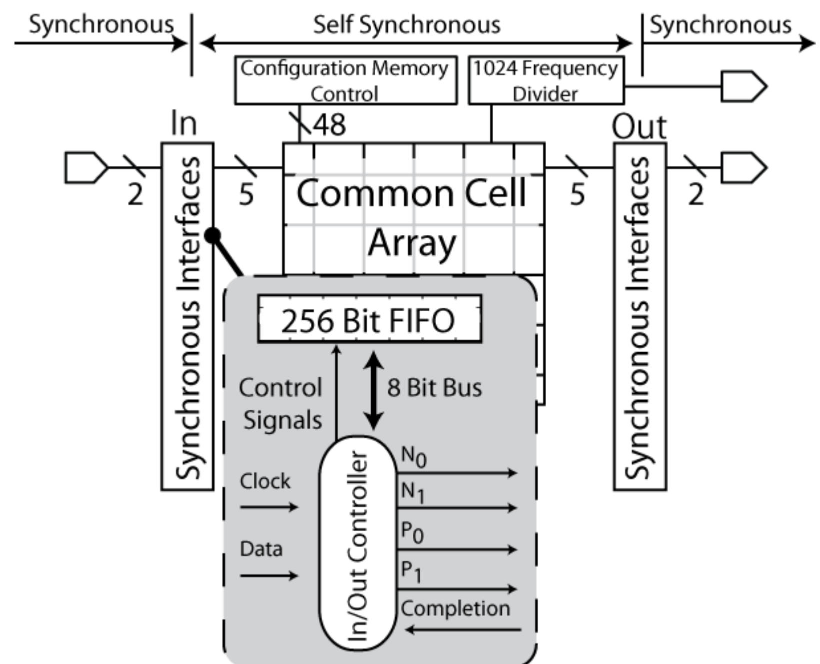


(Row and column address decoders for error count readout)

65nm Fabricated Chip

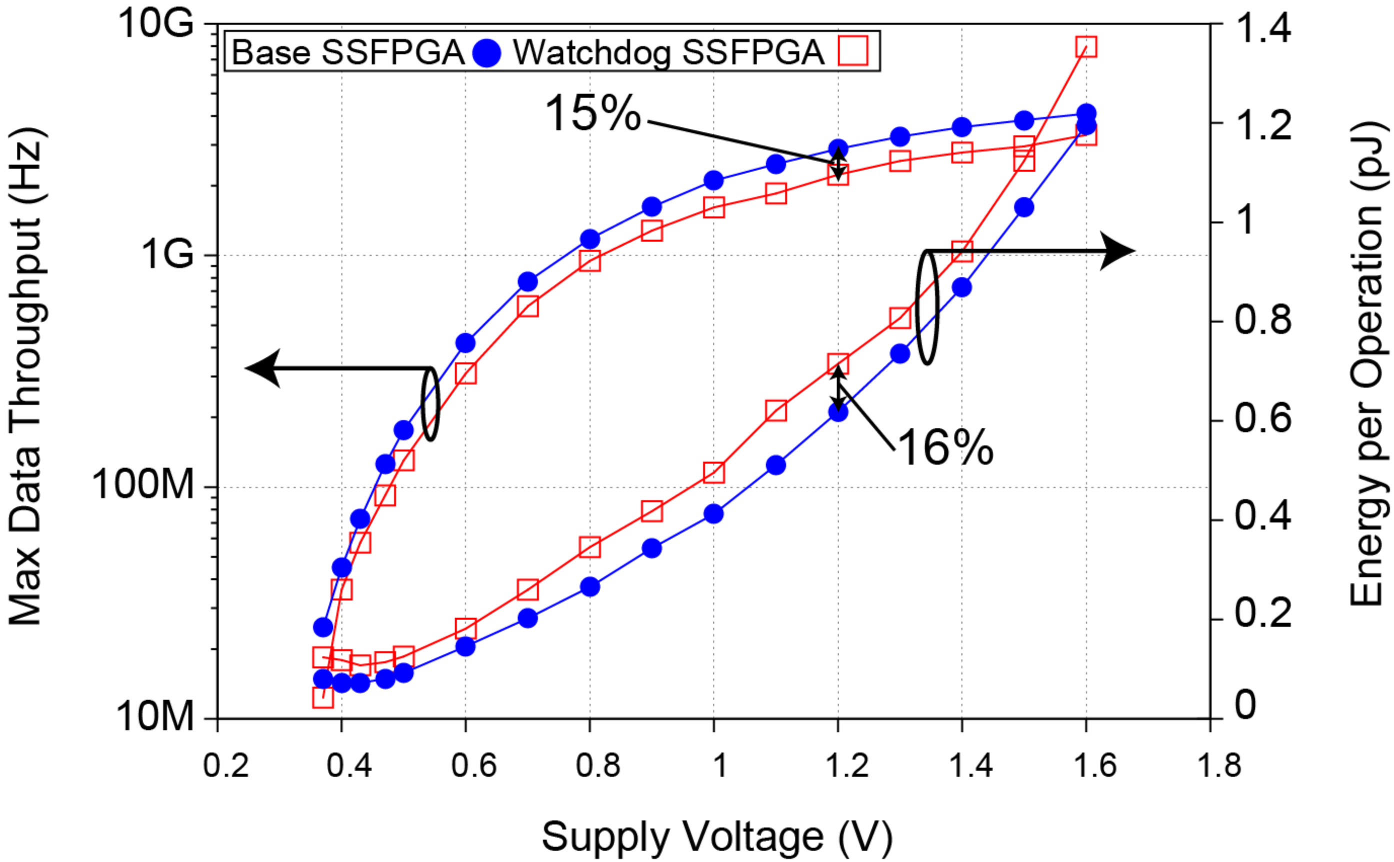
- 2mm x 4mm chip fabricated in 65nm 12ML CMOS process
- Internal operating speed measured by frequency divider
- Input and Output Interfaces with 256bit SRAM FIFO
- Hand layout + some automatic wire routing
- Base SSFPGA + Watchdog SSFPGA





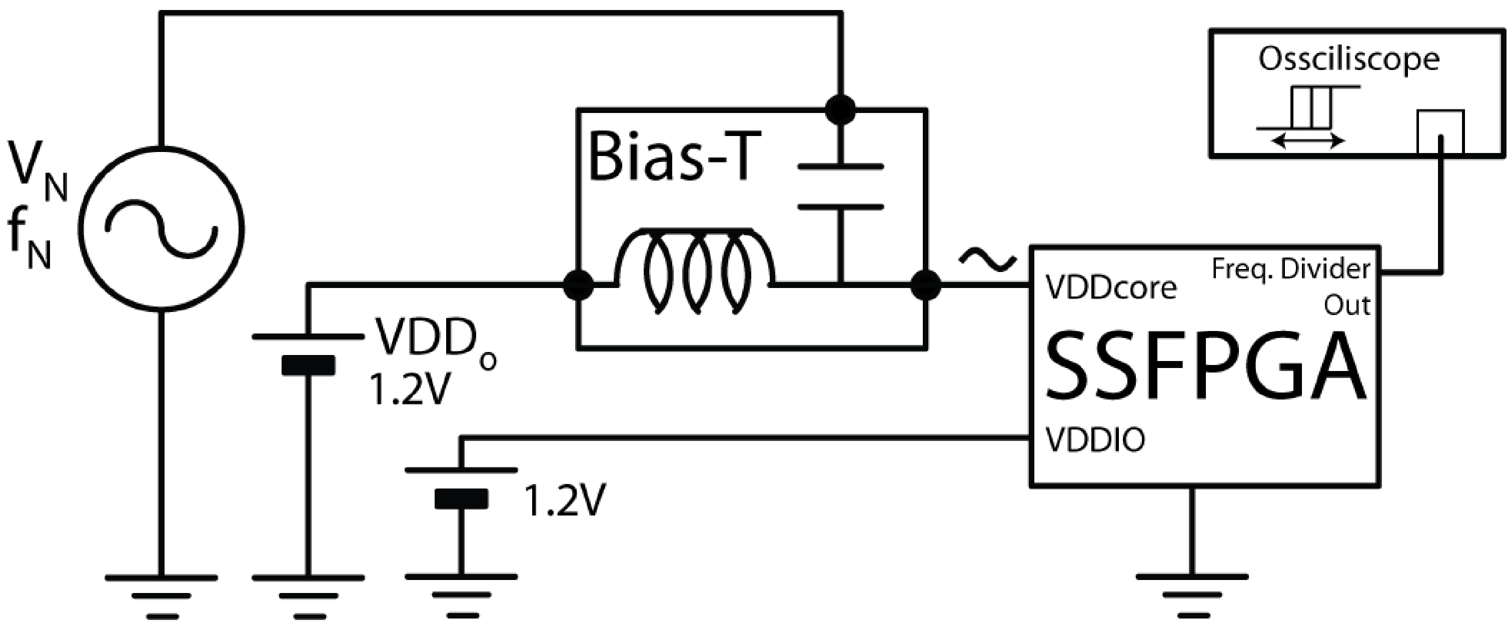
65nm Throughput and Energy Results

- Correct operation from 1.6V to 0.37V
  - 7% area, 15% throughput and 16% energy overhead measured on a 16-NAND chain loop @ 25ºC (operation also confirmed 0ºC to 120ºC)
  - 2.4GHz pipeline to pipeline operation @ 1.2V



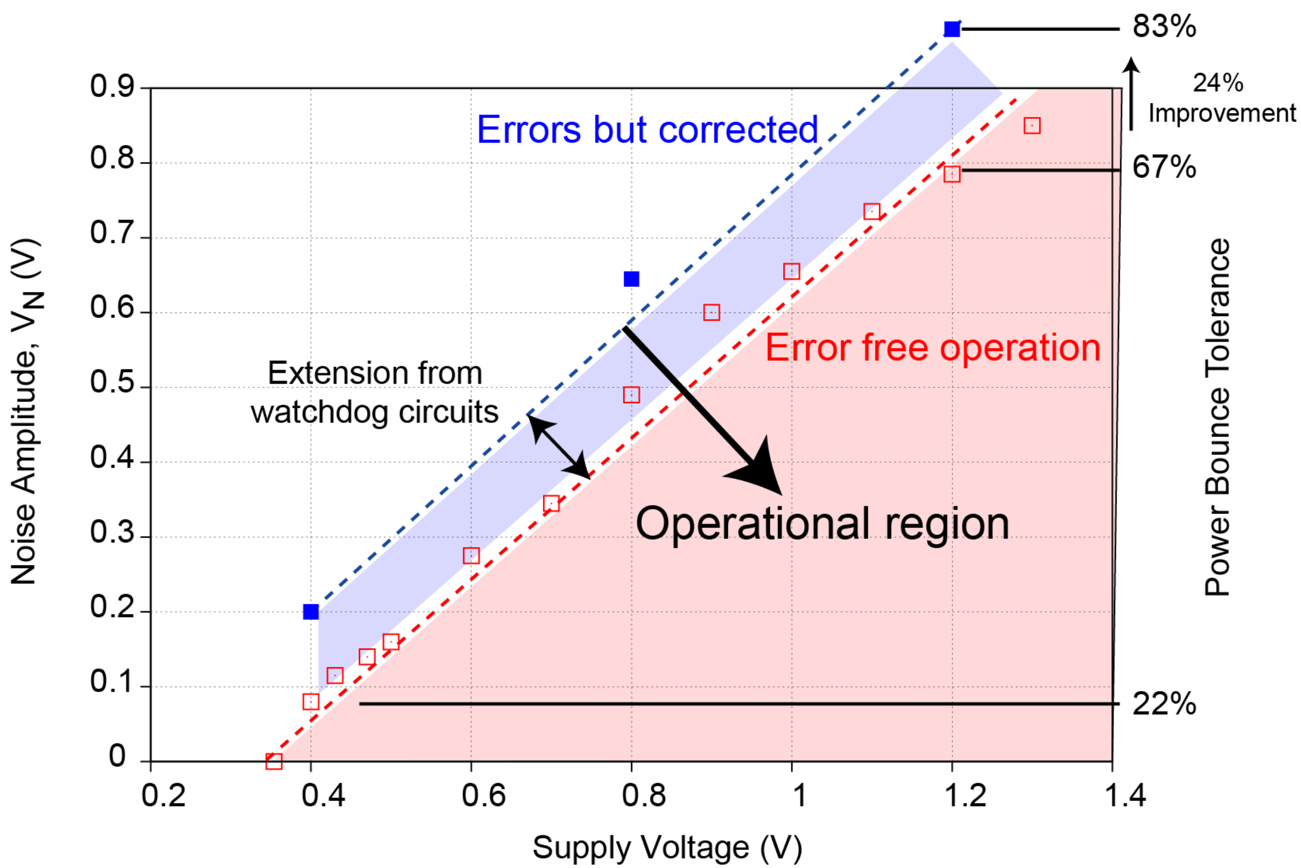
External Noise Injection

- Inject sine wave noise with varying amplitude and frequency, and measure resulting errors



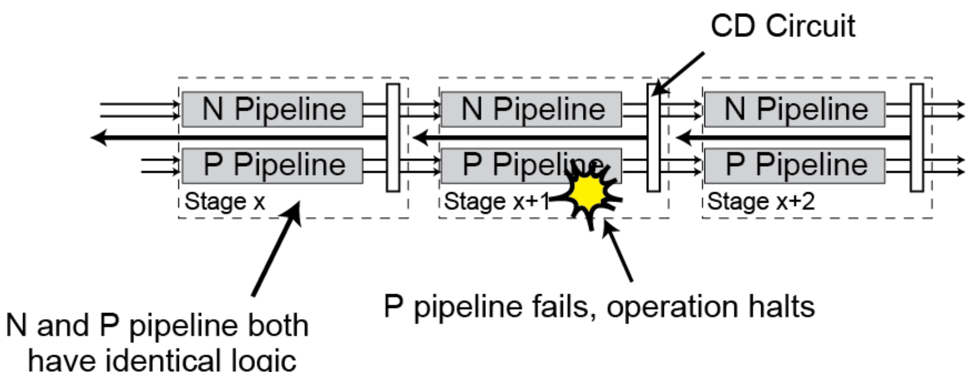
65nm Robustness Comparison to Base SSFPGA

- 16-NAND circuit loop at maximum throughput @ 25ºC
- 500MHz sine-wave noise
- 24% improvement over base-SSFPGA @1.2V

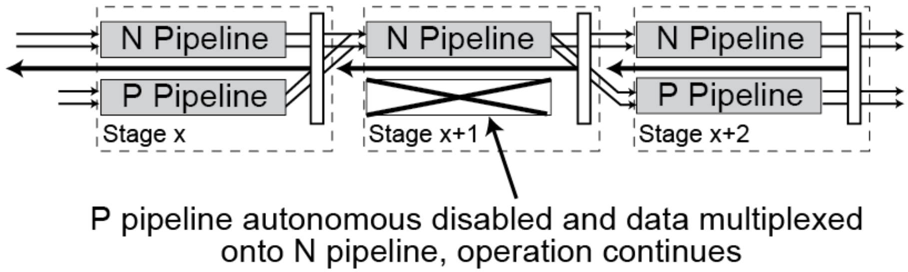


Pipeline disabling

- Autonomous disabling of a faulty pipeline
  - For example if watchdog error counter > x
  - Seamless operation with throughput decrease



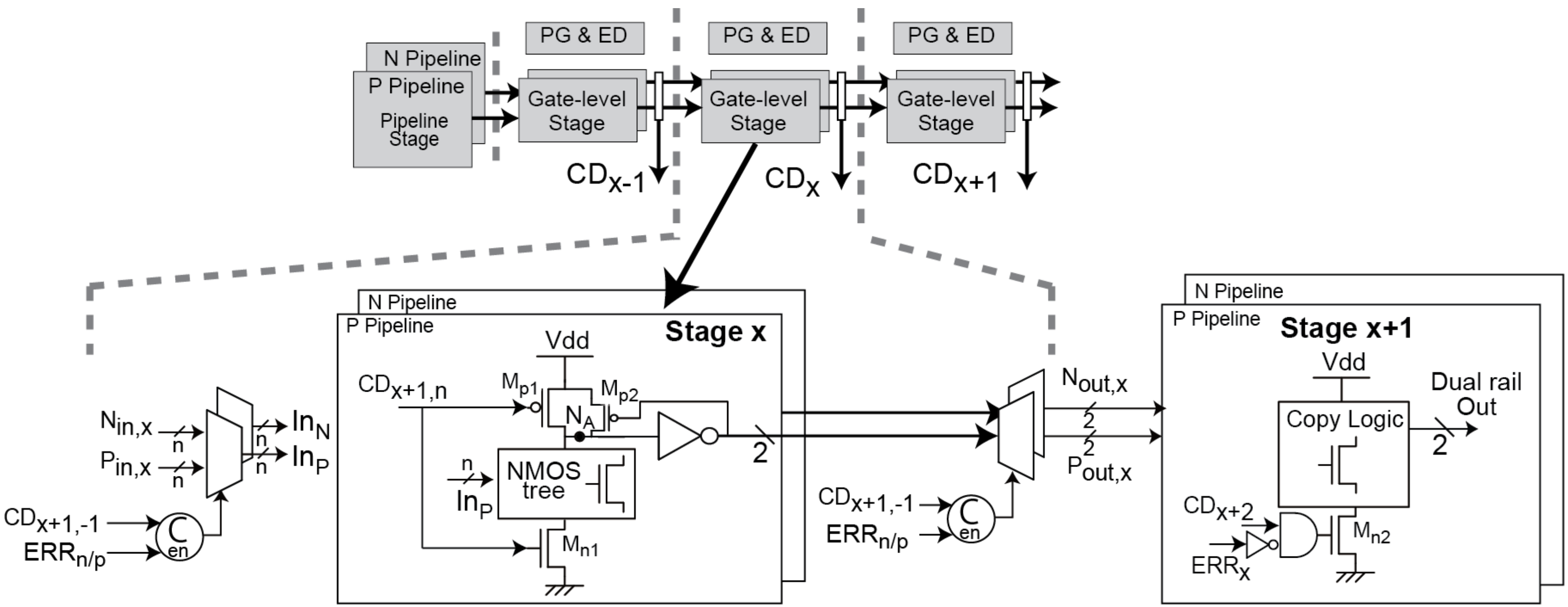
(a) Conventional method



(b) Proposed method

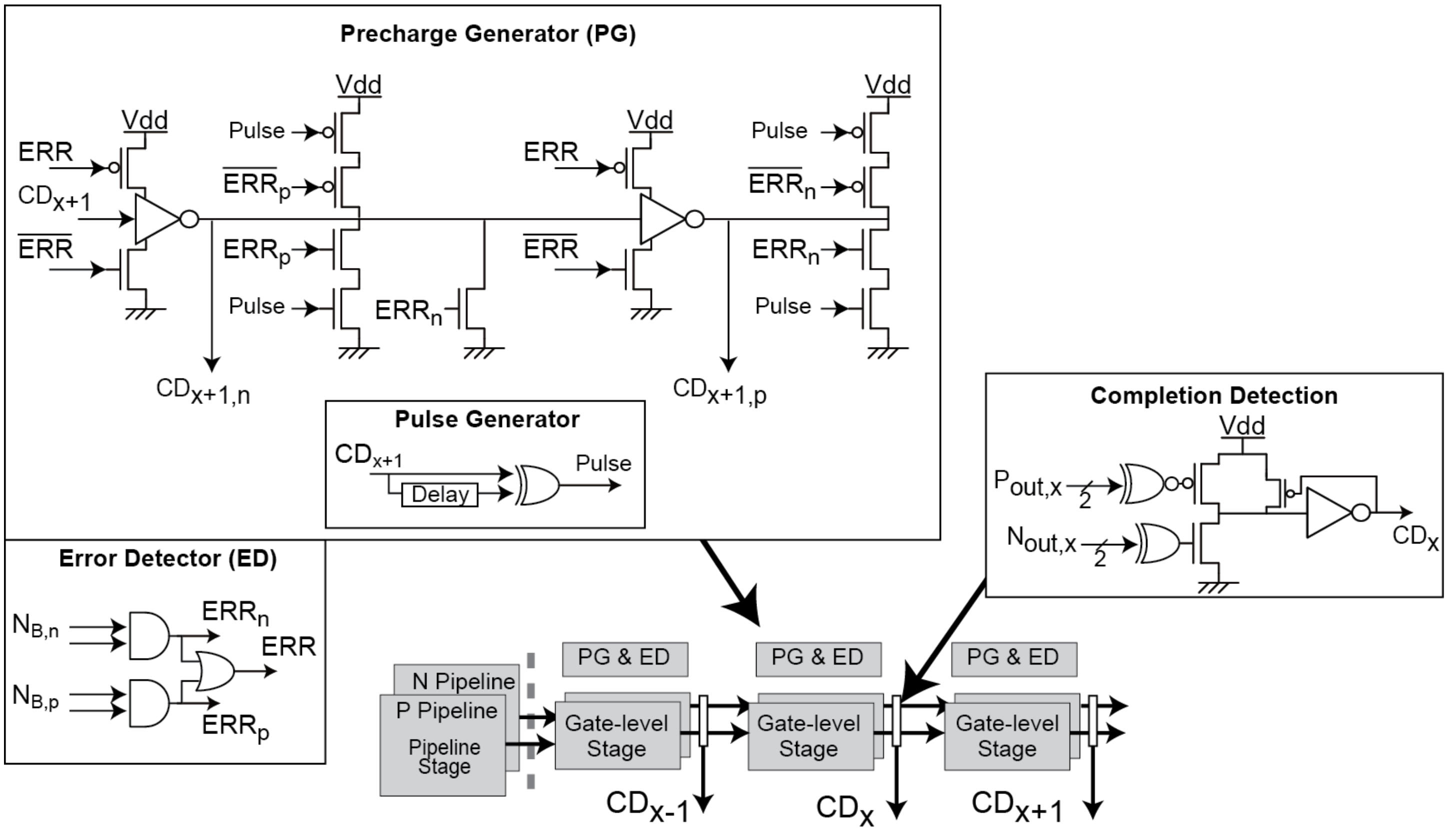
Disabling Circuits

- Add a Precharge Generator (PG), Error Detector (ED), multiplexors to each stage
- Logic in stage x+1 to stop error propagation



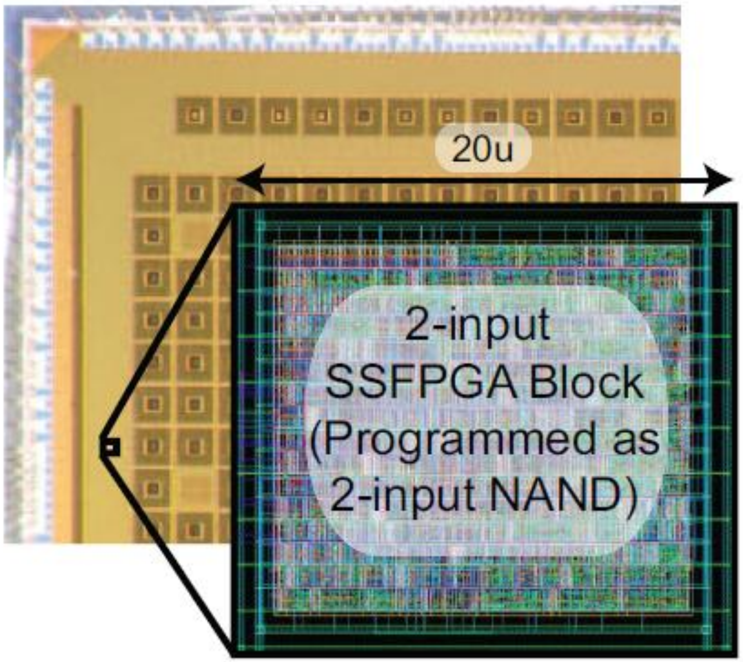
Disabling Circuits

- Pulse generator generates precharge when error occurs



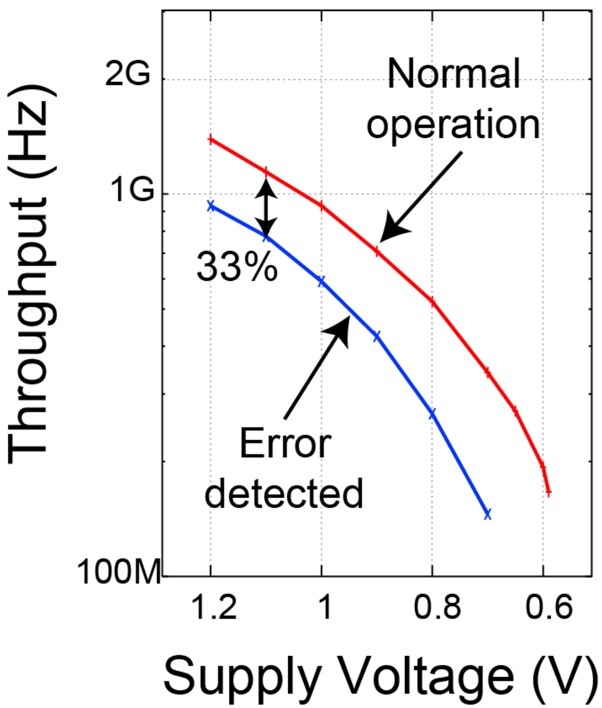
40nm Fabricated Chip

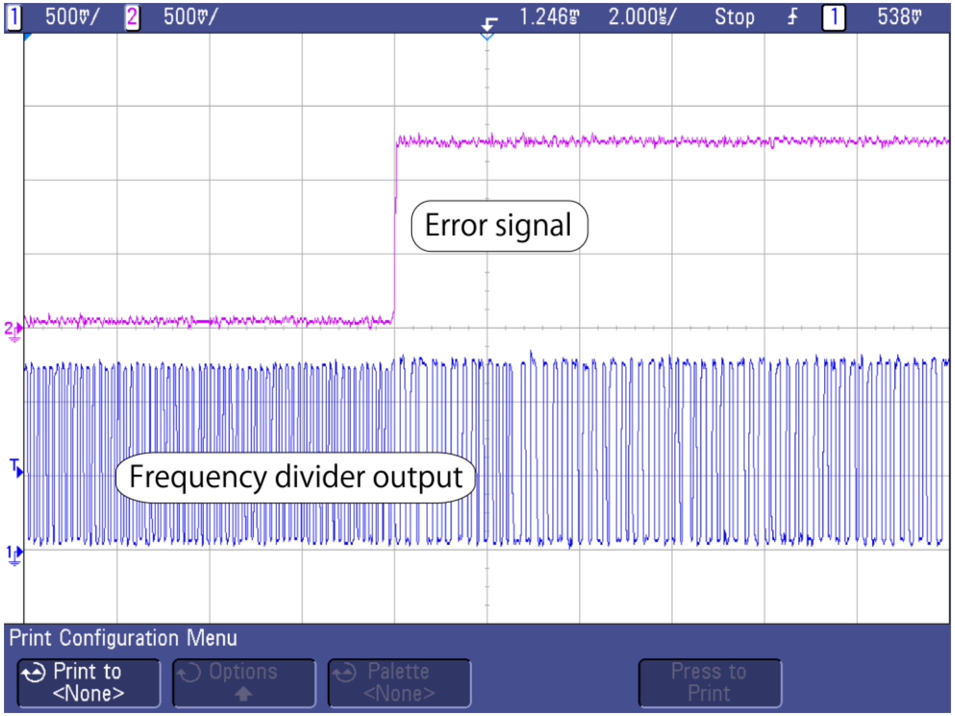
- 20u x 20u 40nm 7ML CMOS
- 2-input LUT 2x2 channel SSFPGA block
- Internal frequency divider
- Design standard cells, automatic place and route flow



Measured Results

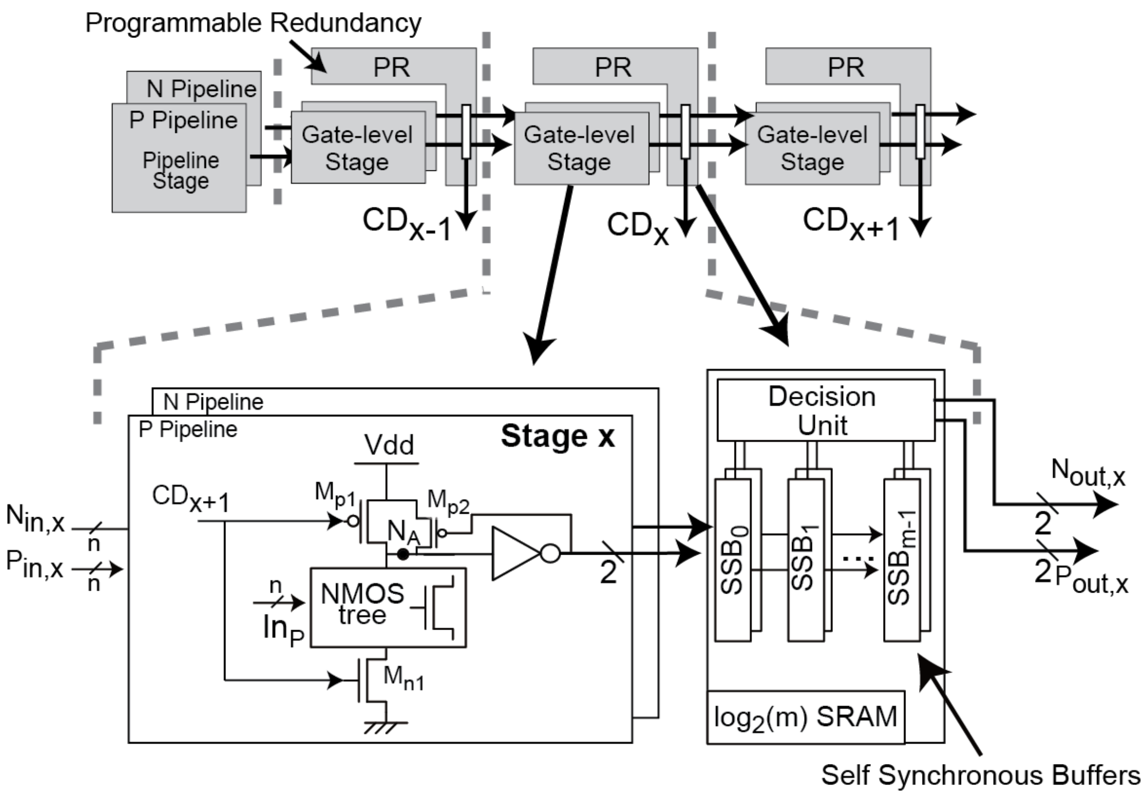
- Correct operation from 1.2V to 0.7V
  - 33% overhead when pipeline is disabled by using internal circuit to simulate error
  - 1.2GHz @ 1.1V





Time-interleaved Programmable Redundancy

- Can correct for incorrect “01” or “10” error by trading off throughput for robustness
- PR can be built from m-input LUT



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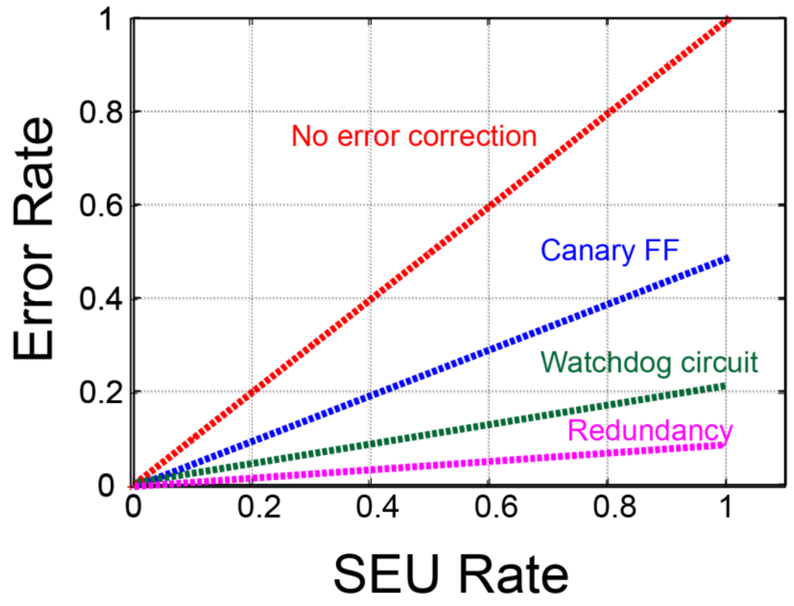
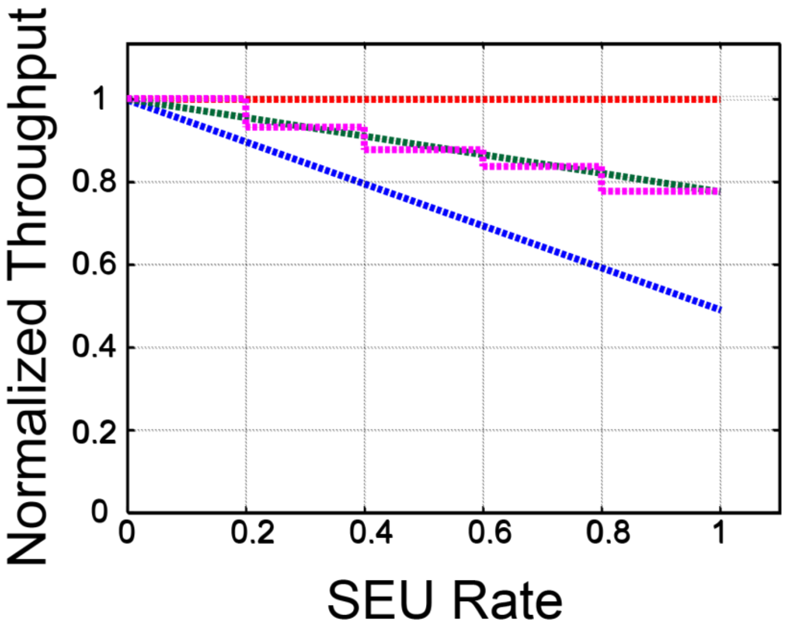
SEU Analysis of Synchronous Circuits

- Monte-carlo SEU simulations performed
  - 10,000 simulations, SEU rate is SEU per time cycle
  - 40% error rate improvement over canary FF using watchdog circuit
  - 50% error rate improvement with programmable redundancy





Conclusions

- Investigation of "self checking" behavior of dual pipeline self synchronous circuits and proposed circuits for complete coverage
- Fabrication in 65nm and 40nm shows operational circuits
  - 2.4GHz operation @ 1.2V in 65nm
  - Seamless operation to 370mV, 83% power bounce tolerance @ 1.2V in 65nm
  - Correctly detect and disable faulty pipelines in 40nm
- Robust techniques are also evaluated with SEU simulations
  - Up to 50% improvement over canary FF approach
- **This research shows Self Synchronous Circuits can offer High Performance Reliable Operation in nano-meter node processes for future VLSI systems**

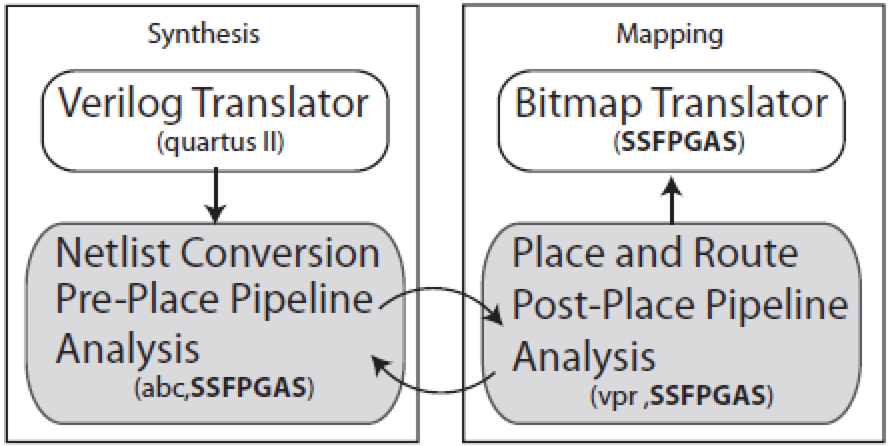
This research was performed by the author for STARC as part of the Japanese Ministry of Economy, Trade and Industry sponsored "Next-Generation Circuit Architecture Technical Development " program.

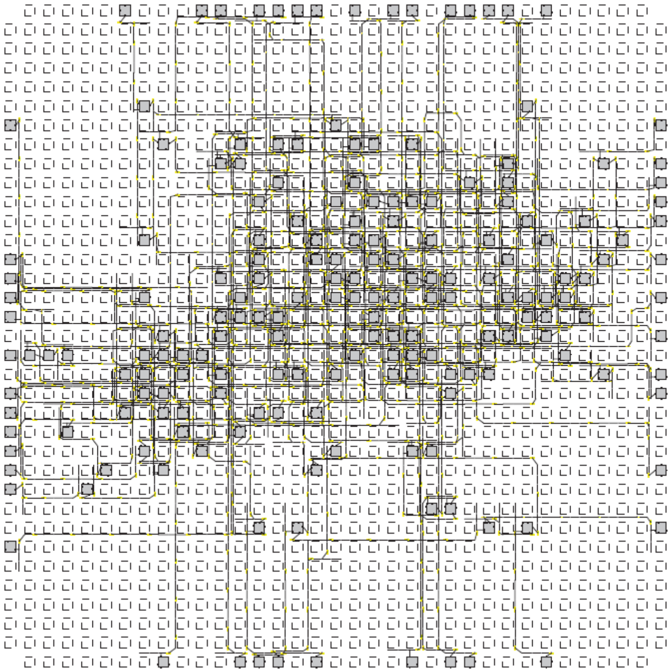
The VLSI chips in this study have been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

Appendix

Programming Flow

- Quartus to convert verilog to LUT blocks
- ABC [1] and SSFPGAS to convert to 4-input LUTs, pipeline alignment, fanout modification
- Modified VPR [2] for place and route with pipeline alignment aware routing
- Bitmap translator

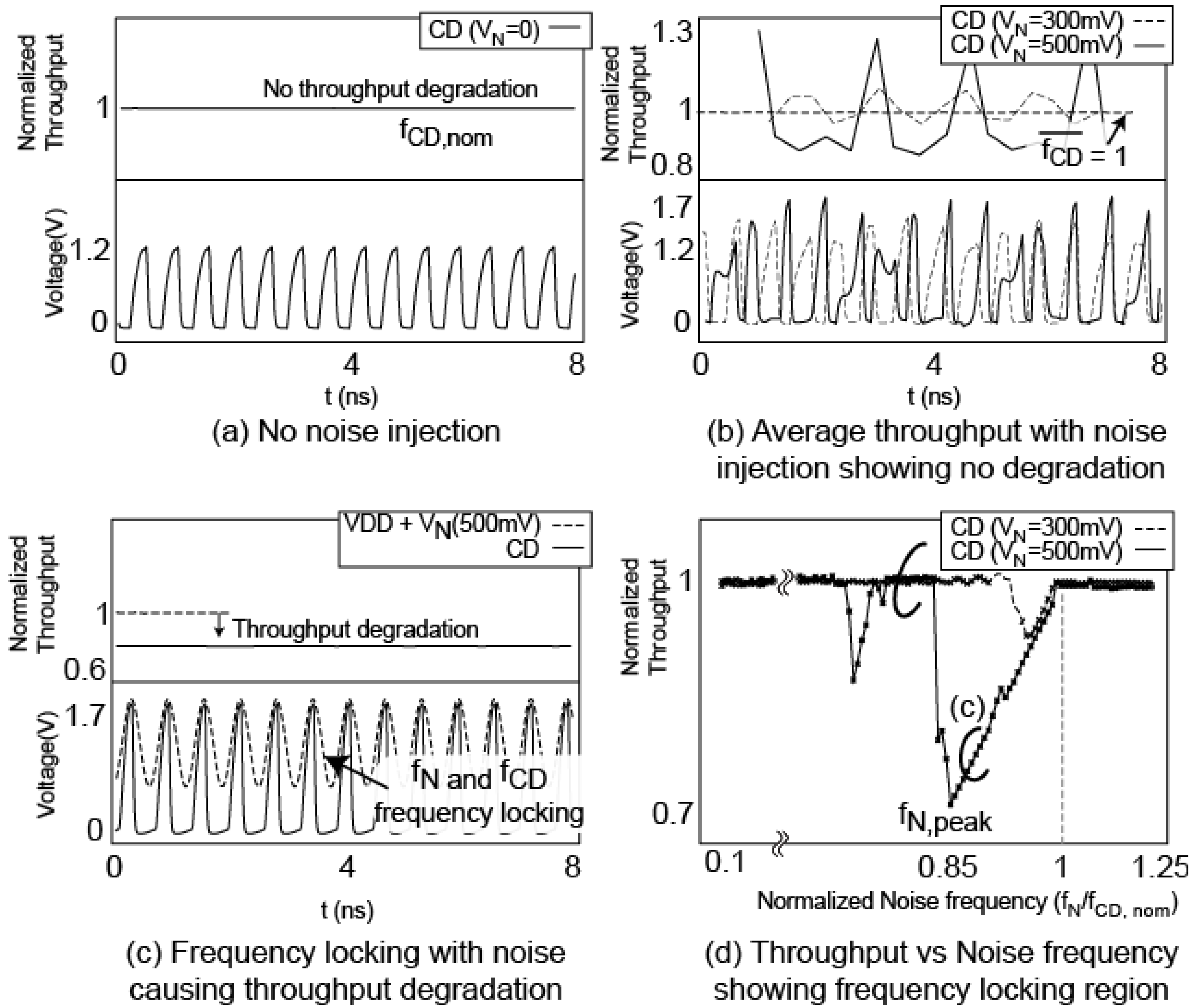




[1] ABC: A System for Sequential Synthesis and Verification, http://www.eecs.berkeley.edu/~alanmi/abc/
[2] VPR: Versatile Place and Route, http://www.eecg.toronto.edu/vpr/

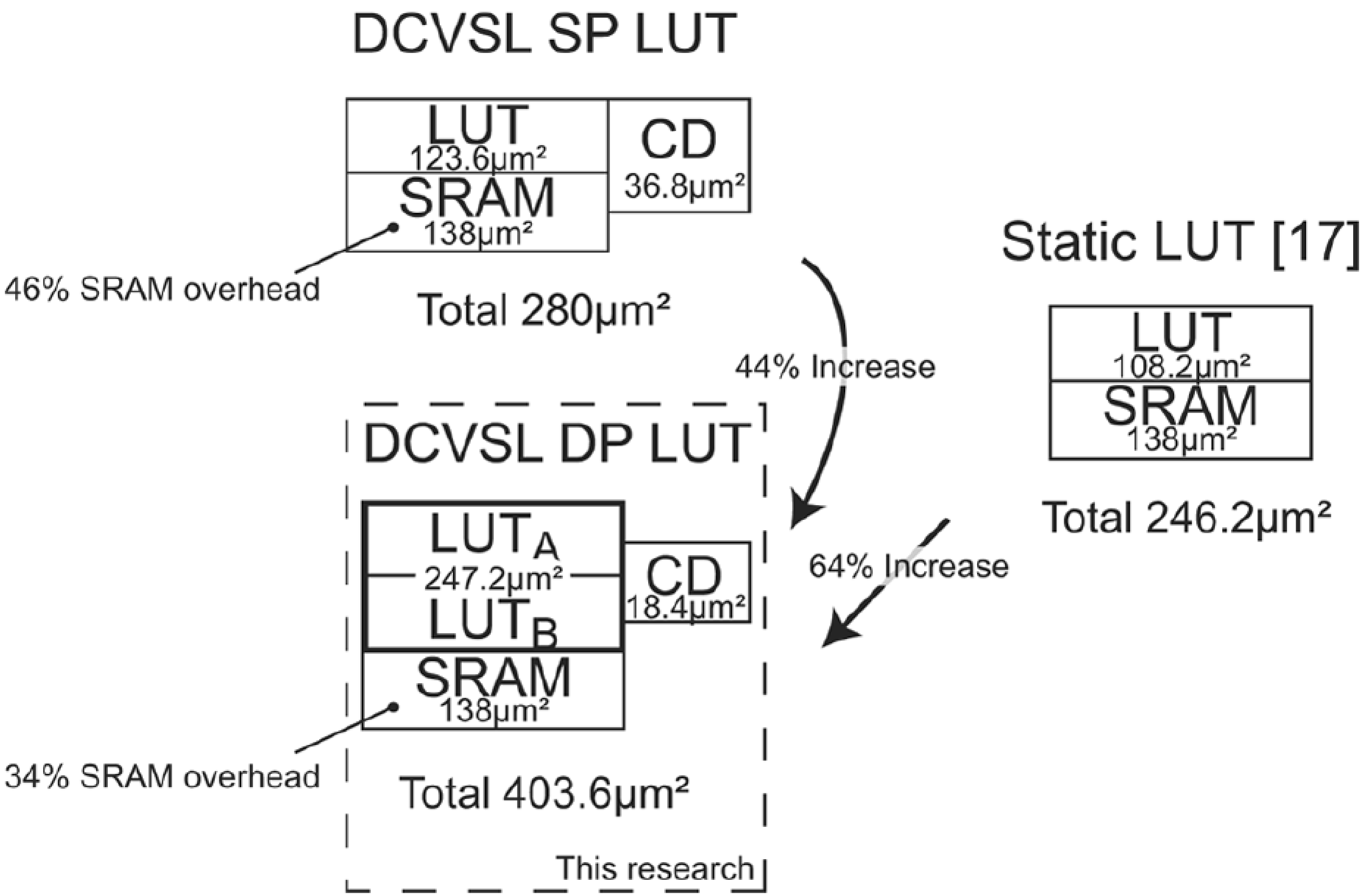
Noise Robustness

- Frequency locking is responsible for throughput degradation



Note on Area Overhead

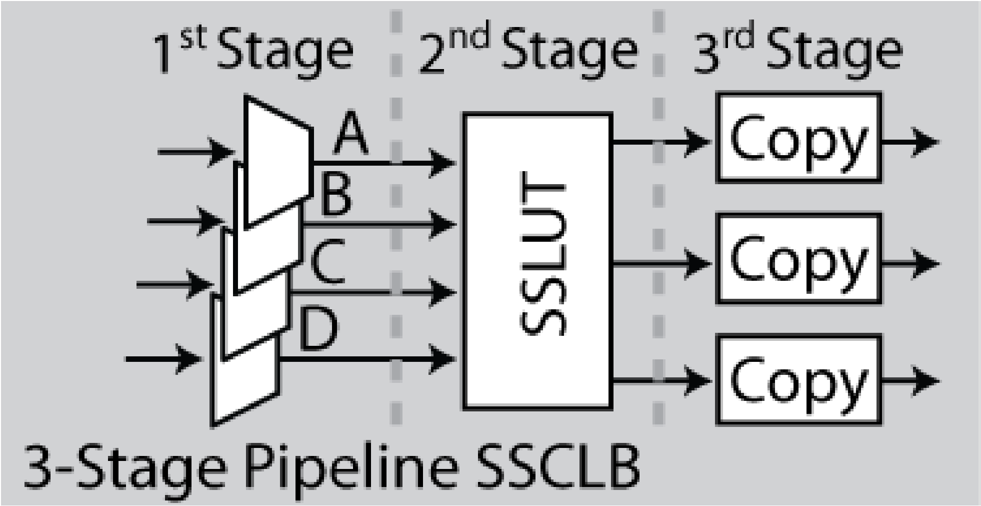
- Area overhead is 44% compared to a single pipeline 4-input LUT



[17] E. Ahmed and J. Rose "The effect of LUT and cluster size on deep-submicron FPGA performance and density", Trans. VLSI 2004

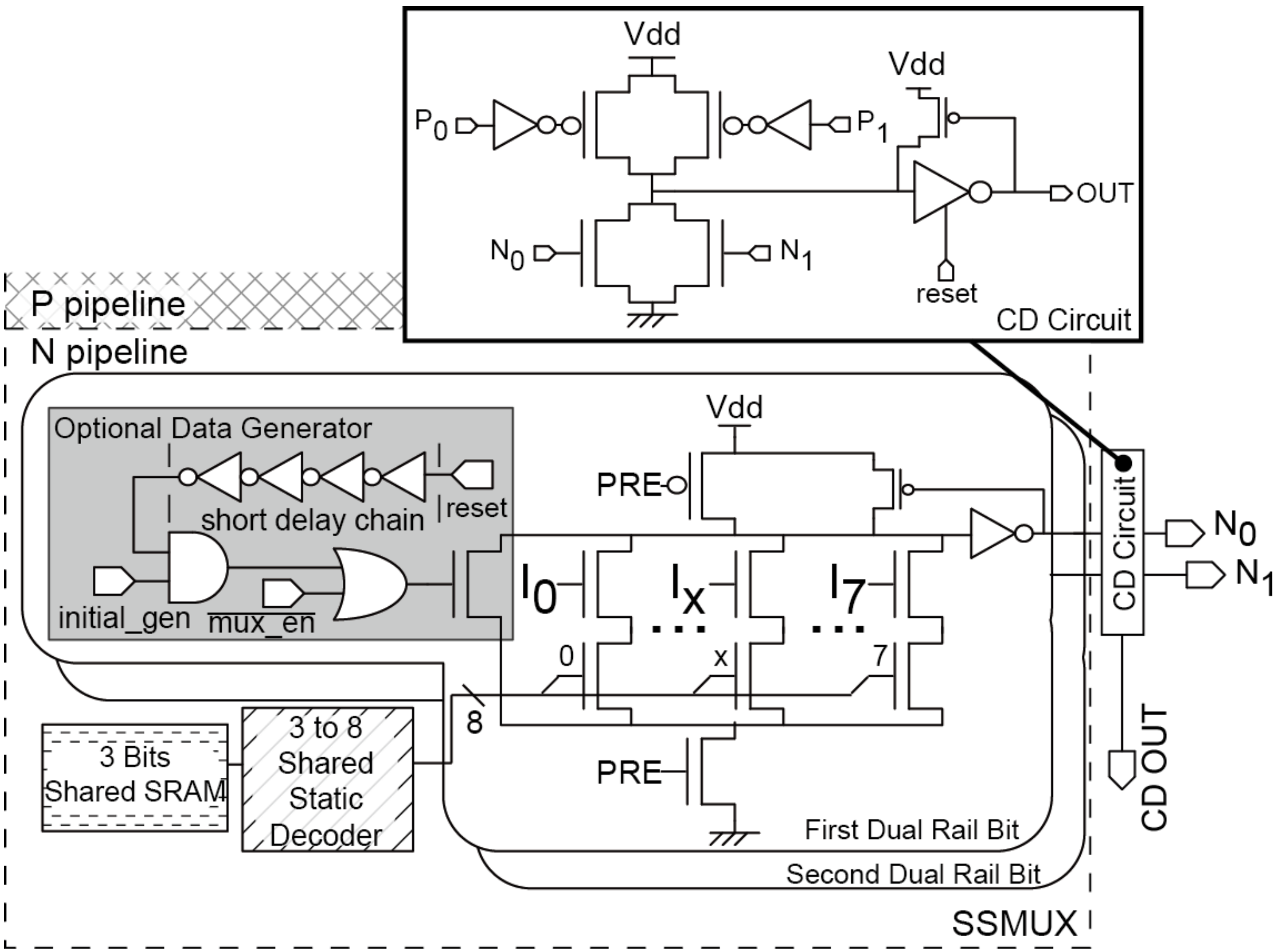
SSFPGA Configurable Logic Block

- SSCLB is composed of 3 gate level pipeline stages
  - 4 Input Self Synchronous Mux (SSMUX) and 3 output copy locations
- Pipeline stages eliminate timing overhead from Self Synchronous operation



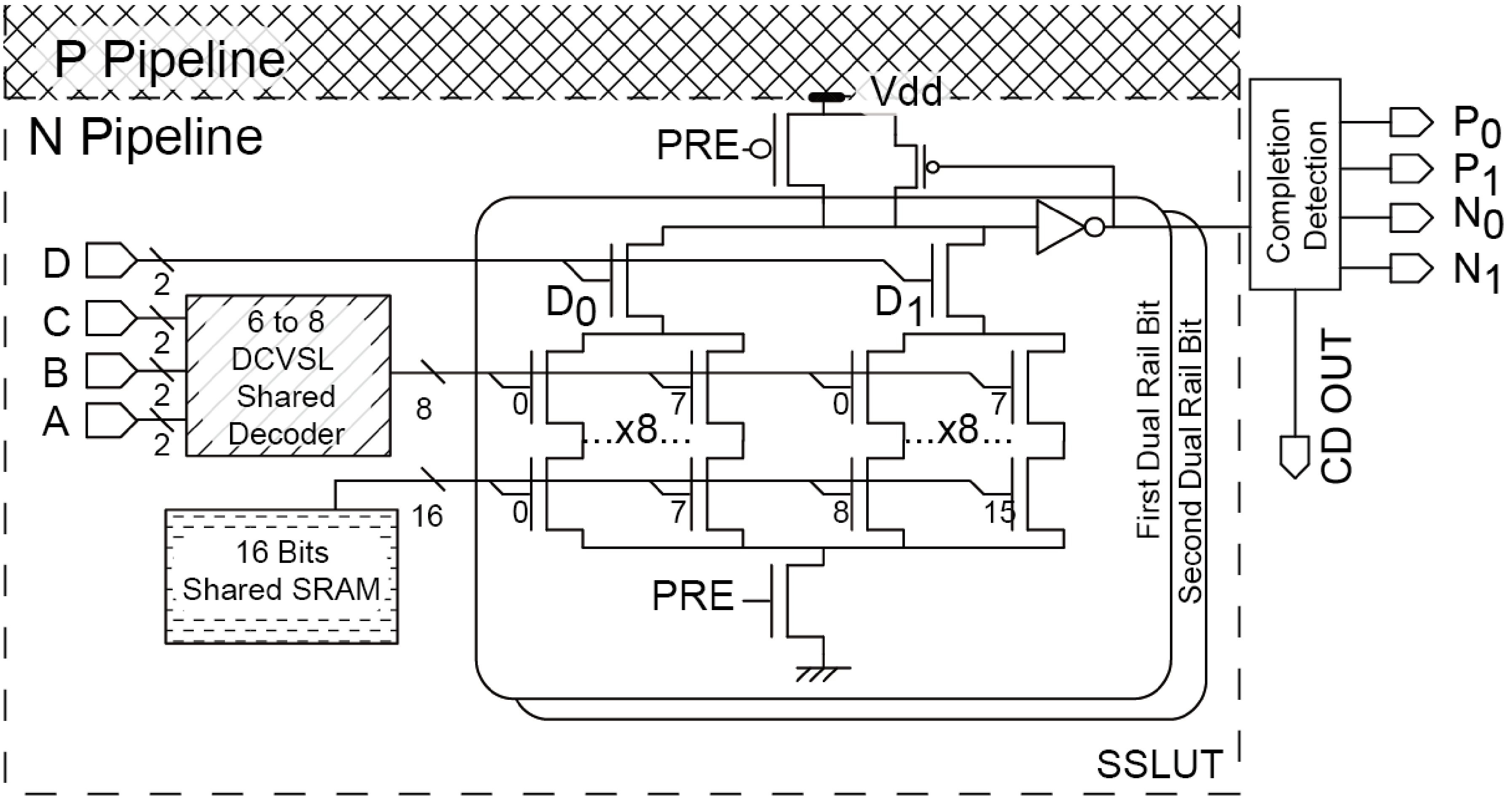
SSMUX and Completion Detection

- Gate-level pipeline stage and programmable MUX combined
- Because of 2 phase CD, the CD overhead is very small



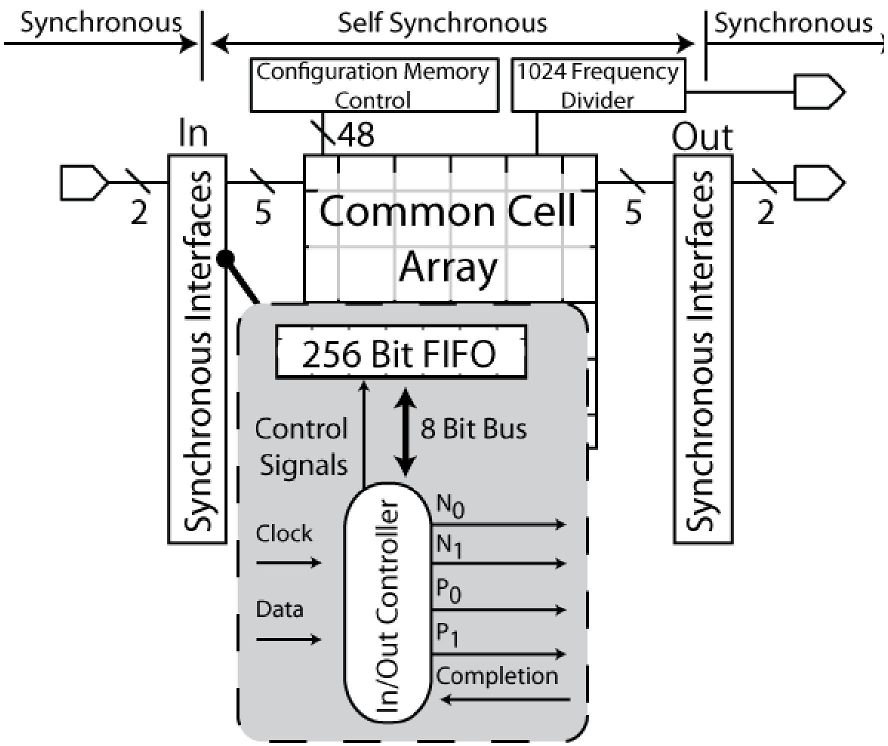
Self Synchronous LUT

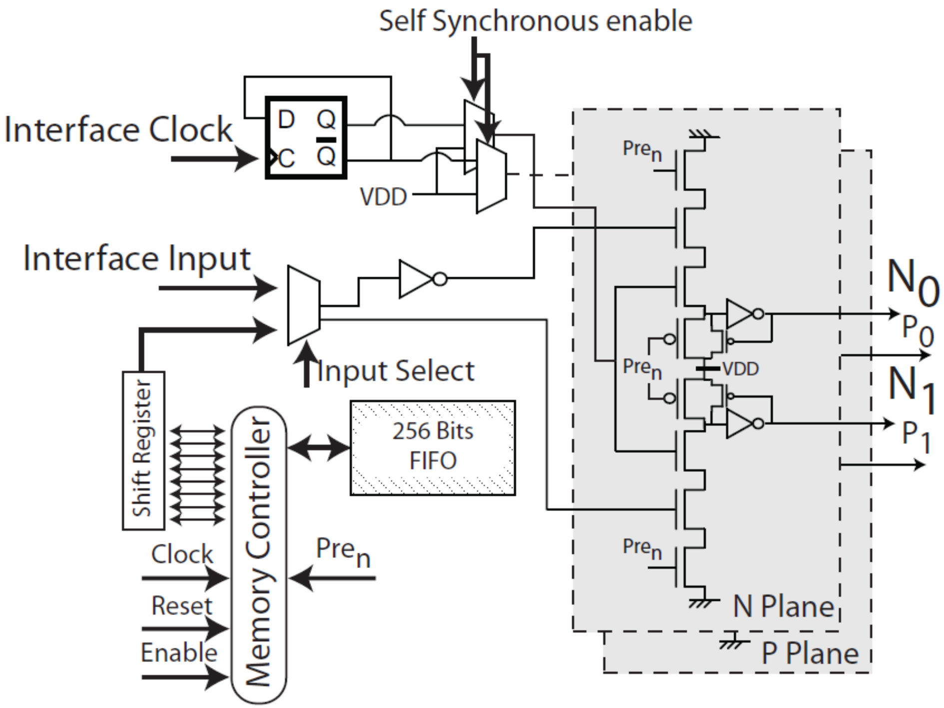
- 4 input LUT, split into decoder-tree architecture



Interfaces

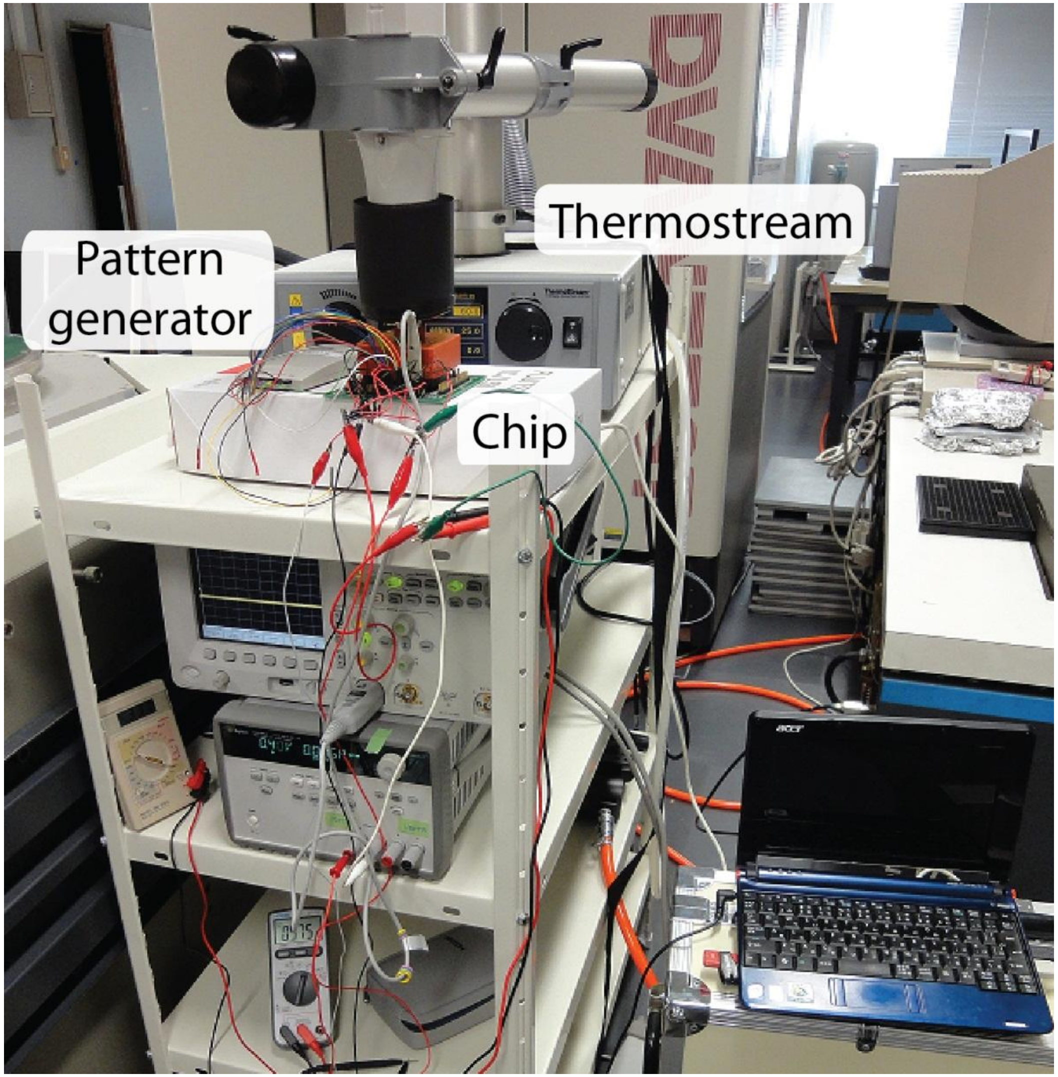
- Synchronous interfaces are used on core boundaries
- 256 bit FIFO to maximize use of high speed SSFPGA



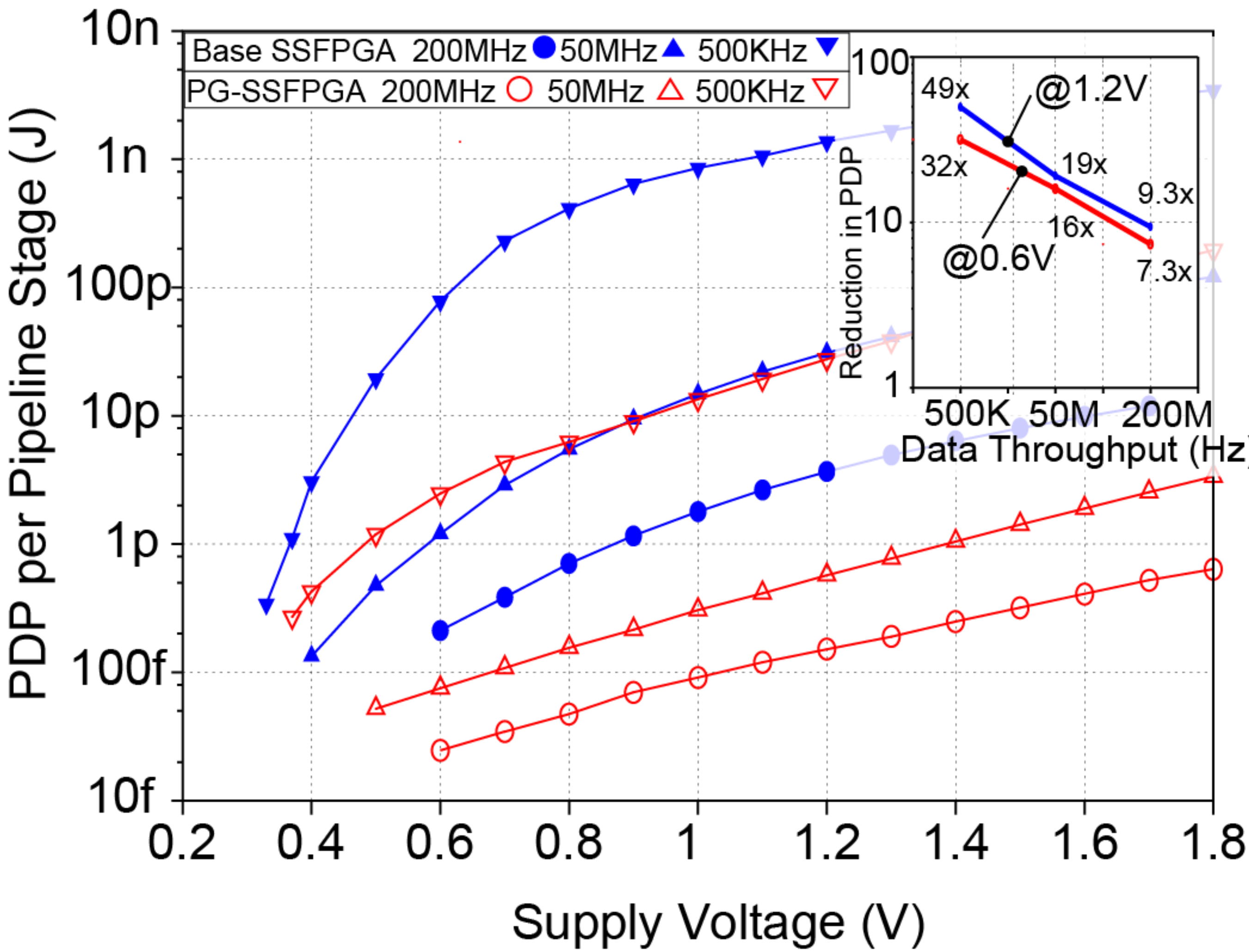


Measurement Setup

- Target circuit is converted into bit-stream by SSFPGA software tool chain
- Bit-steam written into SSFPGA SRAM memory by pattern generator
- Thermostream keeps constant temperature
- Frequency divider output used to measure throughput



Lower data rates



Near-threshold Operation

- Near-threshold operation is attractive to reduce static and dynamic power
  - But delay variation increases with near-threshold operation [1]

$$\tau_{PD} = \frac{C_L}{I_{DS}} \cdot \frac{V_{DD}}{2}$$

$$\left(\frac{\sigma_{I_{DS}}}{\mu_{I_{DS}}}\right)^2 \approx \left(\frac{\sigma_W}{\mu_W}\right)^2 + \left(\frac{\sigma_{V_{TH}}}{\mu_{V_{TH}}}\right)^2 \cdot \left(\frac{\mu_{V_{TH}}}{V_{DD} - \mu_{V_{TH}}}\right)^2$$

[1] Alioto, M.; Palumbo, G.; Pennisi, M.; , "Understanding the Effect of Process Variations on the Delay of Static and Domino Logic," JVLSI 2010.