DVFS Based on Voltage Dithering and Clock Scheduling for GALS Systems

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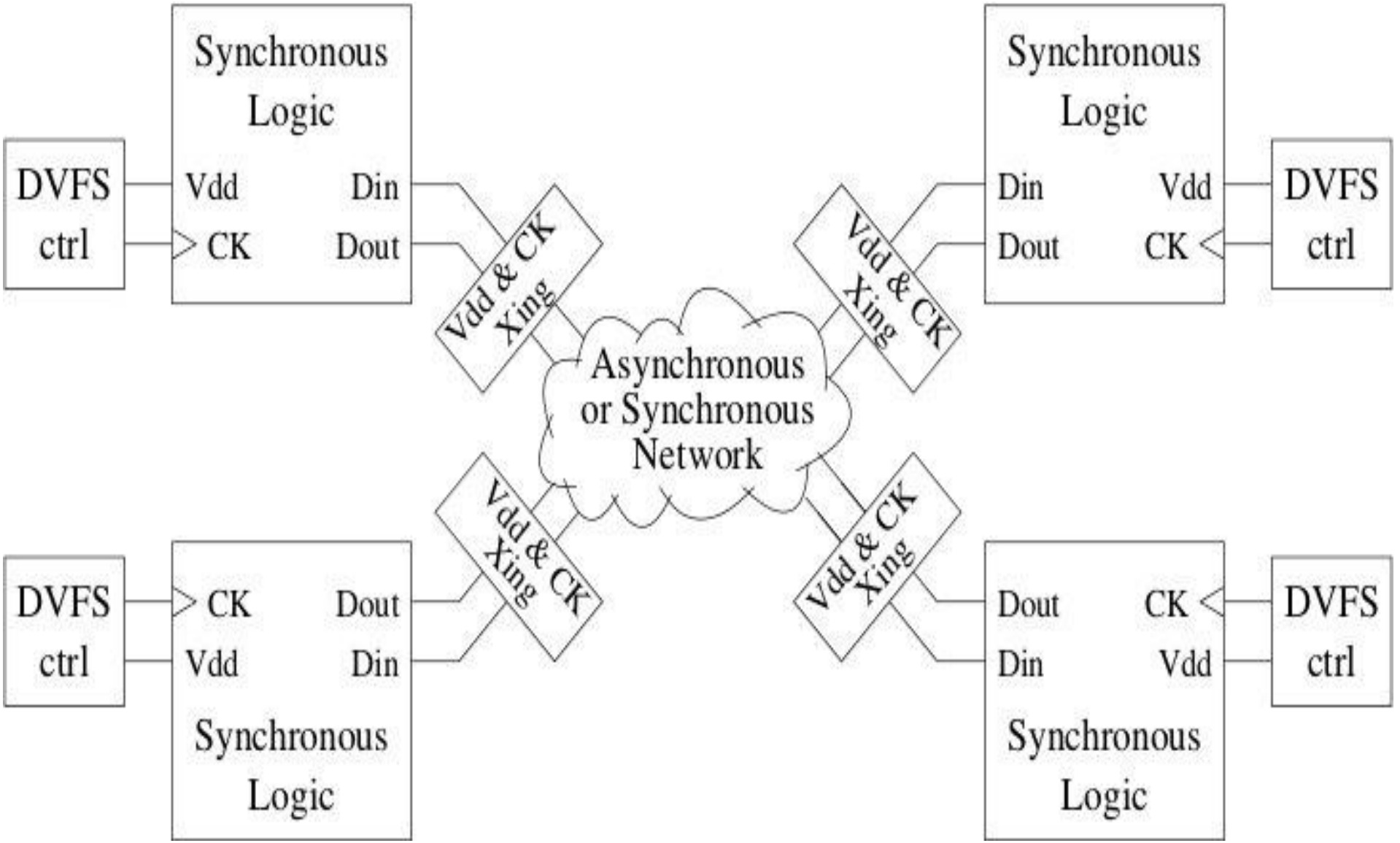
Outline

- Motivations
- Dynamic Voltage and Frequency Scaling
- Frequency Scaling using clock gating
- Simple pipeline and timing error
- DVFS using clock gating mechanisms
- Power performance of simple pipeline
- NoC switch and power performance
- Conclusions

Motivations

- DVFS is established technique for power optimization
- DVFS implementation requires bulky voltage regulators and complex PLLs or DLLs
- GALS Systems could entail tens or even hundreds of different domains, each requires its own DVFS unit

GALS system with per-block DVFS



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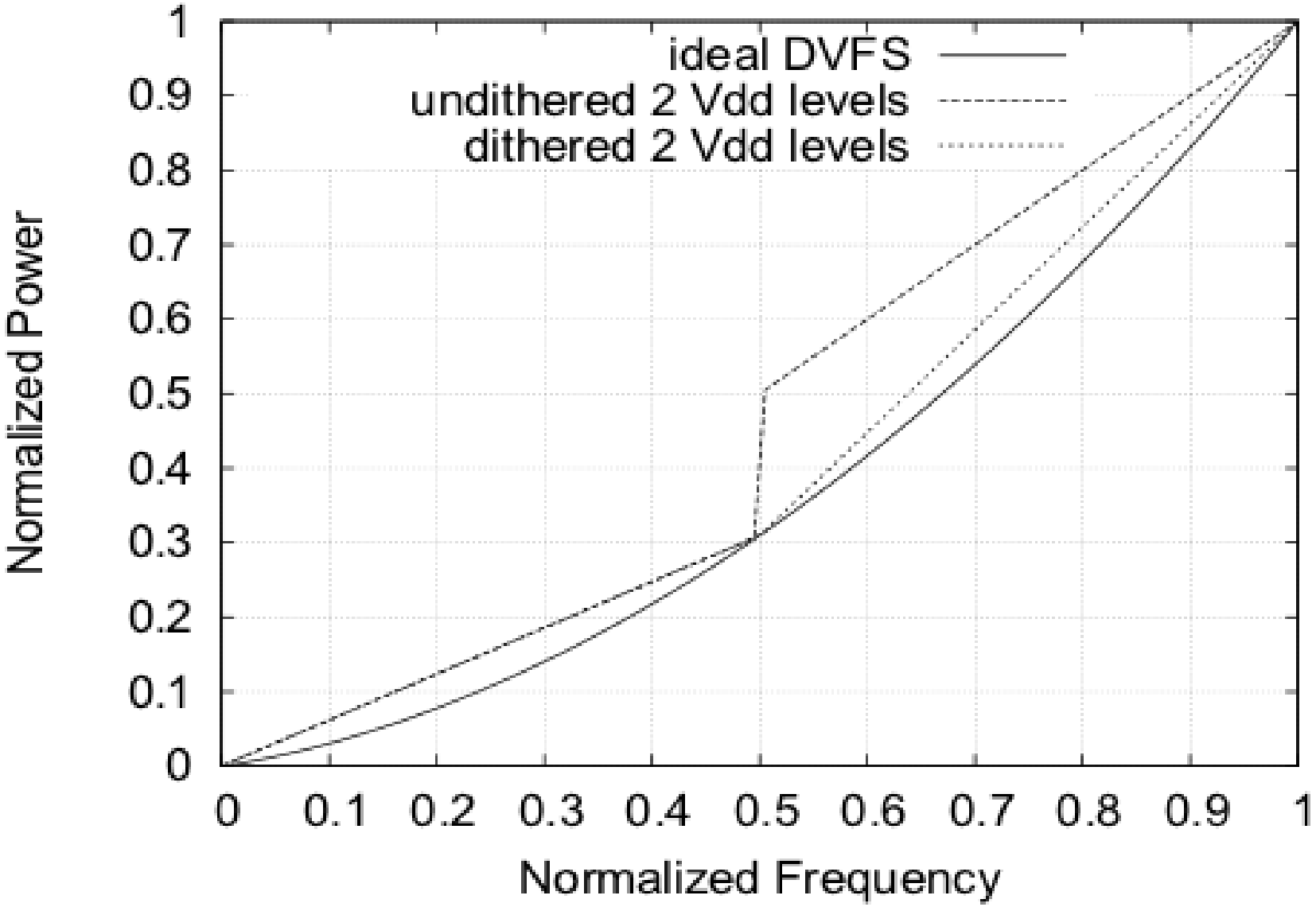
Dynamic Voltage and Frequency Scaling
[Chandrakasan 1997]



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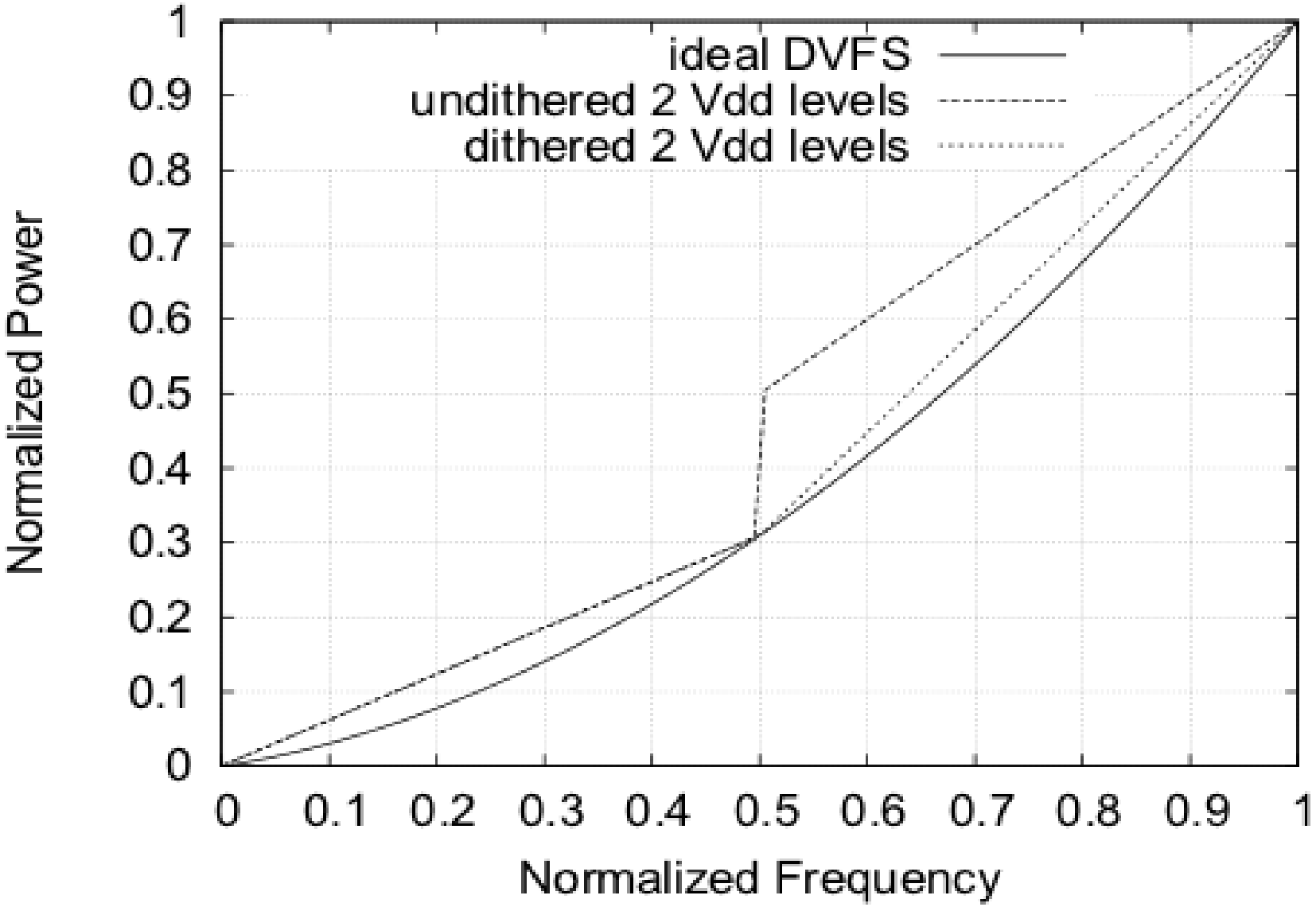

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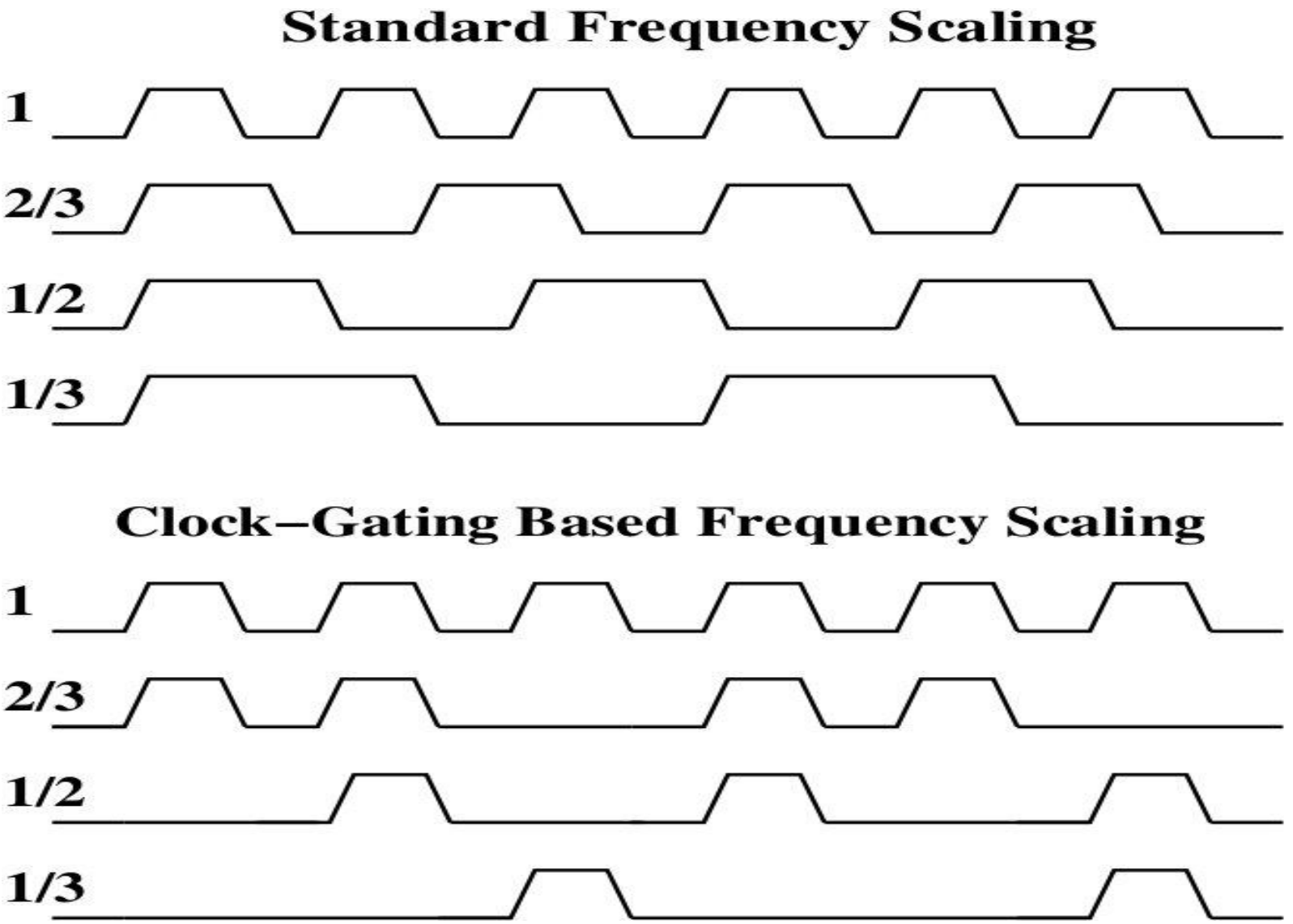
Frequency scaling using clock gating

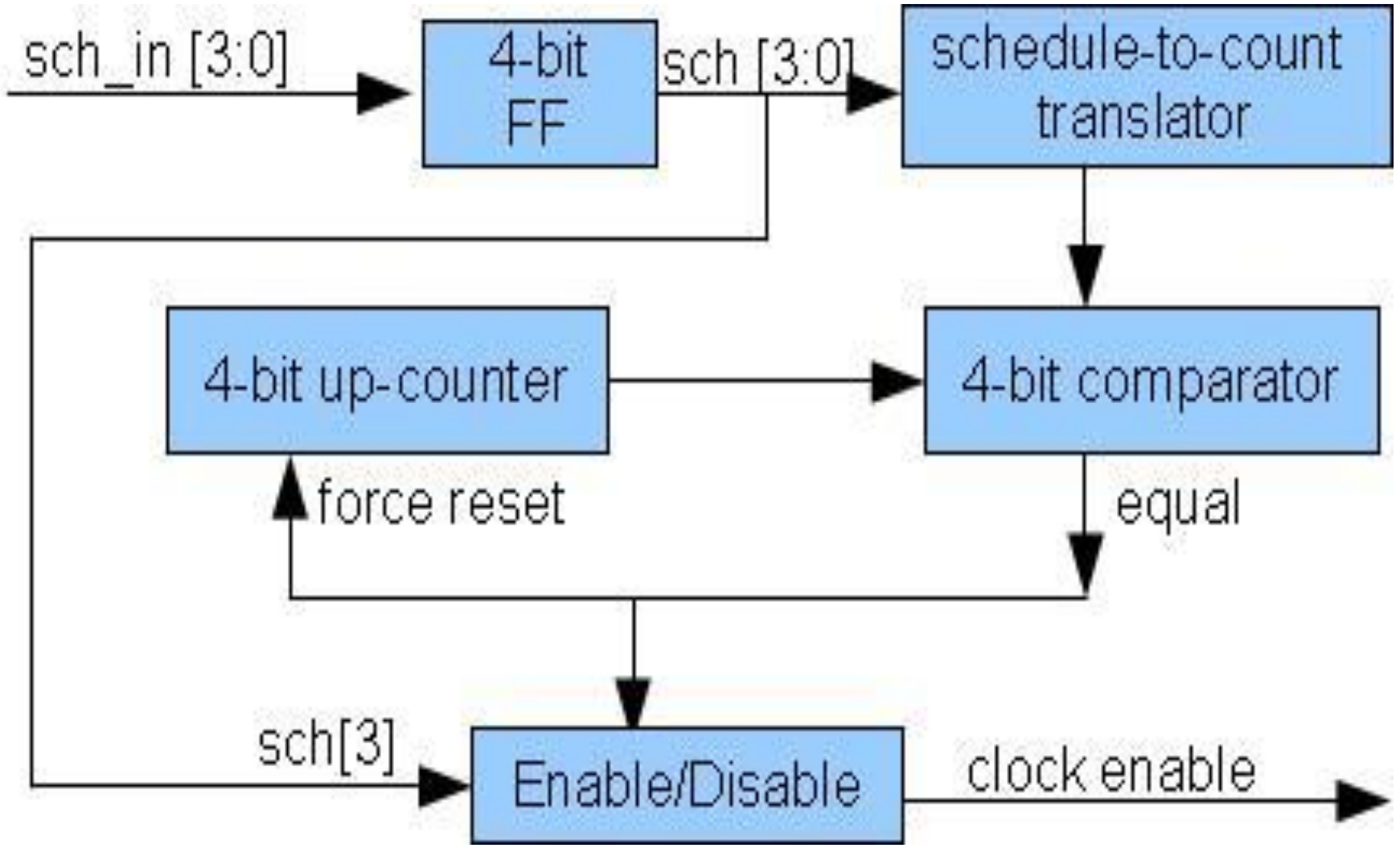


Scheduler

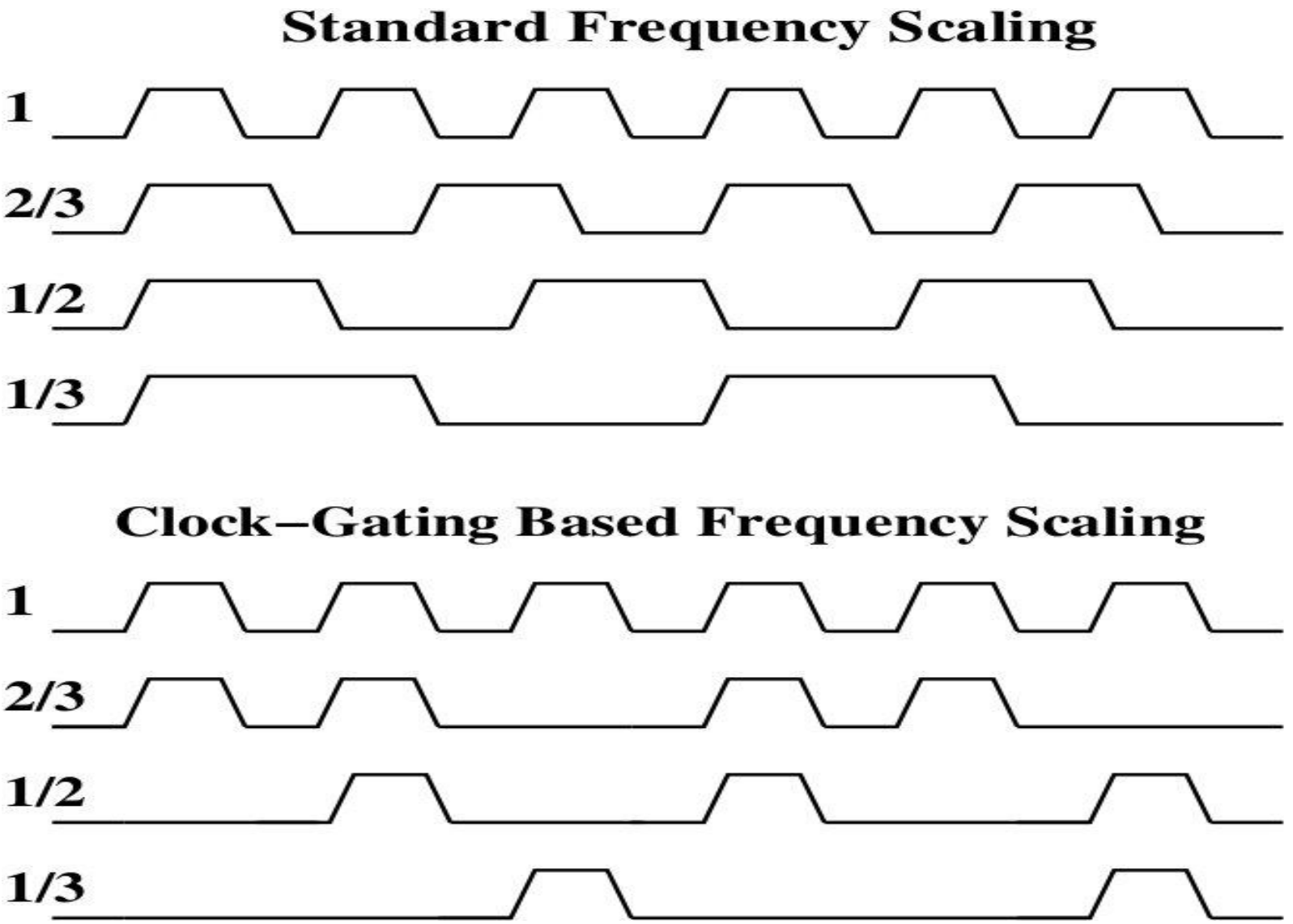
Schedule		Pulse /out of	Duty (%)
Decimal	Binary		
00	00 00	0	0.00
01	00 01	1/16	6.25
02	00 10	1/10	10.00
03	00 11	1/7	14.29
04	01 00	1/5	20.00
05	01 01	1/4	25.00
06	01 10	1/3	33.33
07	01 11	1/2	50.00

Schedule		Pulse /out of	Duty (%)
Decimal	Binary		
08	10 00	2/3	66.67
09	10 01	3/4	75.00
10	10 10	4/5	80.00
11	10 11	6/7	85.71
12	11 00	7/8	87.50
13	11 01	9/10	90.00
14	11 10	15/16	93.75
15	11 11	16/16	100.00

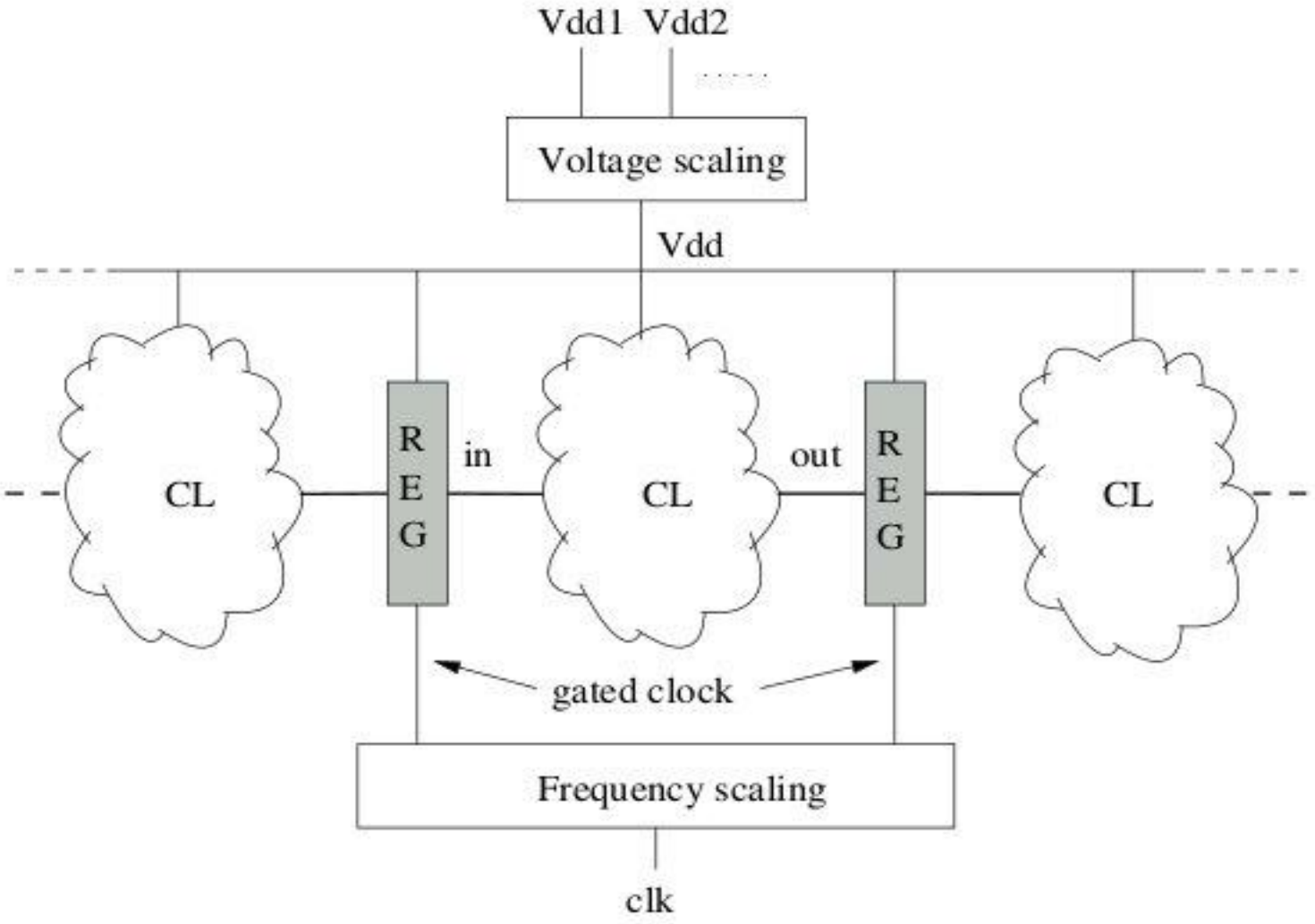
Scheduler


sch_in [3:0]
4-bit FF
sch [3:0]
schedule-to-count translator
4-bit up-counter
4-bit comparator
force reset
equal
sch[3]
Enable/Disable
clock enable

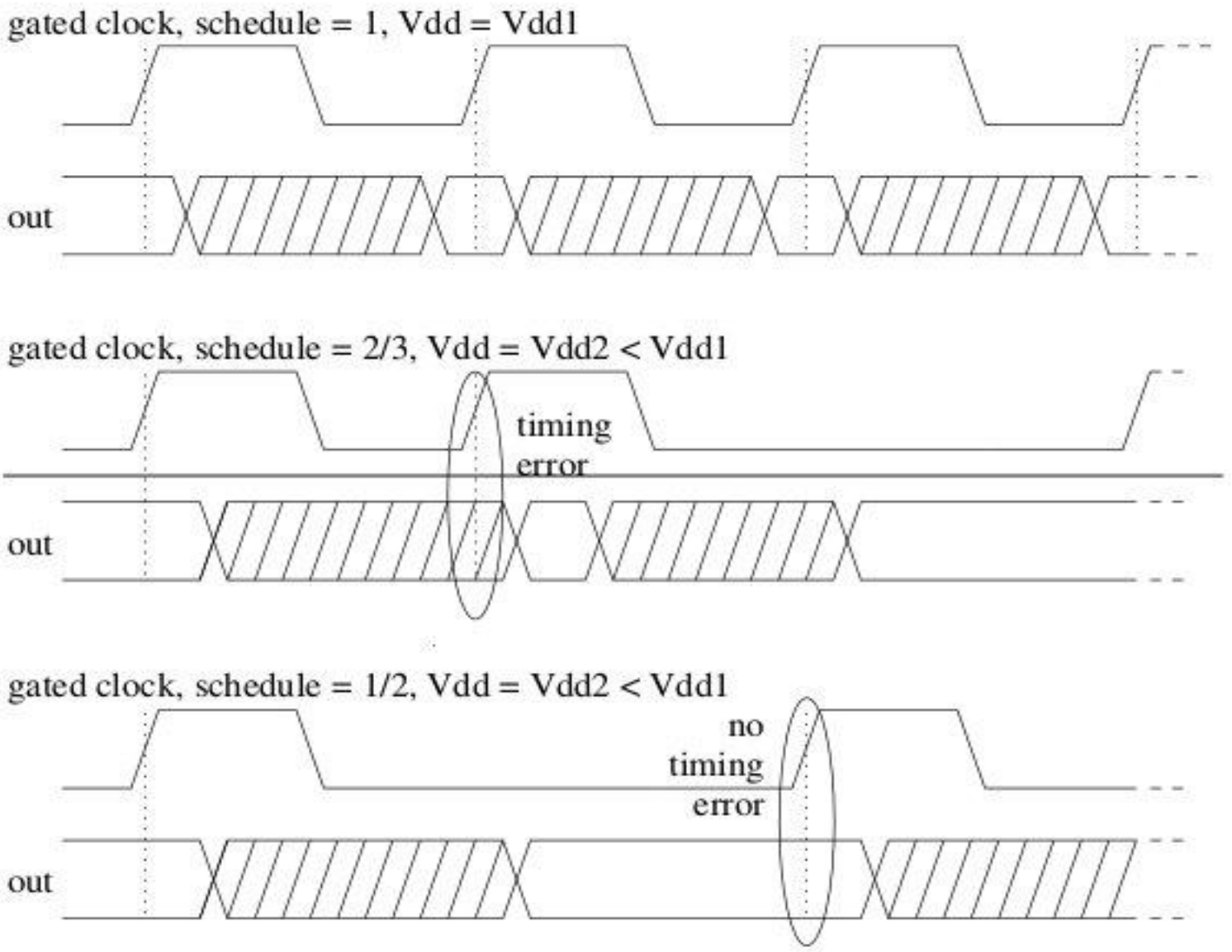
Frequency scaling using clock gating



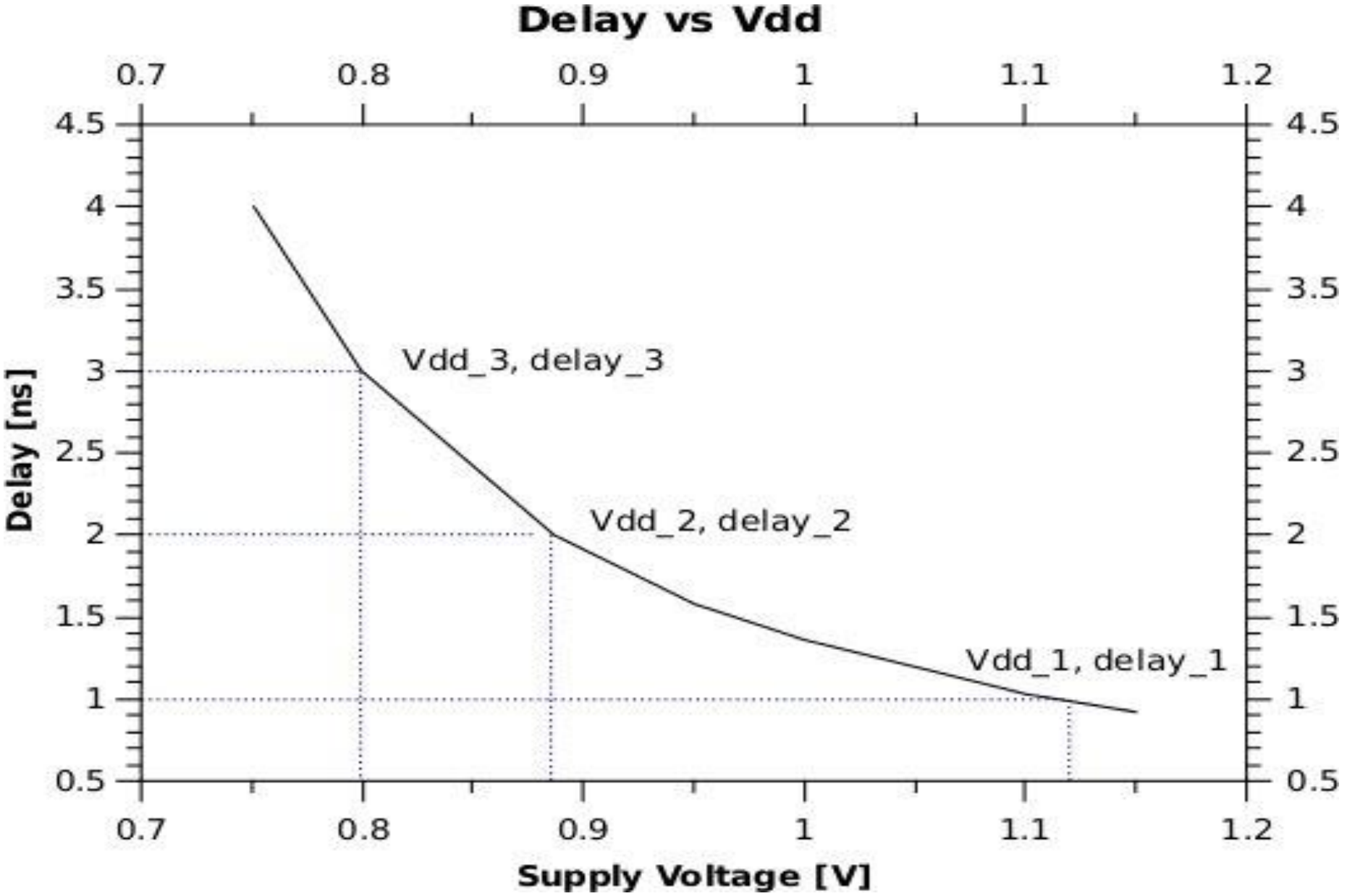
Simple pipeline and timing error



Simple pipeline and timing error



Simple pipeline and timing error



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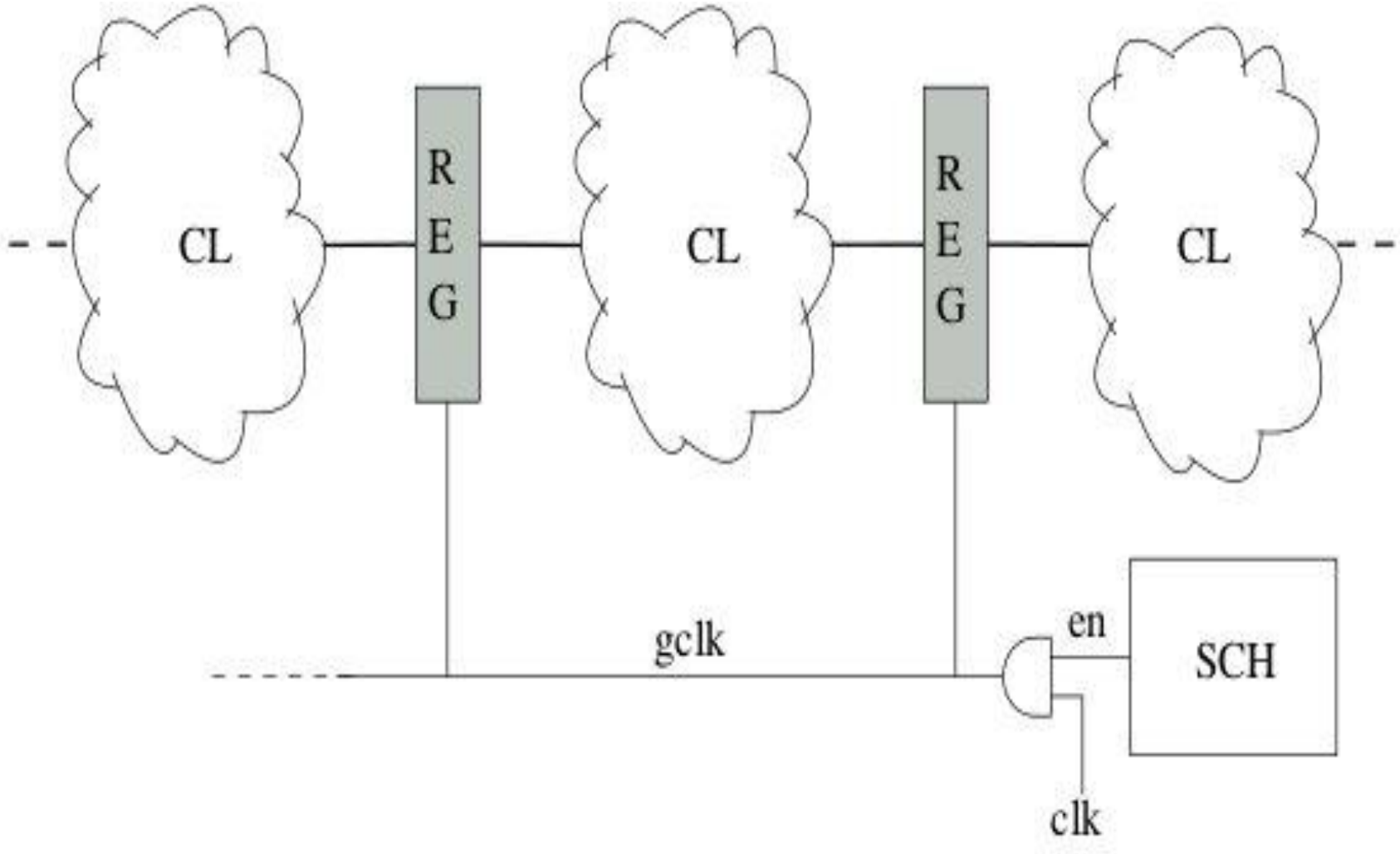
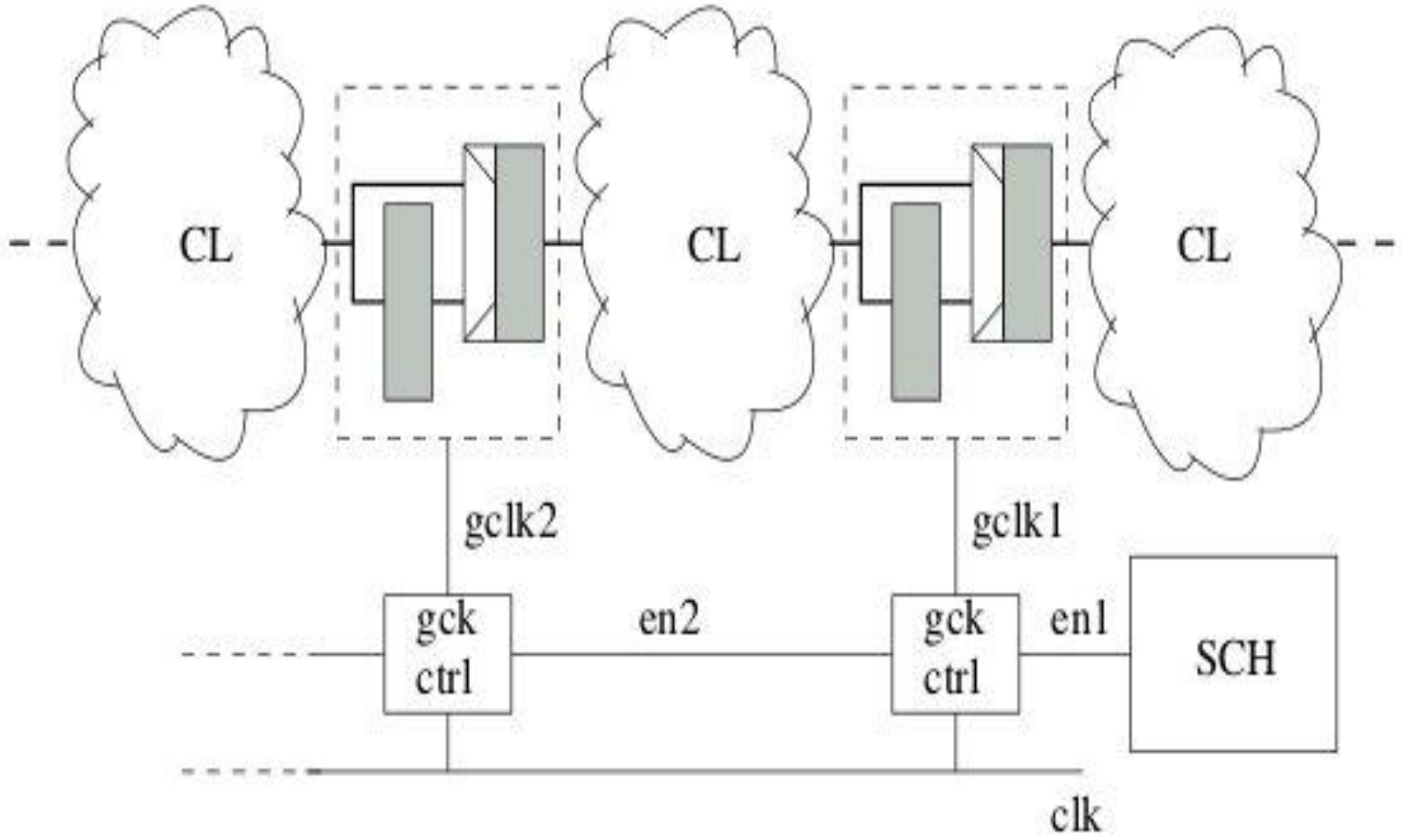
DVFS using clock gating mechanisms

- Global clock gating
- Distributed clock gating using relay station
- Distributed clock gating using latches

DVFS using global clock gating



Distributed clock gating with relay station



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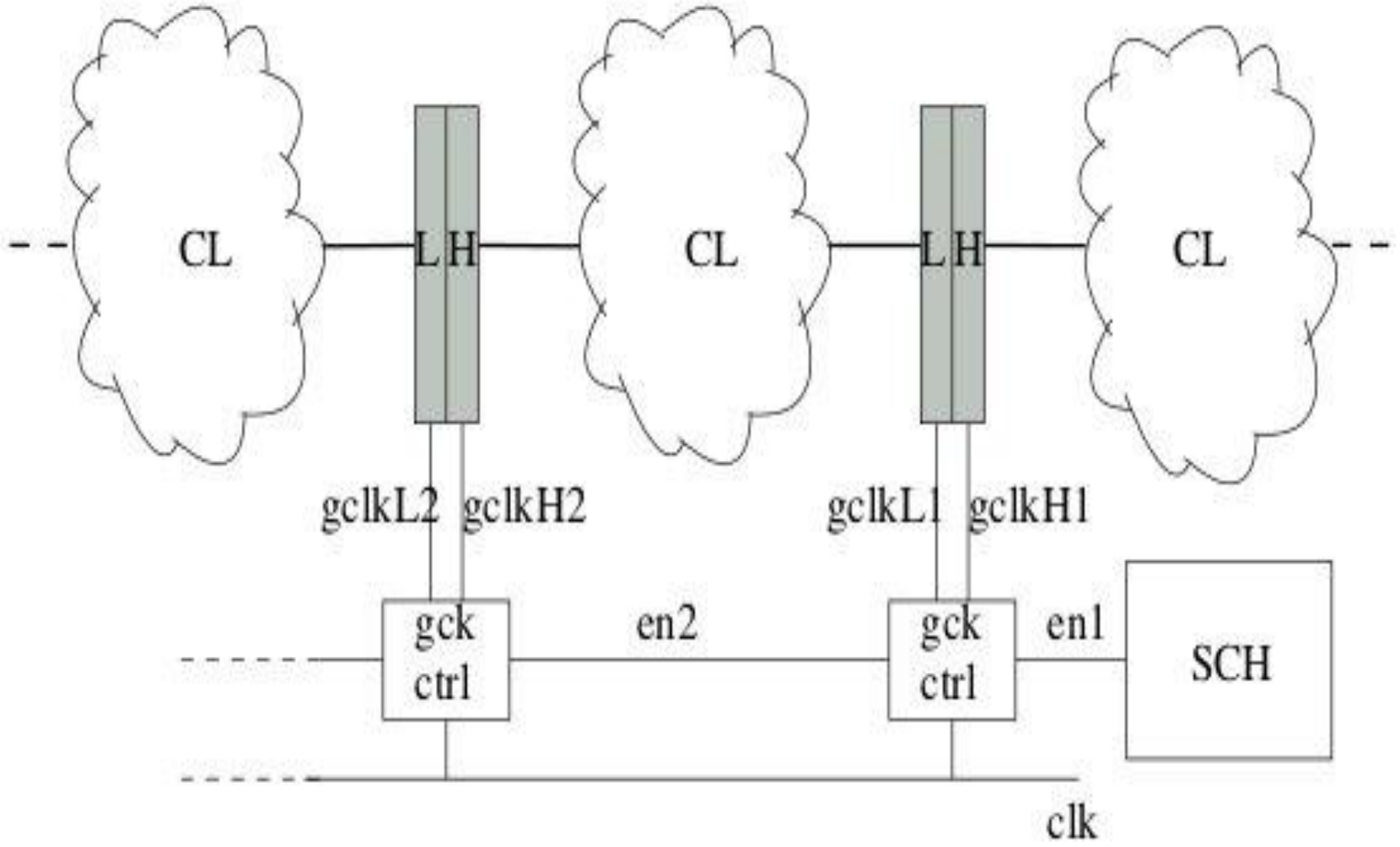
Distributed clock gating with latches



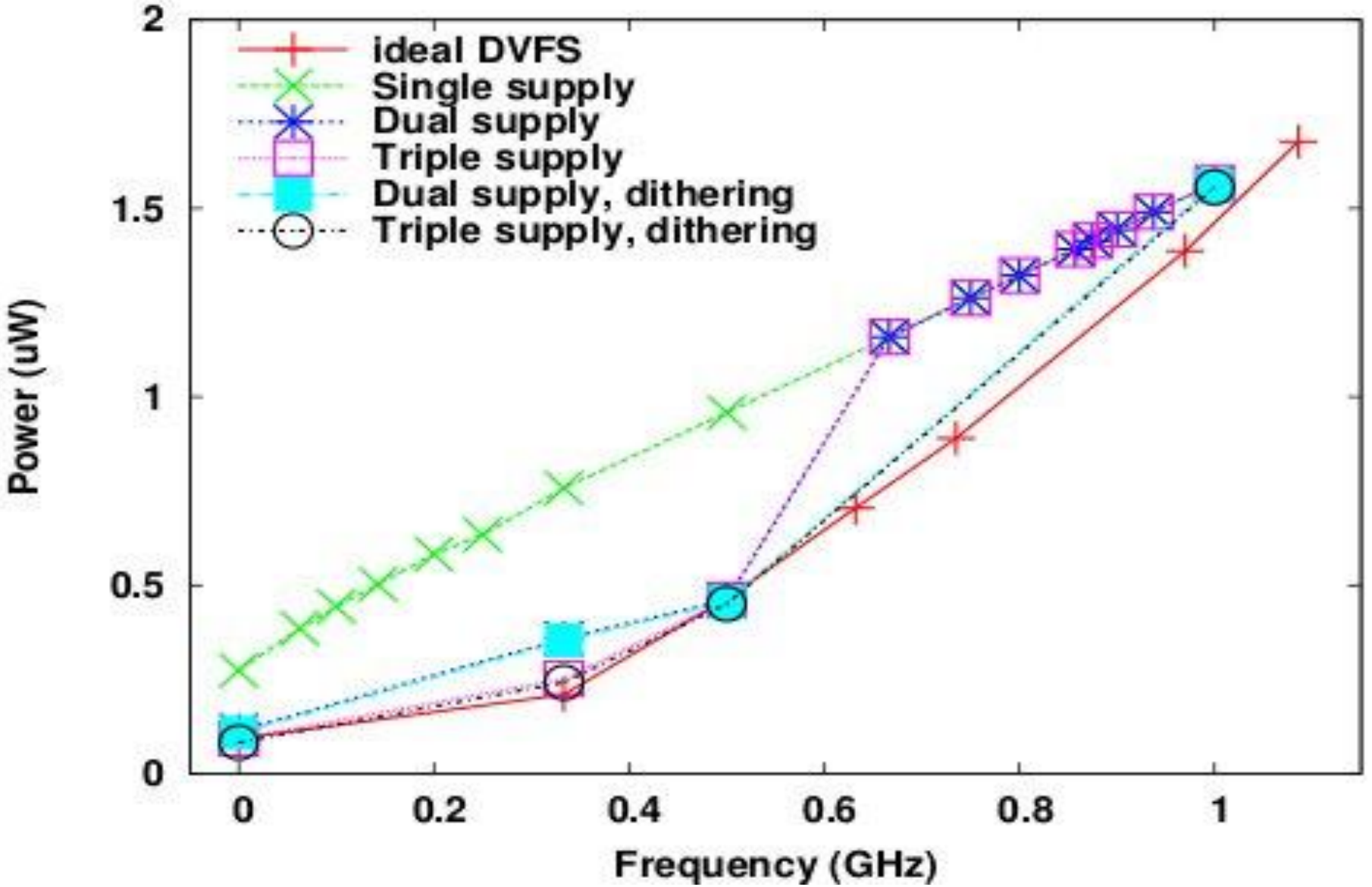
Comparison: Global vs Distributed clock gating

GLOBAL CLOCK GATING	DISTRIBUTED CLOCK GATING
No transition time	Transition time required. Time is dependent of number of stages in pipeline
Current-inrush	Smooth power envelope
Large fan-out	Small fan-out
Larger delay from schedule to enable	Minimum delay from schedule to enable

Experimental Results

- Simple Pipeline with adders
- Pipelined NoC switch

Power vs freq. of simple pipeline,global case



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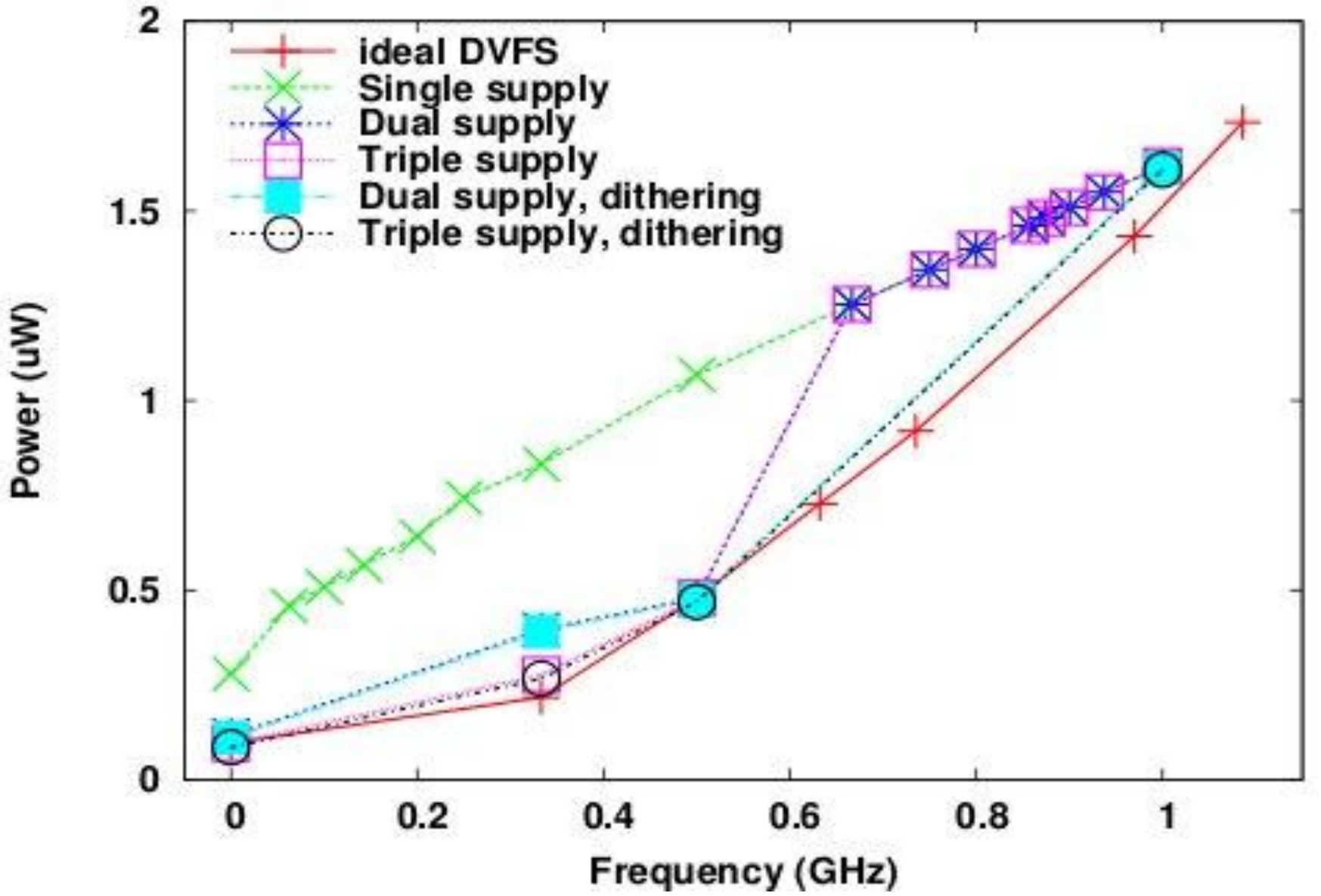
Power vs freq. of simple pipeline with latches



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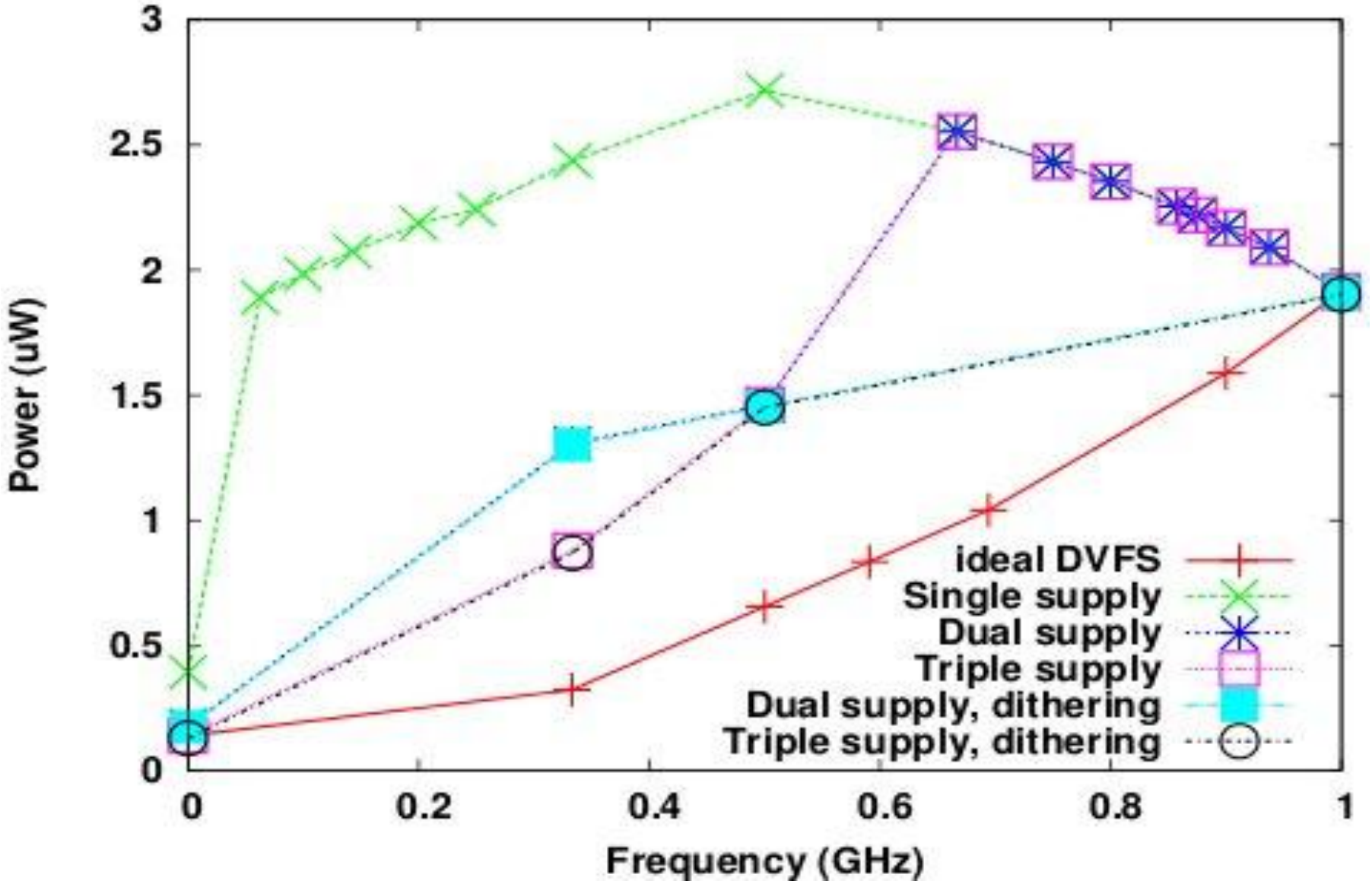
Power vs Freq of simple pipeline with RS



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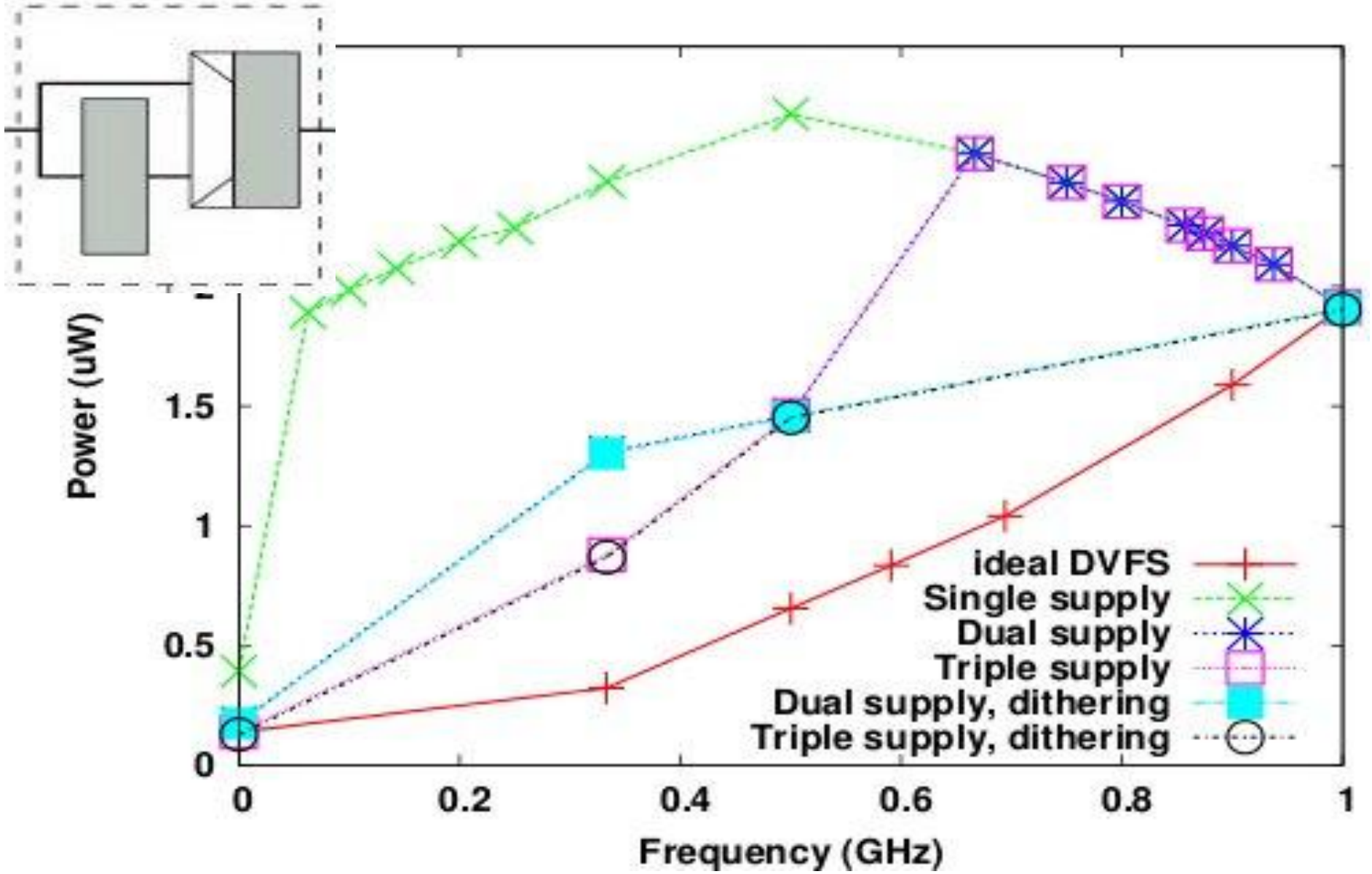
Power vs Freq of simple pipeline with RS



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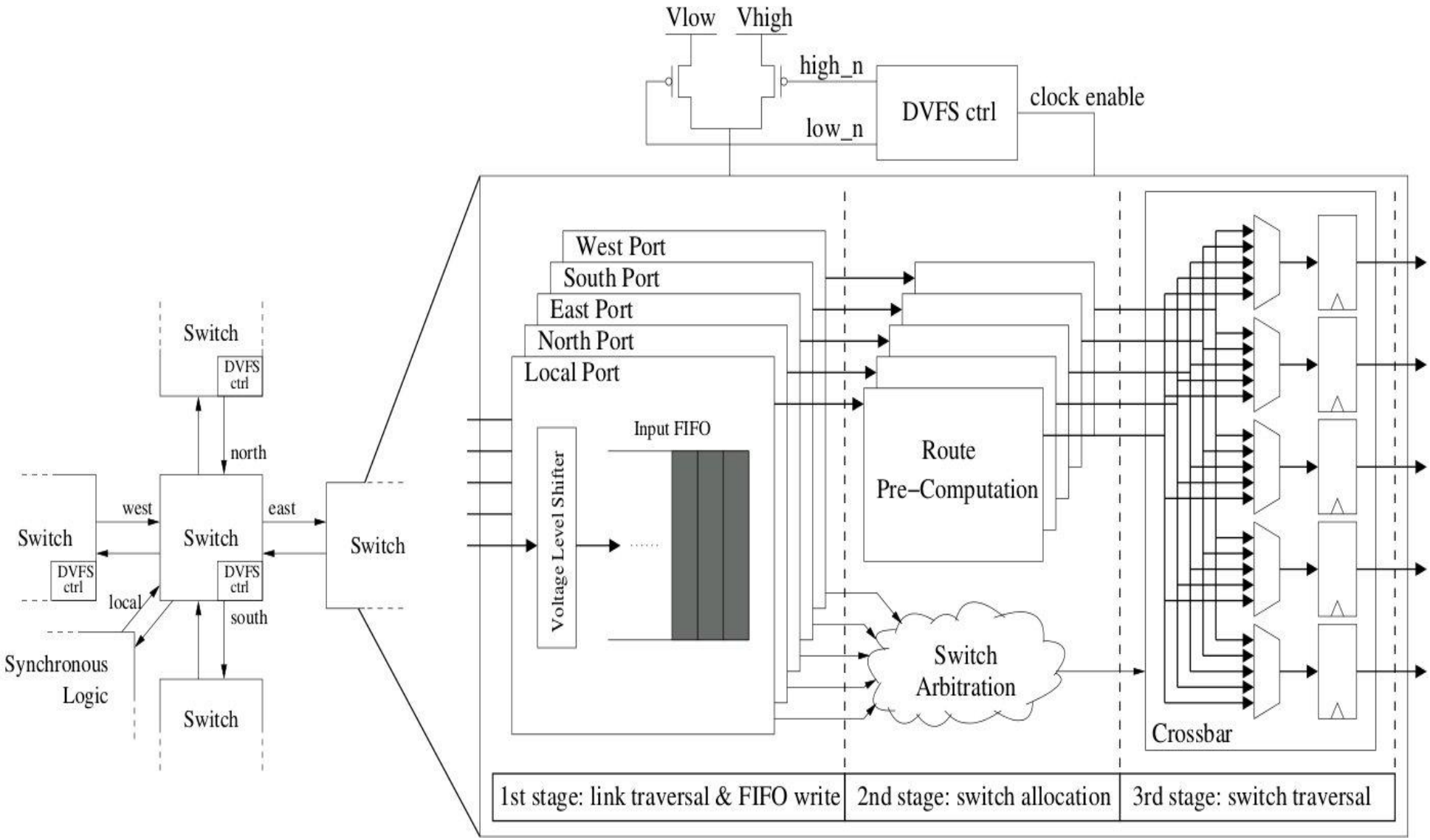
Pipelined NoC switch



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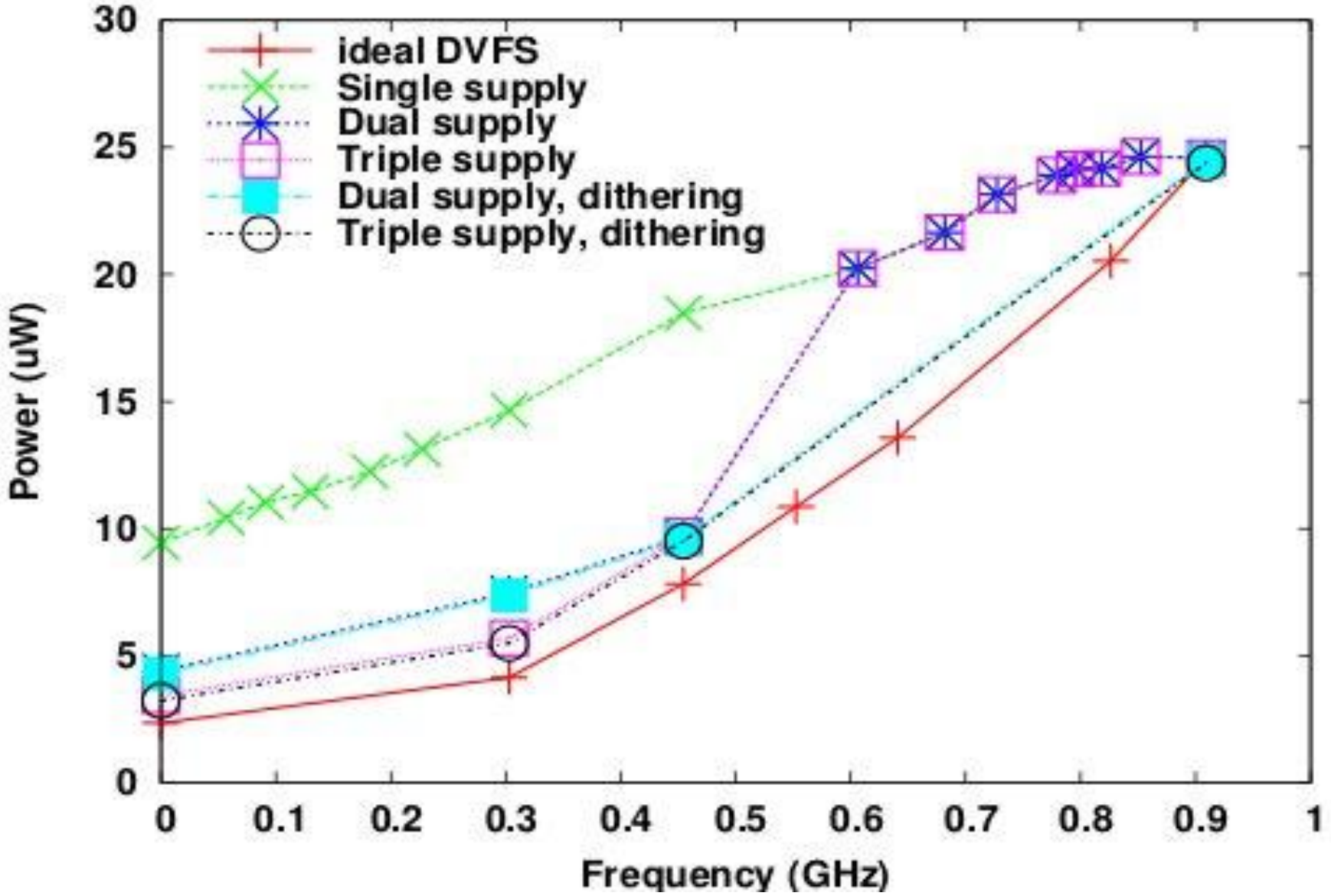
NoC switch and Power vs Freq. Global case



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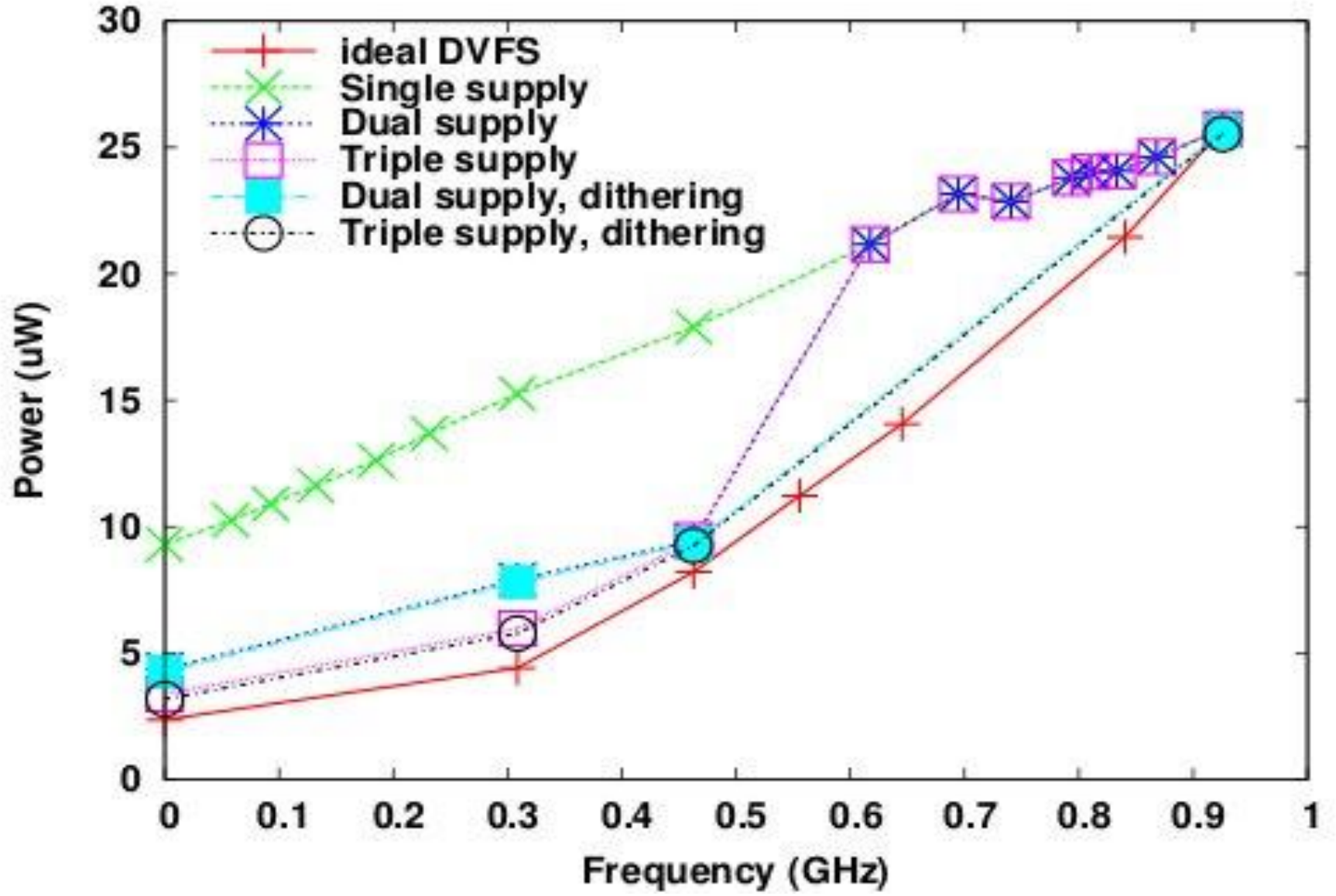
NoC switch and Power vs Freq. Latch case



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Conclusions

- Voltage scaling with few voltage levels
- Frequency scaling based on clock schedule
- Distributed clock gating is potentially advantageous compared to global clock gating
- Latch based distributed clock gating recommended

THANK YOU!!!
for your kind attention