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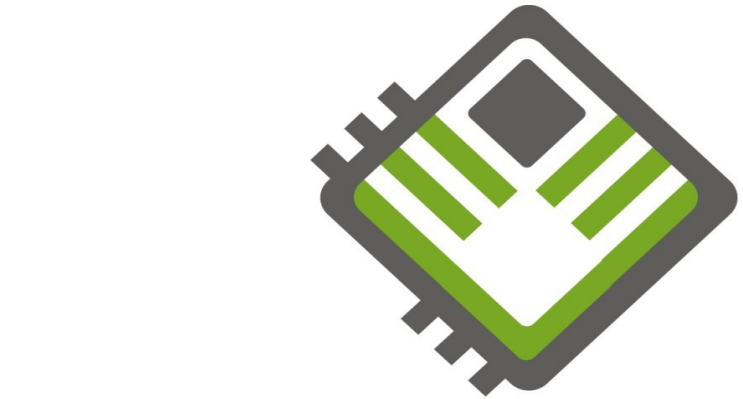

Tiempo

Tiempo Asynchronous Circuits System Verilog Modeling Language

Asynch 2012, Copenhaguen

sales@tiempo-ic.com

May 2012

Outline

Asynchronous Circuits
SystemVerilog Modeling Language

- Motivations
- Which modeling language ?
- Design flow
- Modeling Features
  - Channels
  - Channels operations (memorization, pipelining, non-determinism)
  - Sequential models (implicit and explicit FSM modeling)
  - Some other features
- Conclusion

The presentation is available here : www.tiempo-ic.com/uploads/Tiempo_Async_2012_Talk.pdf