ULTRA LOW POWER BOOTH MULTIPLIER USING ASYNCHRONOUS LOGIC

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  - General Operation
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**Motivation**

<table>
<thead>
<tr>
<th>Low Power Requirement in Embedded Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dynamic Power</strong></td>
</tr>
<tr>
<td><strong>Static Power</strong></td>
</tr>
<tr>
<td><strong>Target:</strong></td>
</tr>
</tbody>
</table>
Background – Booth Multiplier

- **Structure**
  - Partial Product Generator
  - Adder Block

- **Array-Based**
  - Regular Architecture
  - Balanced Capacitive Distribution
Positive Feedback Charge Sharing Logic

- PFCSL = PFAL (Positive Feedback Adiabatic Logic) + Charge Sharing Technology

## PFCSL vs PFAL

<table>
<thead>
<tr>
<th>Description</th>
<th>PFCSL</th>
<th>PFAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Clock</td>
<td>DC Supply (No overhead of power clock network)</td>
<td>Specifically designed Power Clock</td>
</tr>
<tr>
<td>Energy Recycling</td>
<td>~50%</td>
<td>~60%</td>
</tr>
<tr>
<td>Speed</td>
<td>Run @ 100MHz</td>
<td>Not Efficient in High-Speed Applications</td>
</tr>
</tbody>
</table>

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Positive Feedback Charge Sharing Logic

- General Operation
  1) VPC(i)\(\uparrow\) to VDD, VPC(i-1)\(\downarrow\) to Ground.
  2) VPC(i) Shares the ENERGY with VPC(i+1), meeting @ VDD/2
  3) VPC(i+1)\(\uparrow\) to VDD, VPC(i)\(\downarrow\) to Ground.

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Positive Feedback Charge Sharing Logic

- Power Estimation
- Charge Sharing: $Q = C_1V_1 = C_1V_2 + C_2V_2$
- Due to the Balanced Distribution, ~50% Energy transferred from one stage to the next.
Signal Transition Diagram

- Four-Phase Handshaking Model
  - Controlled by C-element

- PFCSL Handshaking Model
  - Controlled by Dynamic-AND

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Two Controlled Latch

- Normal D-Latch is **NOT** suitable in PFCSL circuits.

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PFCSL Booth Multiplier

- Only ONE set of Y(i) is fetched at each time.
- Smaller Area
- Lower Power

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## Results Comparison – ADDER

### One-Bit Full Adder (VDD=1V, 45nm TSMC)

<table>
<thead>
<tr>
<th>Speed</th>
<th>Static</th>
<th>Dynamic</th>
<th>PFAL (Non-Adiabatic)</th>
<th>PFCSL</th>
</tr>
</thead>
<tbody>
<tr>
<td>100MHz</td>
<td>325nW</td>
<td>550nW</td>
<td>520nW</td>
<td>266nW</td>
</tr>
<tr>
<td>~</td>
<td>20%</td>
<td>52%</td>
<td>49%</td>
<td>/</td>
</tr>
</tbody>
</table>

**Dynamic Power**

**Static Power**

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Results Comparison – Multiplier

Dynamic Power

Static Power

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## Results Comparison – Multiplier

### Area Comparison (Transistor Numbers)

<table>
<thead>
<tr>
<th></th>
<th>PPG</th>
<th>Communication Circuits</th>
<th>Adders</th>
<th>Latches</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFCSL</td>
<td>1830</td>
<td>280</td>
<td>6231</td>
<td>4300</td>
<td>12641</td>
</tr>
<tr>
<td>STATIC</td>
<td>6544</td>
<td>154</td>
<td>6952</td>
<td>3440</td>
<td>17090</td>
</tr>
</tbody>
</table>
Conclusion & Future Work

- New Logic family – PFCSL
- New structure of PPG, Booth Multiplier
- Power and area improvements
- In the future, implement into 8051 microcontroller design. Fabricate it!!!
Acknowledgements

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Thank you!
Questions?