ULTRA LOW POWER BOOTH MULTIPLIER USING ASYNCHRONOUS LOGIC

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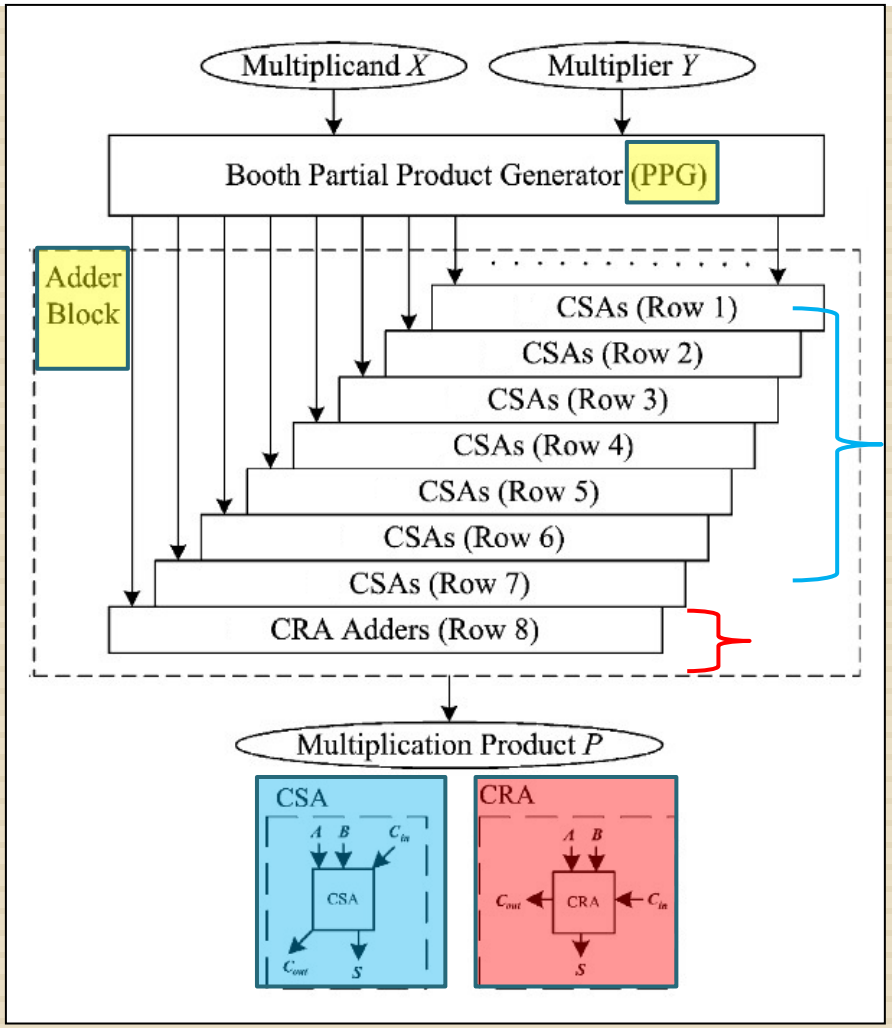
Motivation

Low Power Requirement in Embedded Systems	
Dynamic Power	Lower Voltage Supply, Avoid Unwanted Switches, Adiabatic Logic and etc.
Static Power	Power Gating, Multi-threshold and etc.
Target:	Low Power Parallel Multiplier (Booth Radix-4 Array Multiplier)

Background – Booth Multiplier

- Structure
  - Partial Product Generator
  - Adder Block
- Array-Based
  - Regular Architecture
  - Balanced Capacitive Distribution



PositiveFeedbackChargeSharingLogic

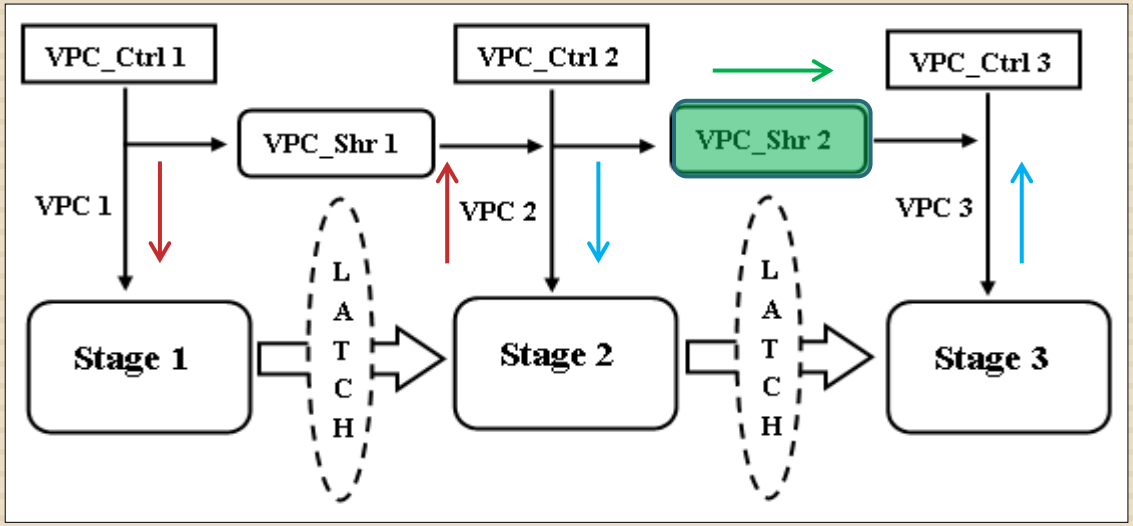
- PFCSL= PFAL (Positive Feedback Adiabatic Logic) +

  Charge Sharing Technology

PFCSL vs PFAL		
Power Clock	DC Supply (No overhead of power clock network)	Specifically designed Power Clock
Energy Recycling	~50%	~60%
Speed	Run @ 100MHz	Not Efficient in High-Speed Applications

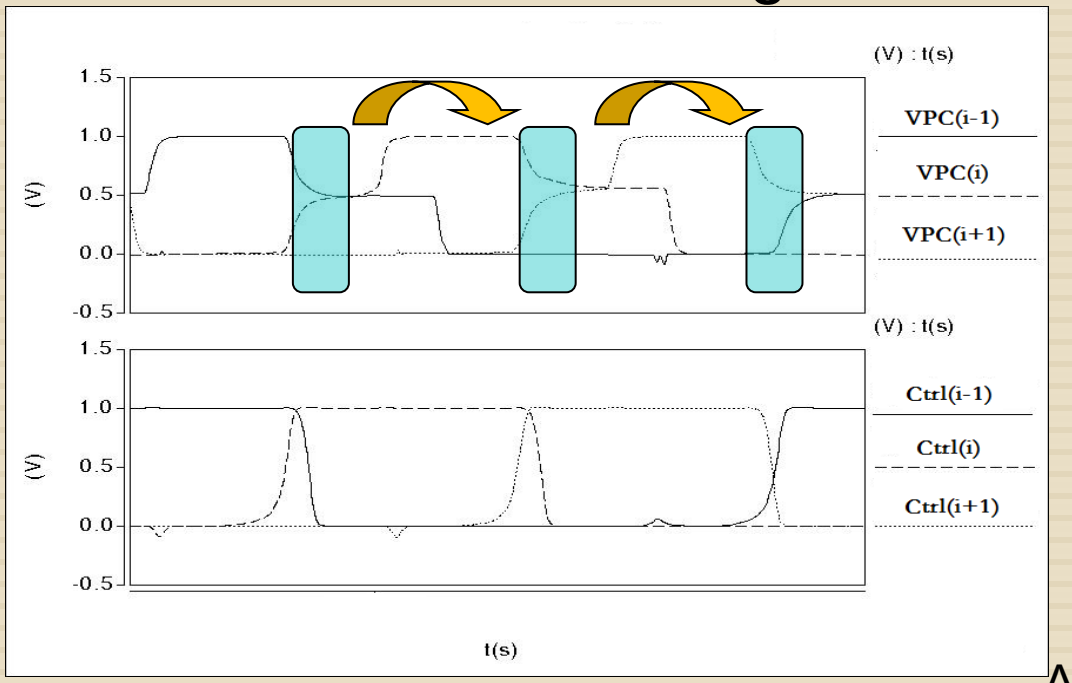
PositiveFeedbackChargeSharingLogic

- General Operation
  1) VPC(i) ↑ to VDD, VPC(i-1) ↓ to Ground.
  2) VPC(i) Shares the ENERGY with VPC(i+1), meeting @ VDD/2
  3) VPC(i+1) ↑ to VDD, VPC(i) ↓ to Ground.



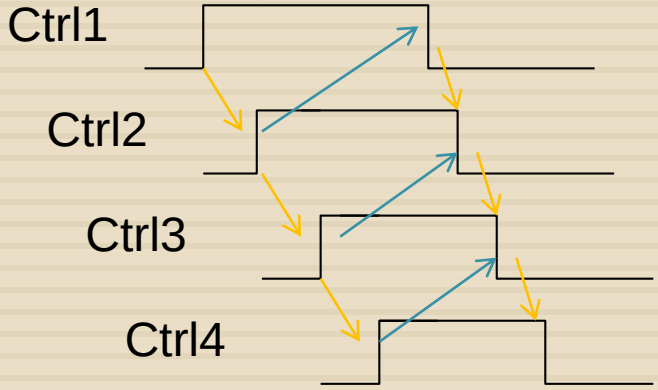
PositiveFeedbackChargeSharingLogic

- Power Estimation
  - Charge Sharing $Q = C_1V_1 = C_1V_2 + C_2V_2$
  - Due to the Balanced Distribution, ~50% Energy transferred from one stage to the next.

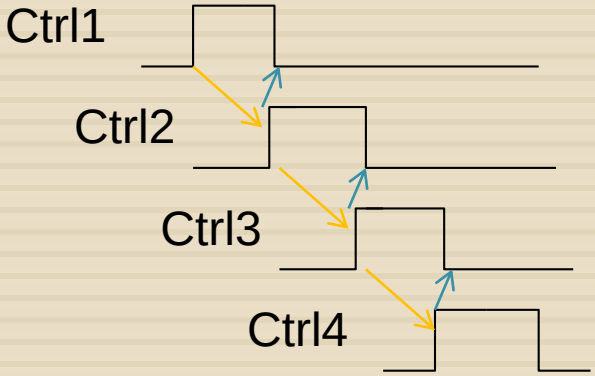


Signal Transition Diagram

- Four-Phase Handshaking Model
- Controlled by C-element

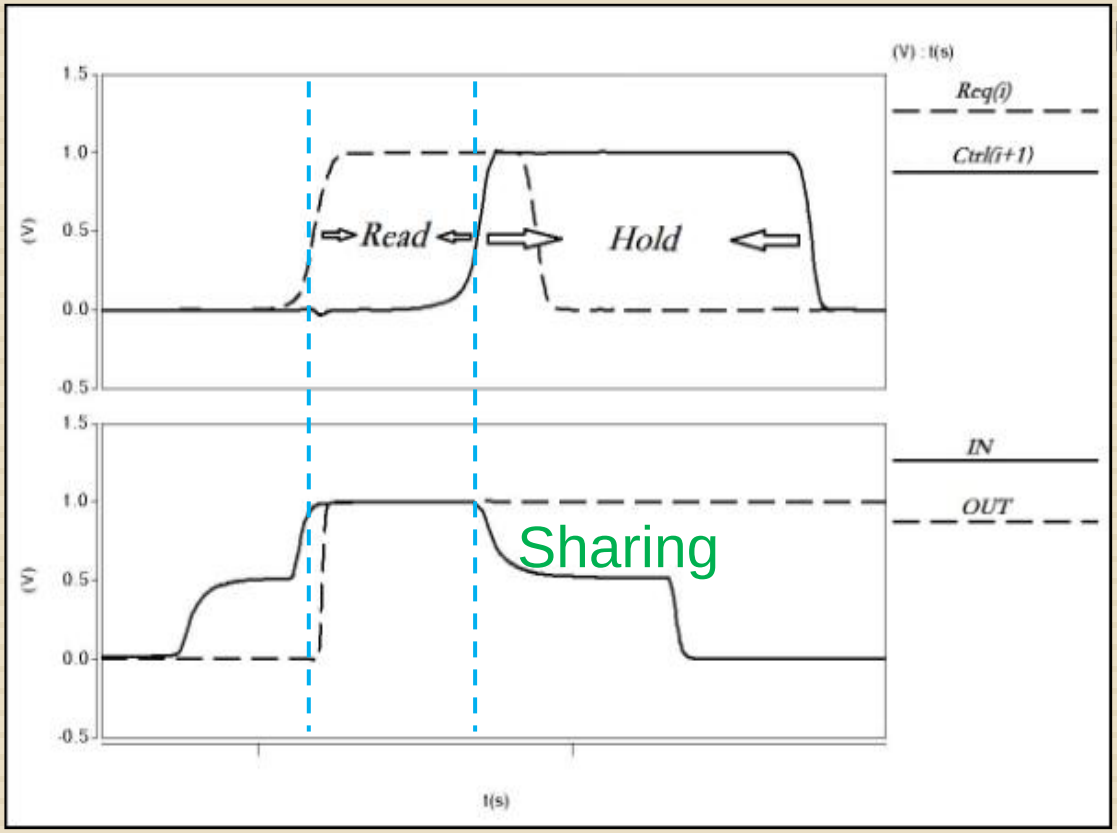


- PFCSL Handshaking Model
- Controlled by Dynamic-AND



Two Controlled Latch

- Normal D-Latch is NOT suitable in PFCSL circuits.



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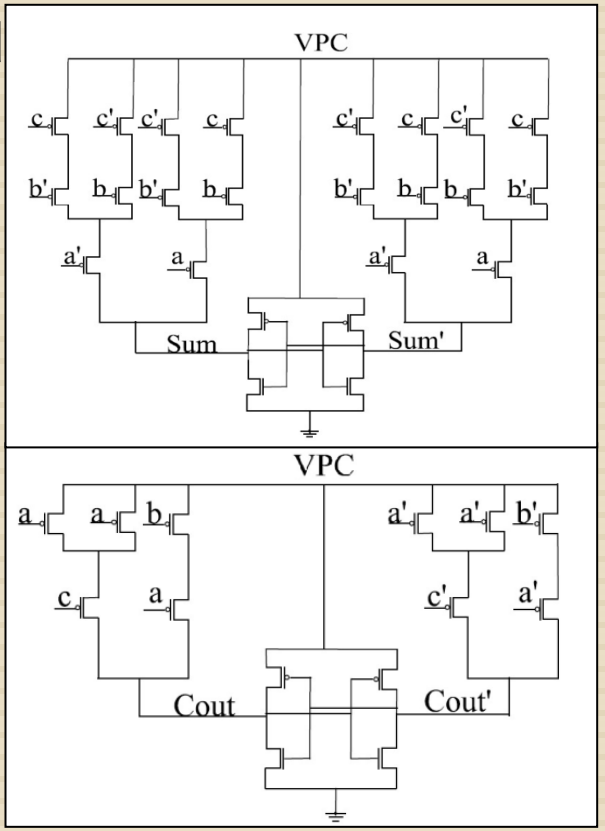
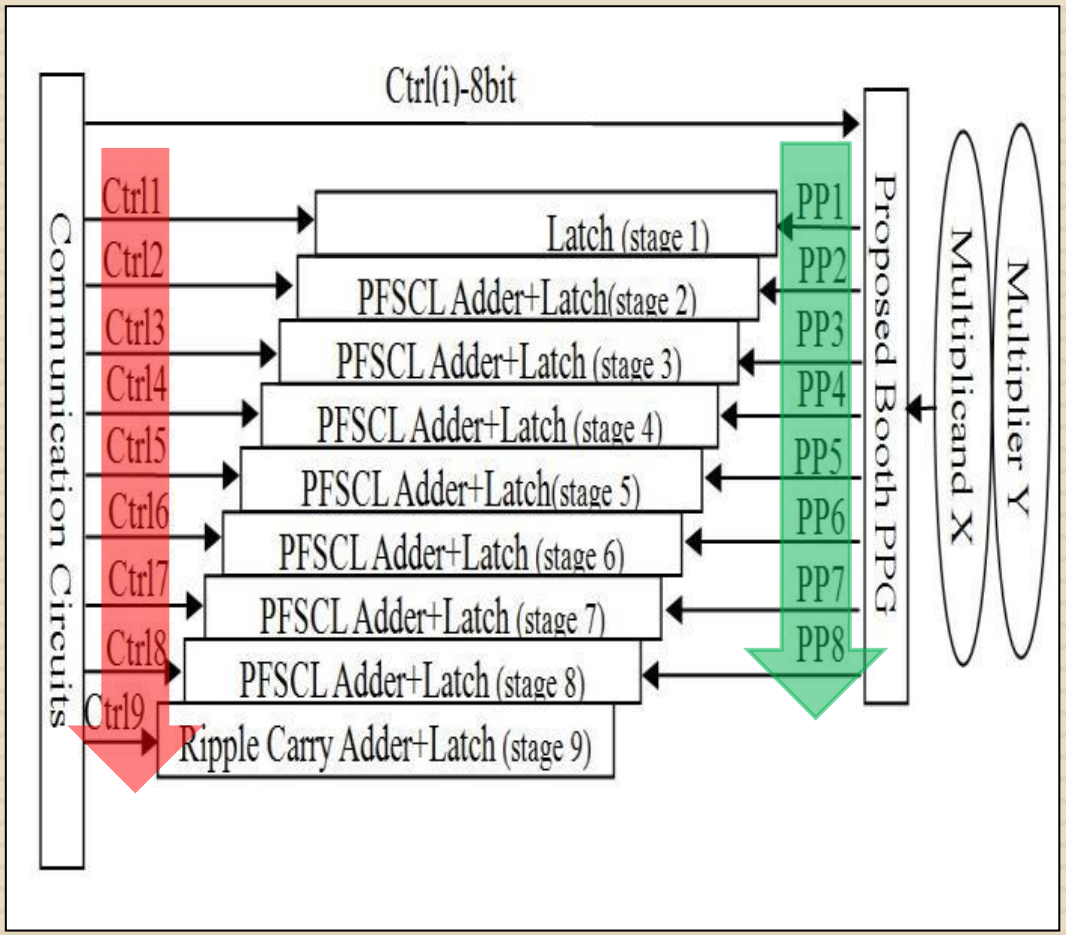
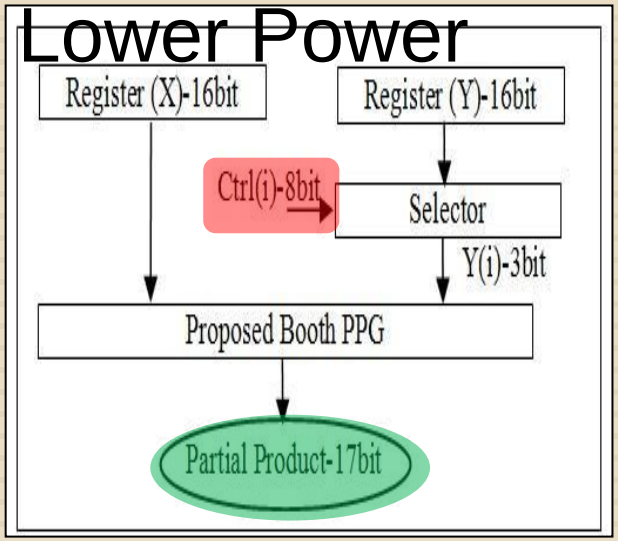


PFCSL Booth Multiplier



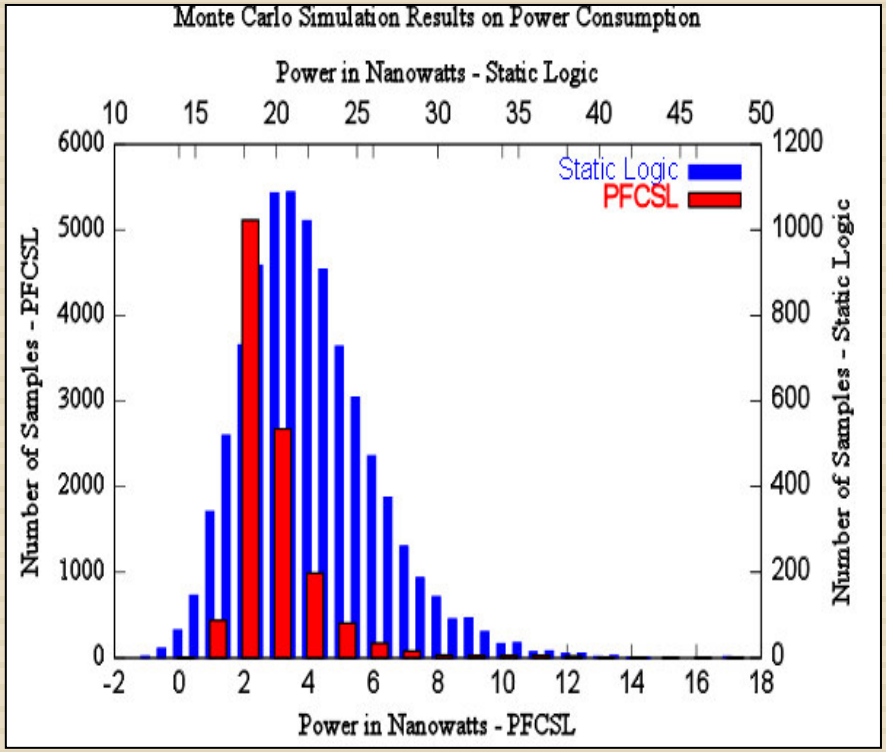
- Only ONE set of Y(i) is fetched at each time.
- Smaller Area
- Lower Power



Results Comparison – ADDER

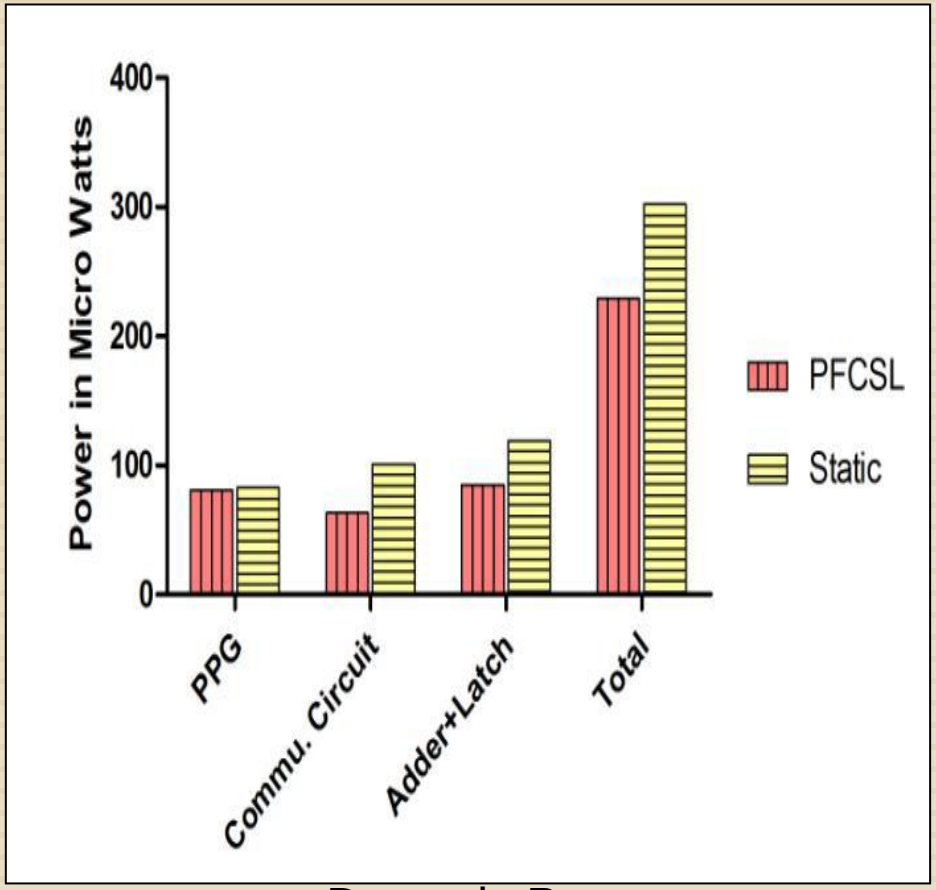
One-Bit Full Adder (VDD=1V, 45nm TSMC)				
Speed	Static	Dynamic	PFAL (Non-Adiabatic)	PFCSL
100MHz	325nW	550nW	520nW	266nW
~	20%	52%	49%	/

Dynamic Power

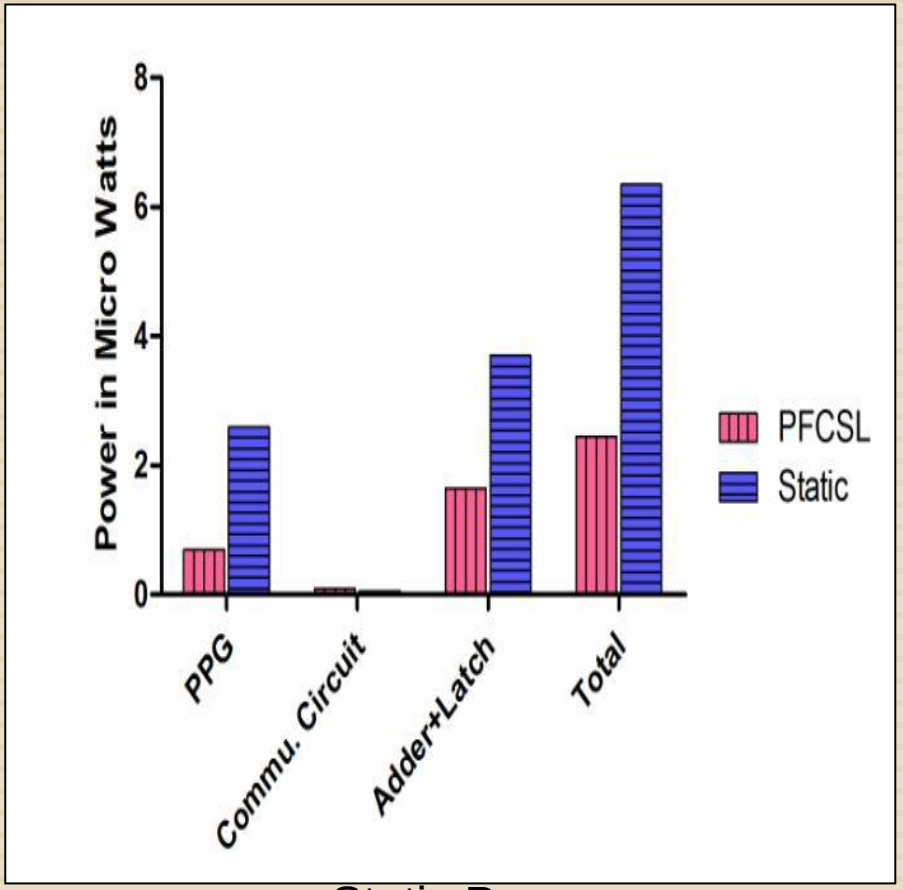


Static Power

Results Comparison – Multiplier



Dynamic Power



Static Power

Results Comparison – Multiplier

Area Comparison (Transistor Numbers)					
	PPG	Communication Circuits	Adders	Latches	Total
PFCSL	1830	280	6231	4300	12641
STATIC	6544	154	6952	3440	17090

Conclusion & Future Work

- New Logic family – PFCSL
- New structure of PPG, Booth Multiplier
- Power and area improvements
- In the future, implement into 8051 microcontroller design. Fabricate it!!!

Acknowledgements

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Thank you !
Questions ?