18th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), May 7-9, 2012, Copenhagen

High-Throughput Low-Energy Content-Addressable Memory Based on Self-Timed Overlapped Search Mechanism

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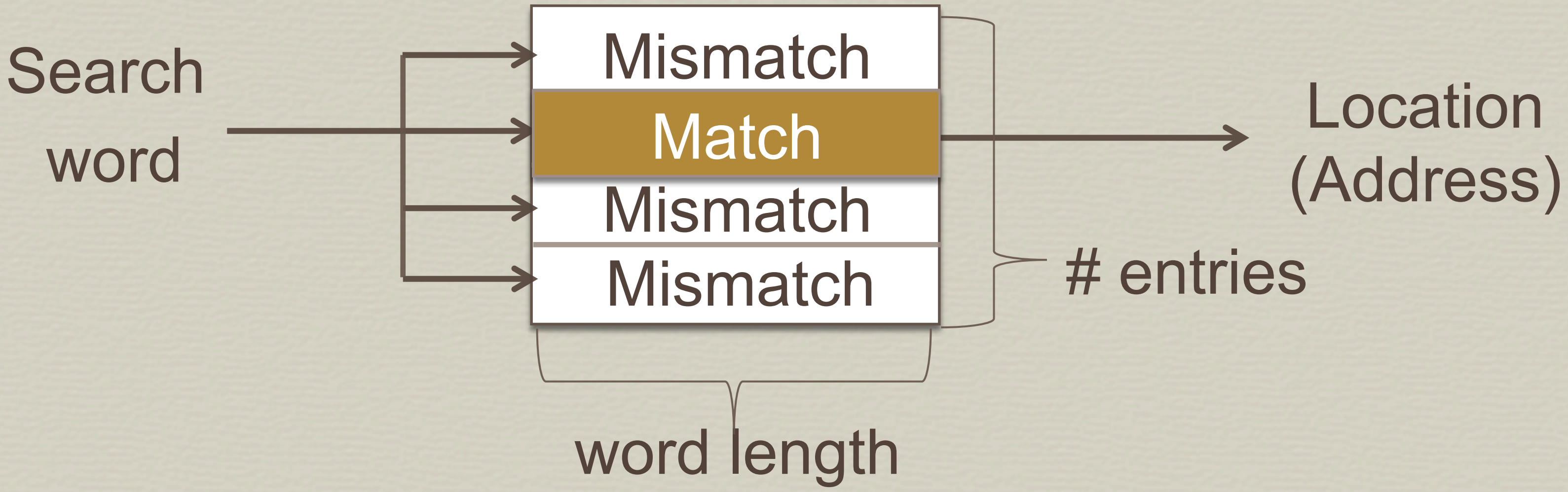
Acknowledgements
This research was supported by Japan Science Technology Agency (JST)
Development of Dependable Network-on-Chip Platform
in Core Research for Evolutional Science and Technology (CREST)

Content-Addressable Memory (CAM)

- Associative memory
- Parallel searching
- Applications
  - Cache, Virus checking
  - Packet forwarding (40G, 100Gbps)

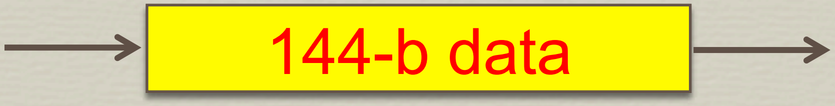


Hardware-Implementation Issue

Speed restriction

- Packet length - 32bit (IPv4), 128,144bit (IPv6)

Search word

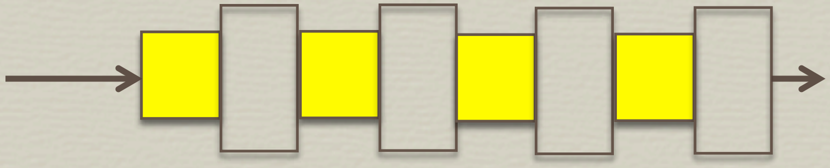


144-b data

➢ Large matching delay

<u>Pipelined approach</u> K. Pagiamtzis, et al (JSSC'04 vol.39-9)

Search word

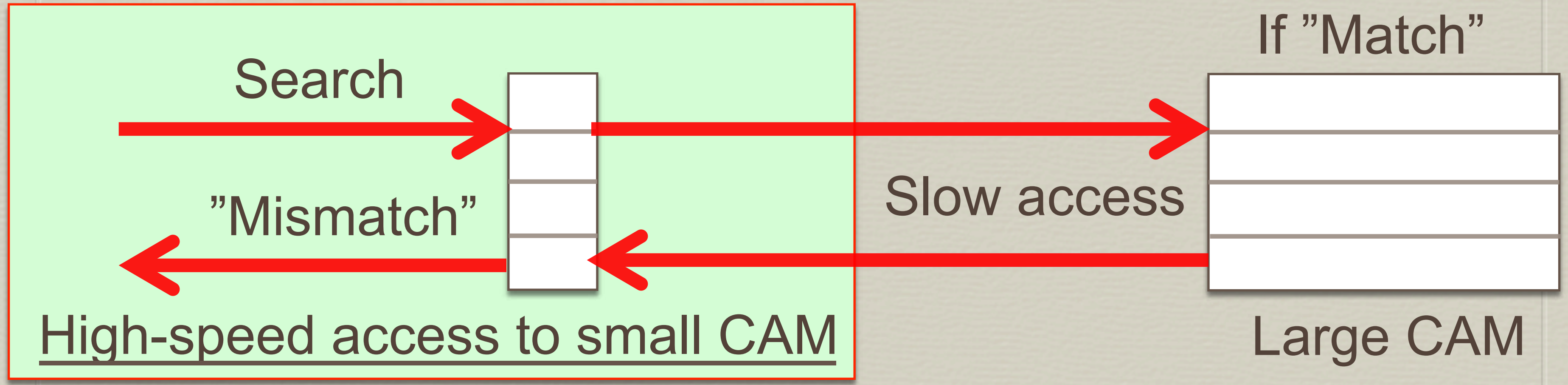


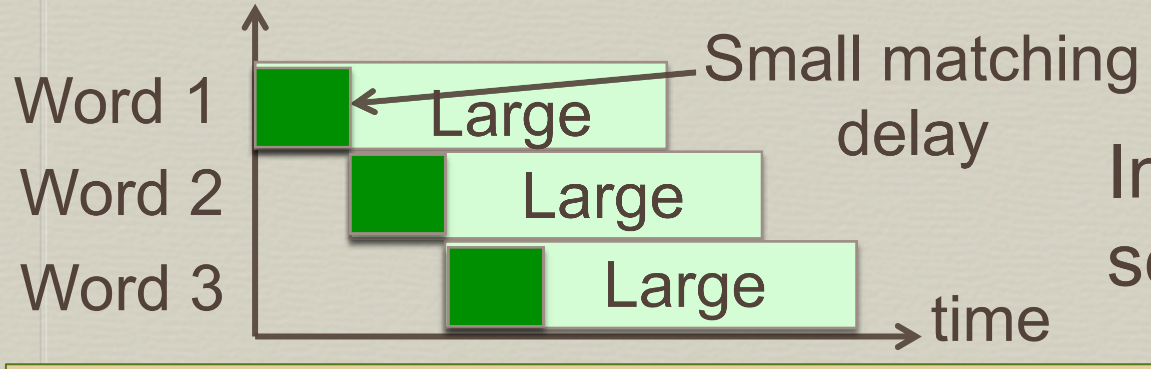
➢ Large area and power dissipation

Goal: High-throughput low-overhead CAM

Concept

- Operate as comparable to small CAM





In most cases, search words "match"

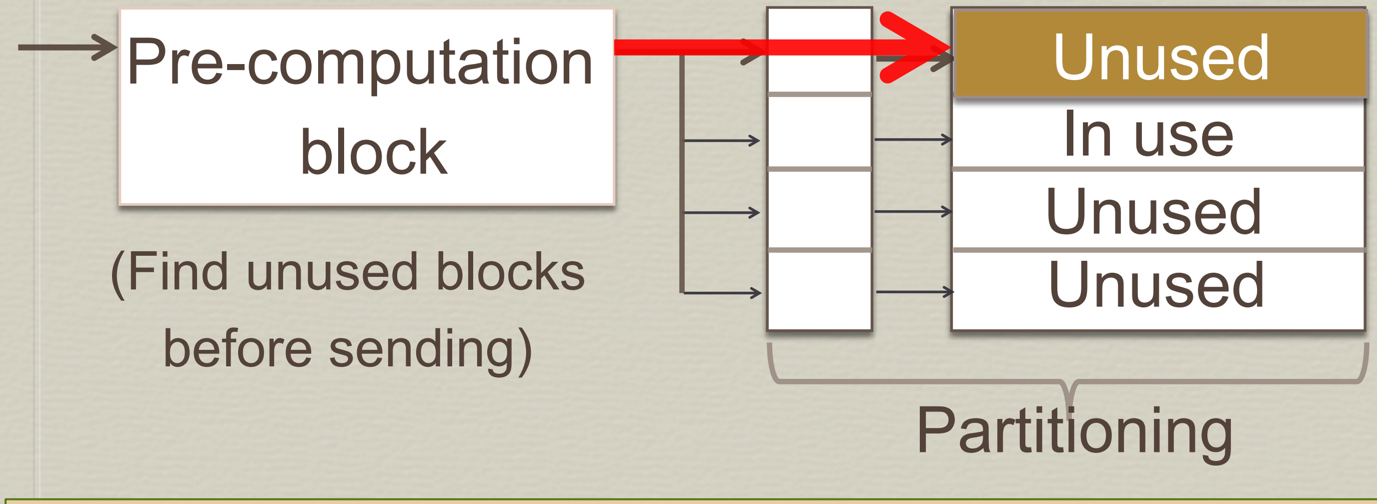
Hide large matching delay to improve throughput

Approach

- Assign search words to unused blocks

After searching first few bits, most blocks are mismatched

➢ If unused blocks are found, it doesn't need to wait to search new words until the current search is complete.



Search new words

after searching few bits

5.57x higher throughput at 8% cost of area

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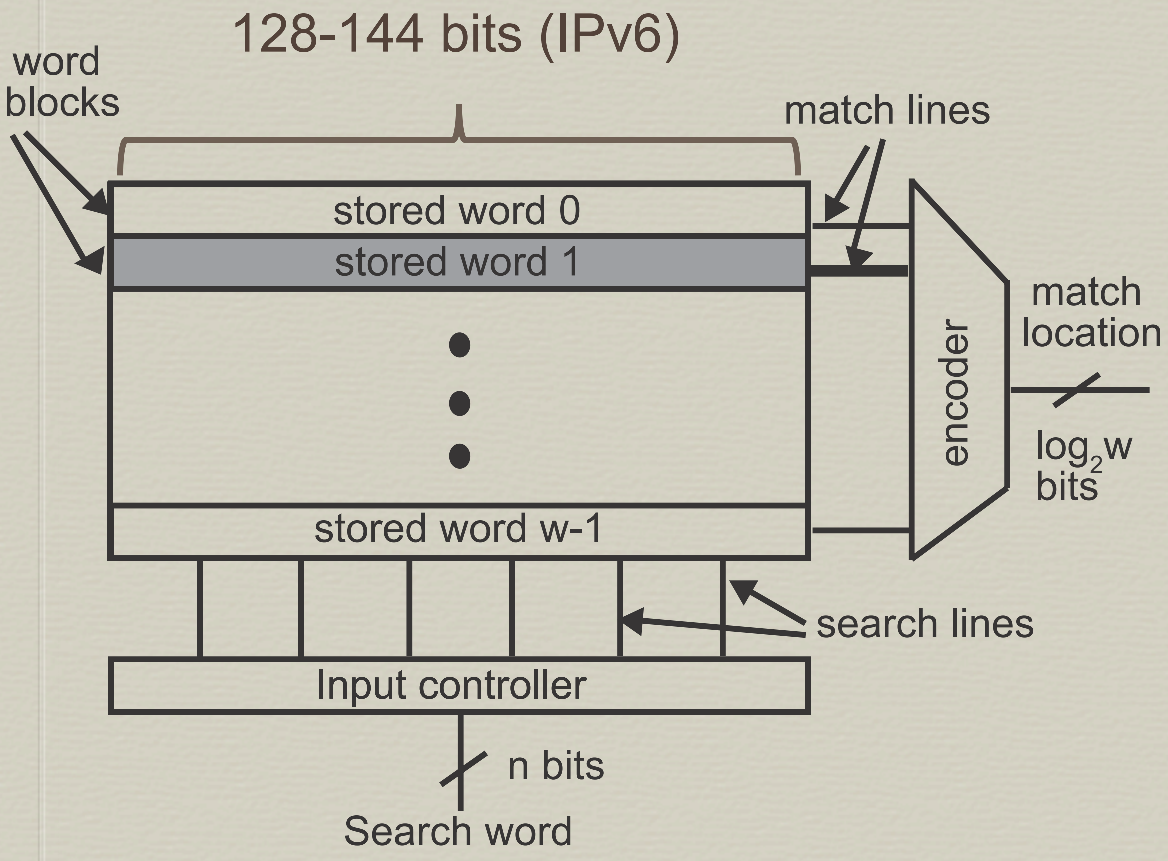
- Introduction to content-addressable memory
- Overlapped search mechanism
  - Word overlapped search
  - Phase overlapped processing
- Hardware implementation
- Evaluation
- Conclusion and future prospect

CAM



Operation

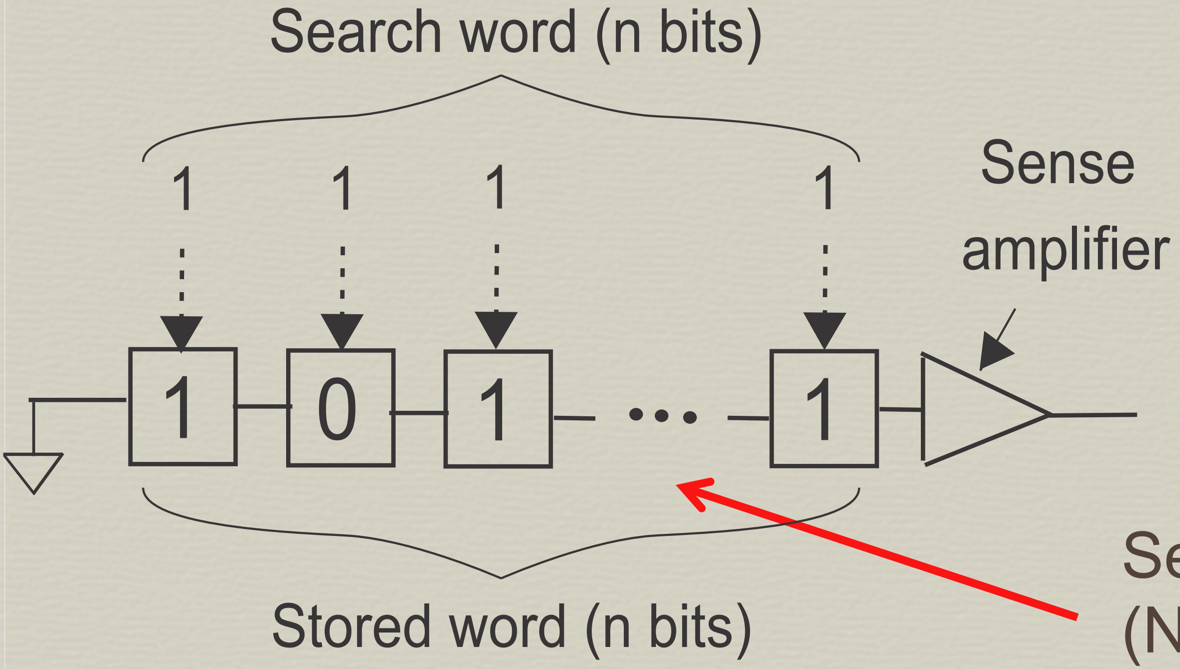
1. Search all words in parallel

2. Find a matched word block

3. Output a matched location (address)

Word-parallel search in single cycle

CAM Word Block



Conditions

- ● Match
- ● Mismatch

Series of CAM cells (NAND-type CAM)

Throughput determined by word length in conventional CAM

Long word length degrades throughput

CAM Characteristics

Matching probability of word blocks after k-bit search is

$$p_{matched} = \left(\frac{1}{2}\right)^k$$

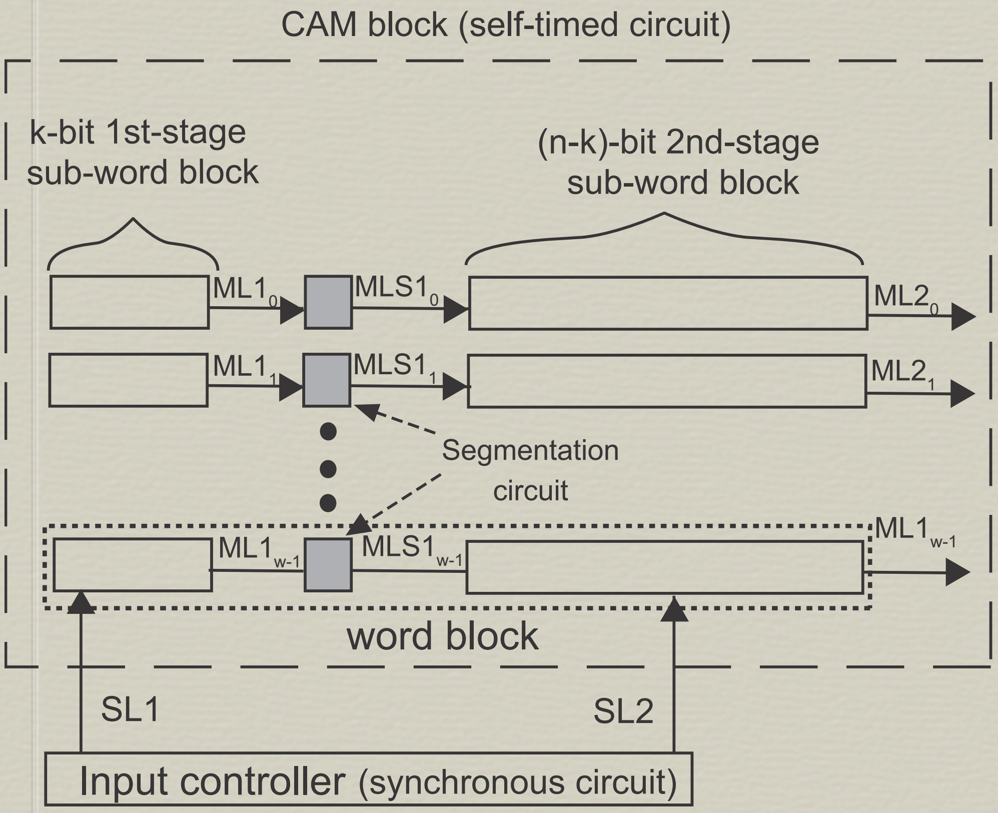
Most word blocks are not used after k-bit search (We set k=8 in the hardware implementation)

➢ Use unused blocks to improve throughput

Most word blocks are unused (mismatched).

Word Overlapped Search (WOS)

CAM architecture based on segmentation method



CAM block (self-timed circuit)
k-bit 1st-stage sub-word block
(n-k)-bit 2nd-stage sub-word block
ML1₀
MLS1₀
ML2₀
ML1₁
MLS1₁
ML2₁
Segmentation circuit
ML1w-1
MLS1w-1
ML1w-1
word block
SL1
SL2
Input controller (synchronous circuit)

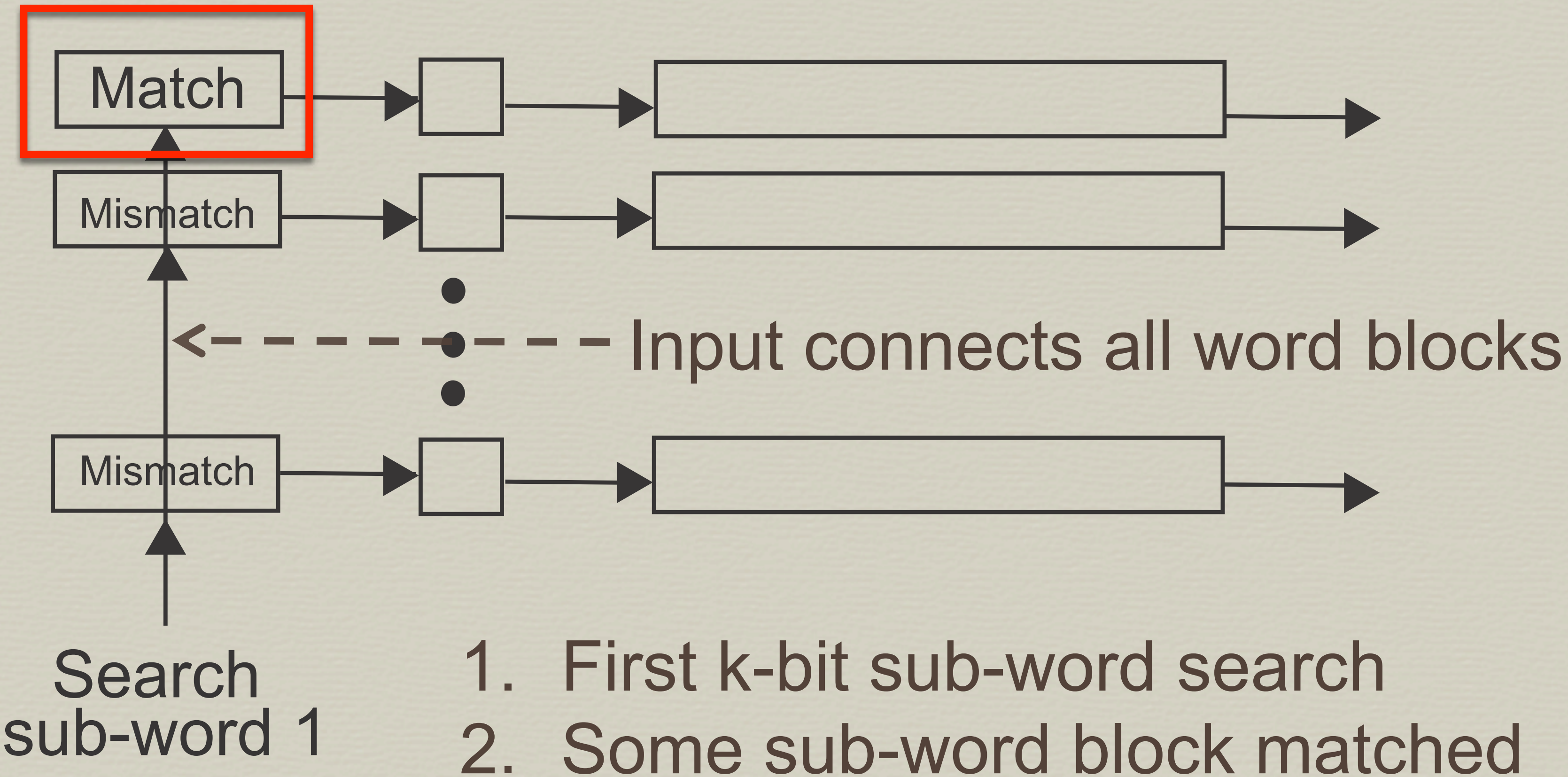
1. Partition word block to:
   a) small k-bit block and
   b) large (n-k)-bit block
   by segmentation block

2. Segmentation block stores Its k-bit matched result

3. Latter block operates when the first block matches

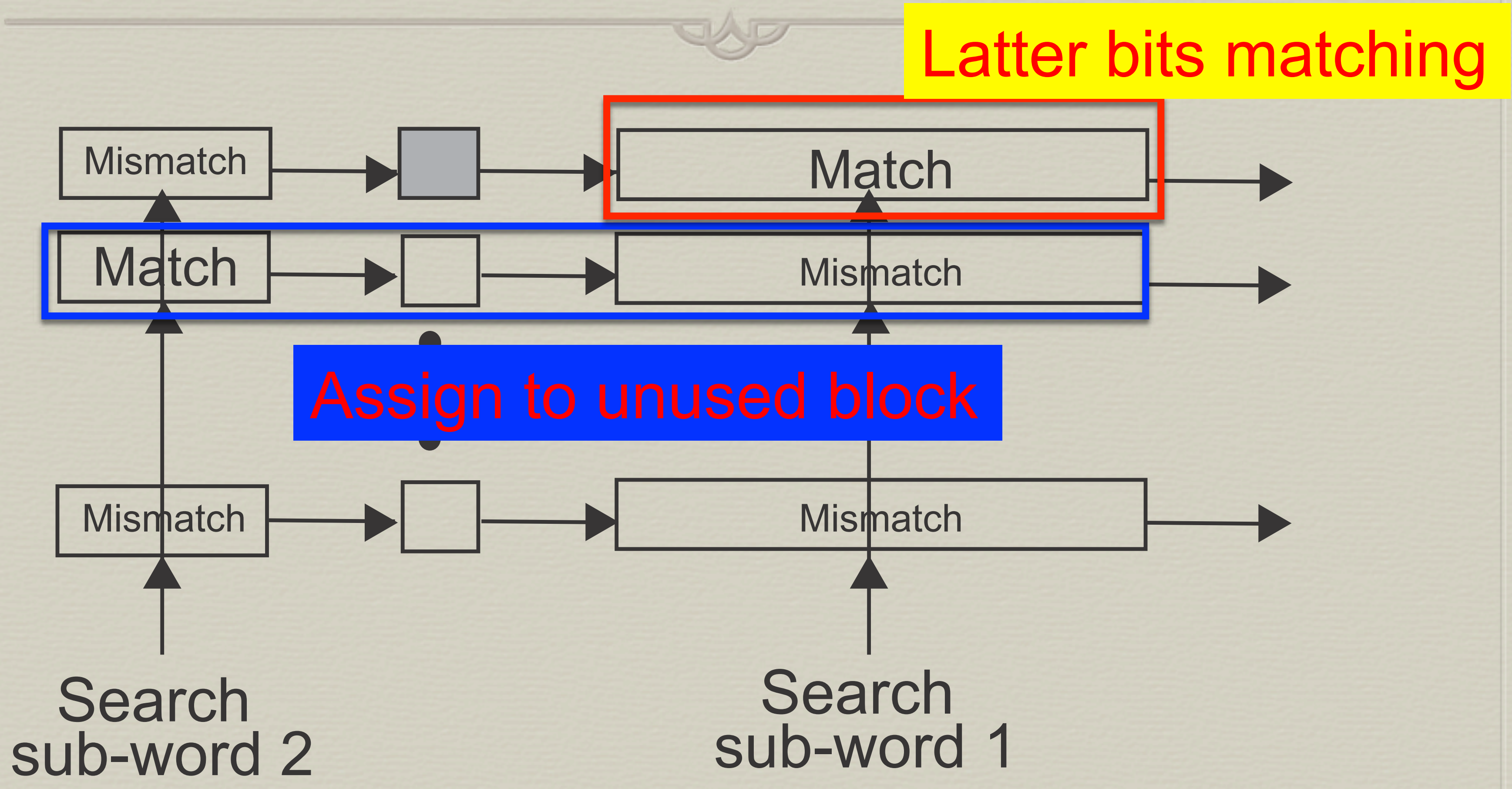
Word block partitioned by segmentation block

WOS operation



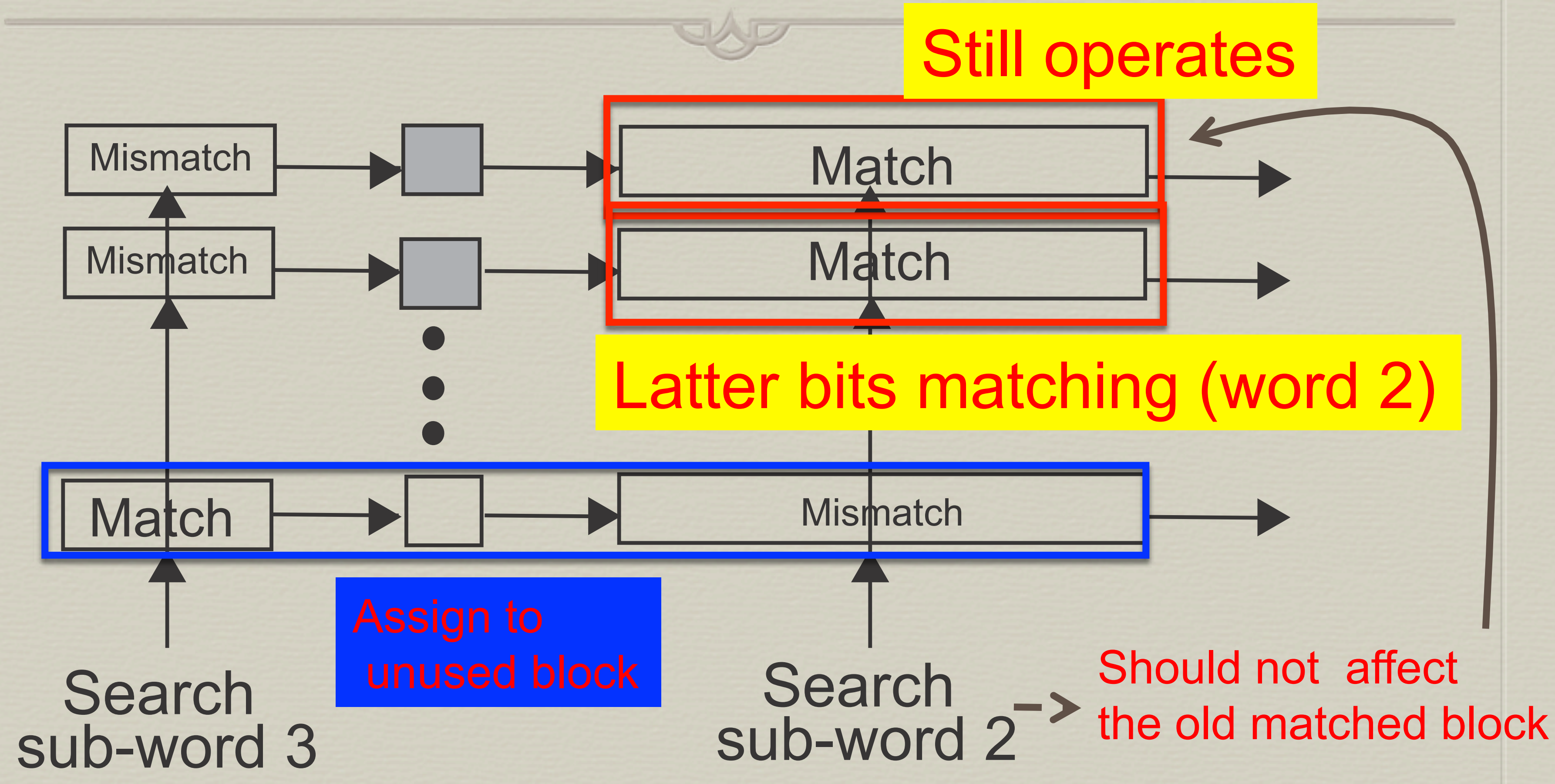
1. First k-bit sub-word search
2. Some sub-word block matched

WOS operation



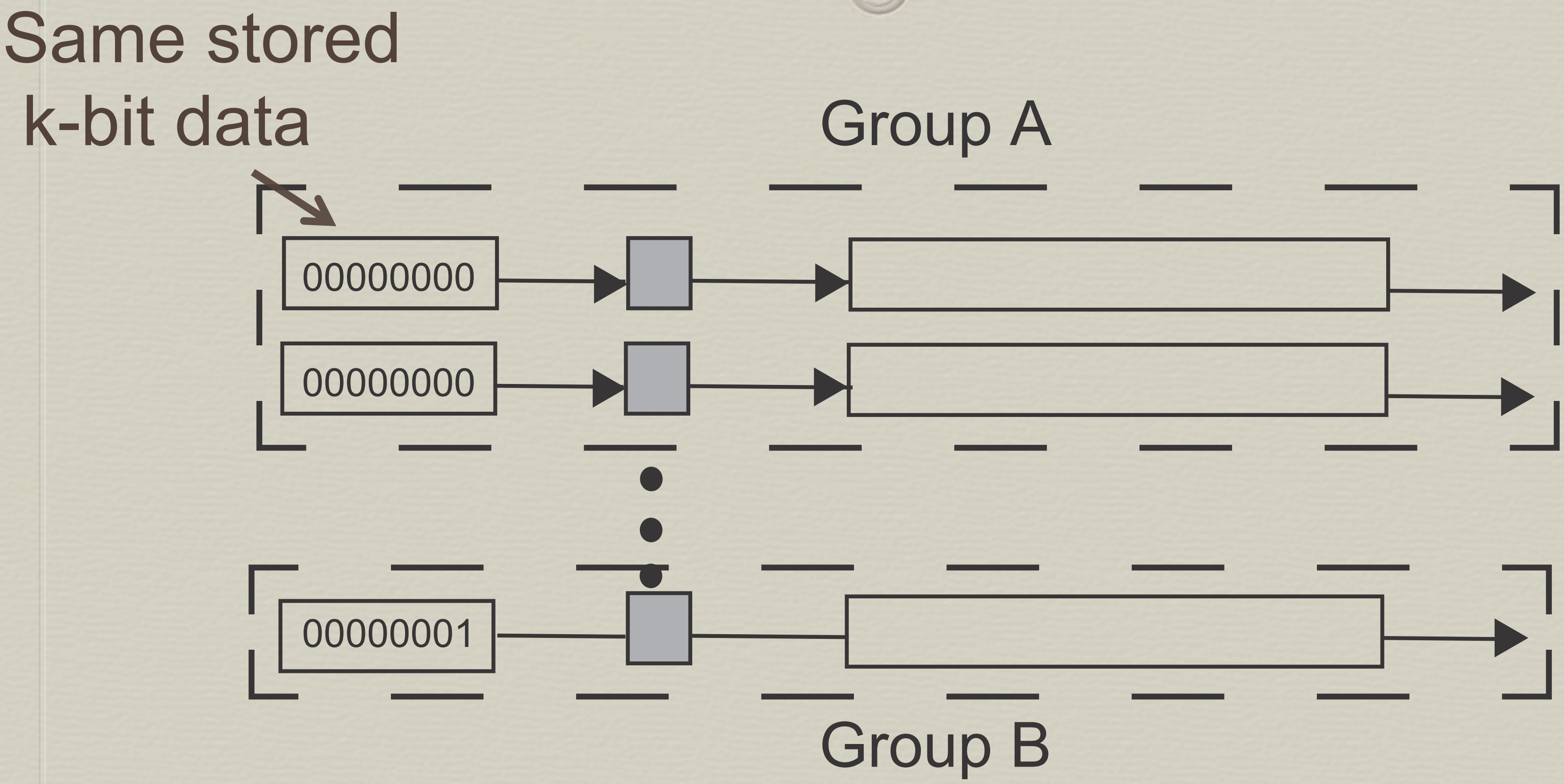
After k-bit search, new search starts

WOS operation



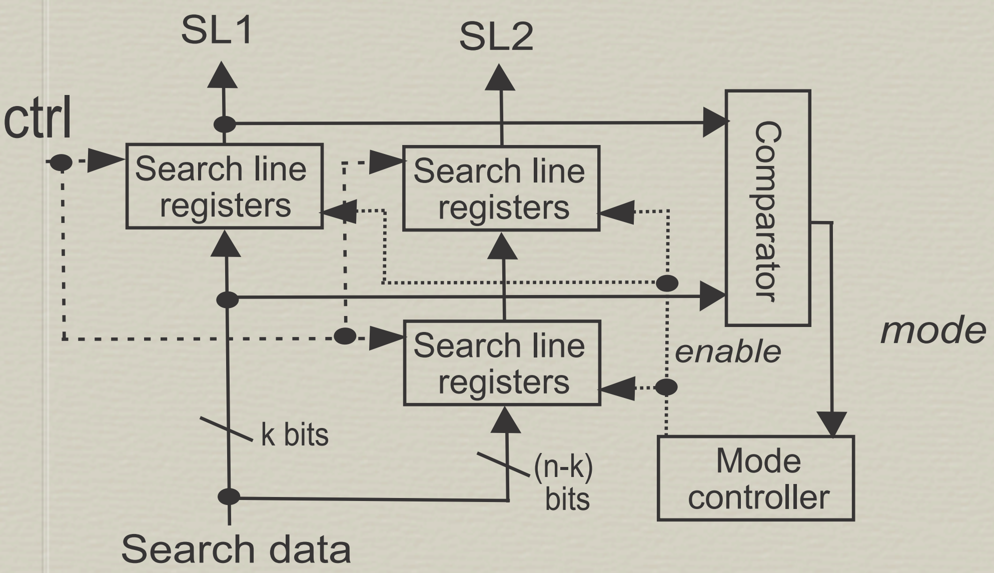
How to assign search words to unused blocks?

Categorize Word Blocks



Categorize based on the first k-bit stored word

Pre-Computation



Input controller (m=1)

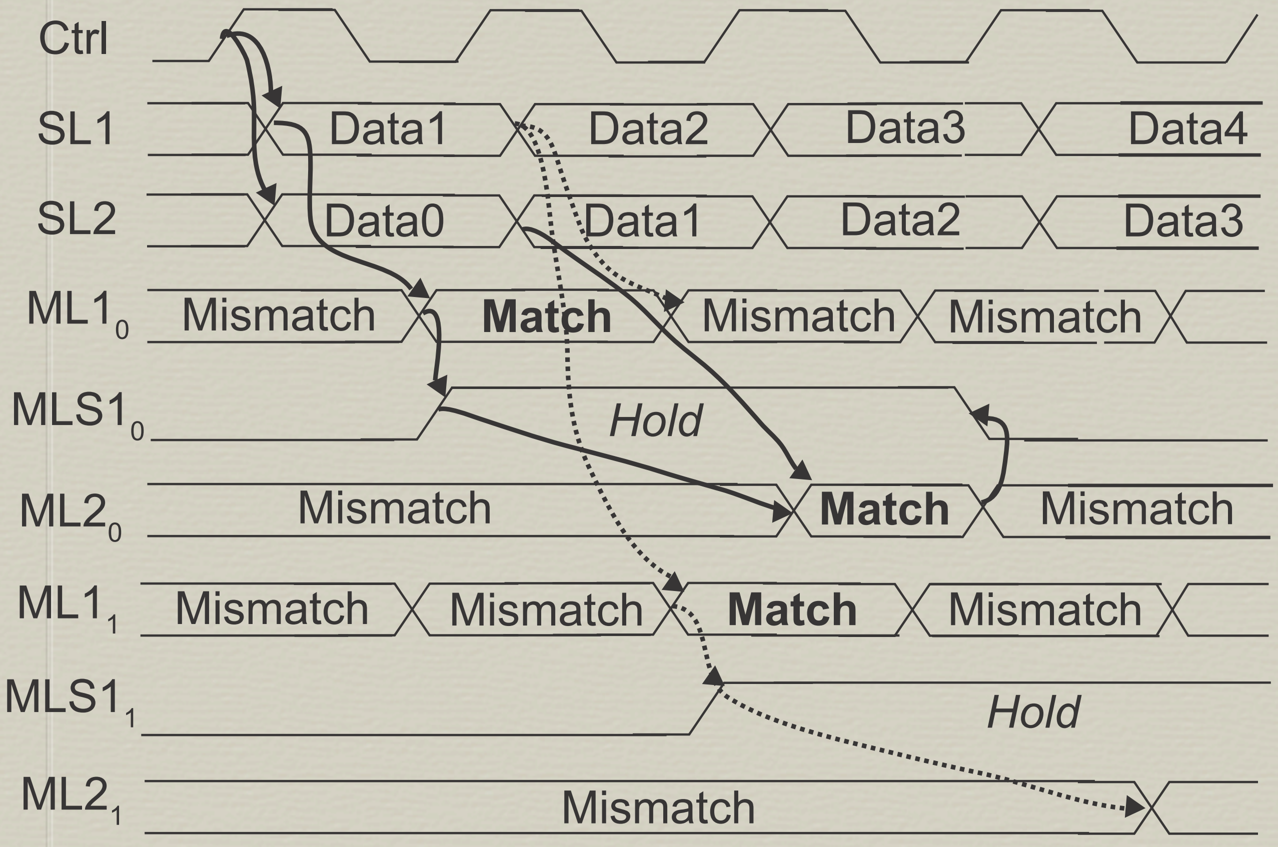
Compare “m” consecutive k-bit search words

If they are different,
they are in different groups
(Category 1: fast mode)

Otherwise,
they are in the same group
(Category 2: slow mode)

Categorize search words using comparator

Timing Diagram (fast mode)



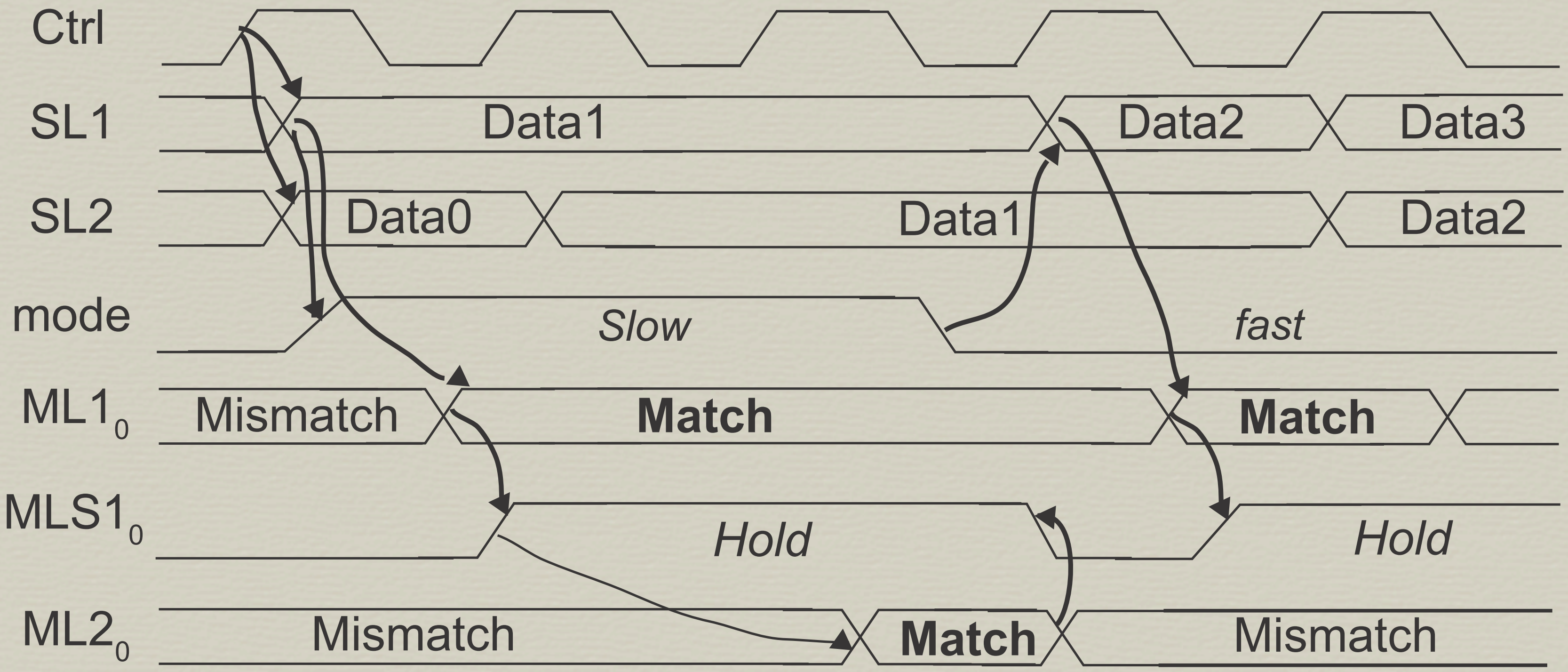
Send search words based on short delay T_{tst}

Consecutive words are assigned to unused blocks

(a)

High-speed searching based on T_{1st}

Timing Diagram (slow mode)



Two consecutive words use the same word block

Wait until the current search is complete

Average Search Delay

- Category 1 – fast mode

Send search words based on the first k-bit delay (T_{1st})

- Category 2 – slow mode

Send a new word after the current n-bit search is complete (T_{slow})

$$T_{sa} = T_{1st}\left(1 - m\left(\frac{1}{2}\right)^{k}\right) + T_{slow}\left(m\left(\frac{1}{2}\right)^{k}\right)$$

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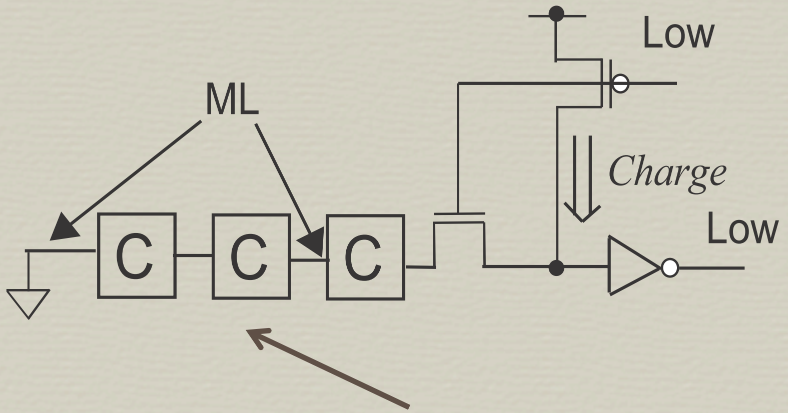
Word Circuit (precharge)

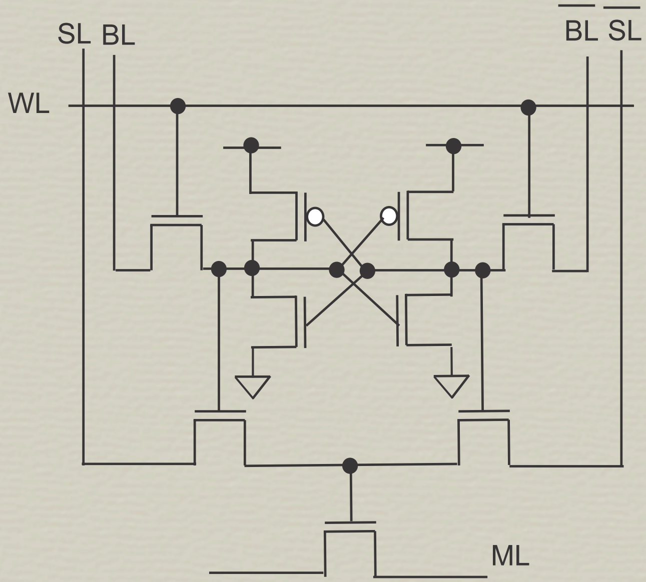
NAND-type word circuit



CAM cell

- Dynamic logic
- Series of pass transistors

NAND-type CAM cell

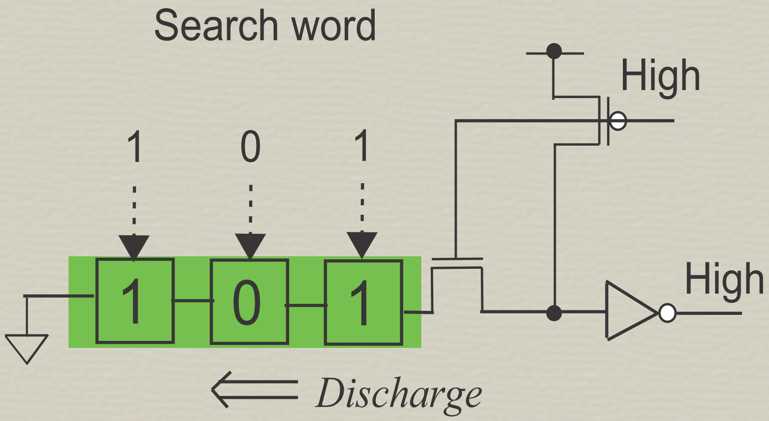


- Match “ON”,
- Mismatch “OFF”

Charge capacitance on match line

Word Circuit (evaluate)

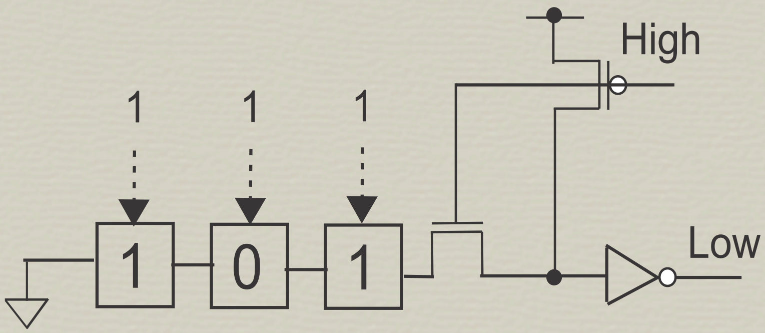
Match operation



Discharging capacitance on match line

➢ Output goes high

Mismatch operation

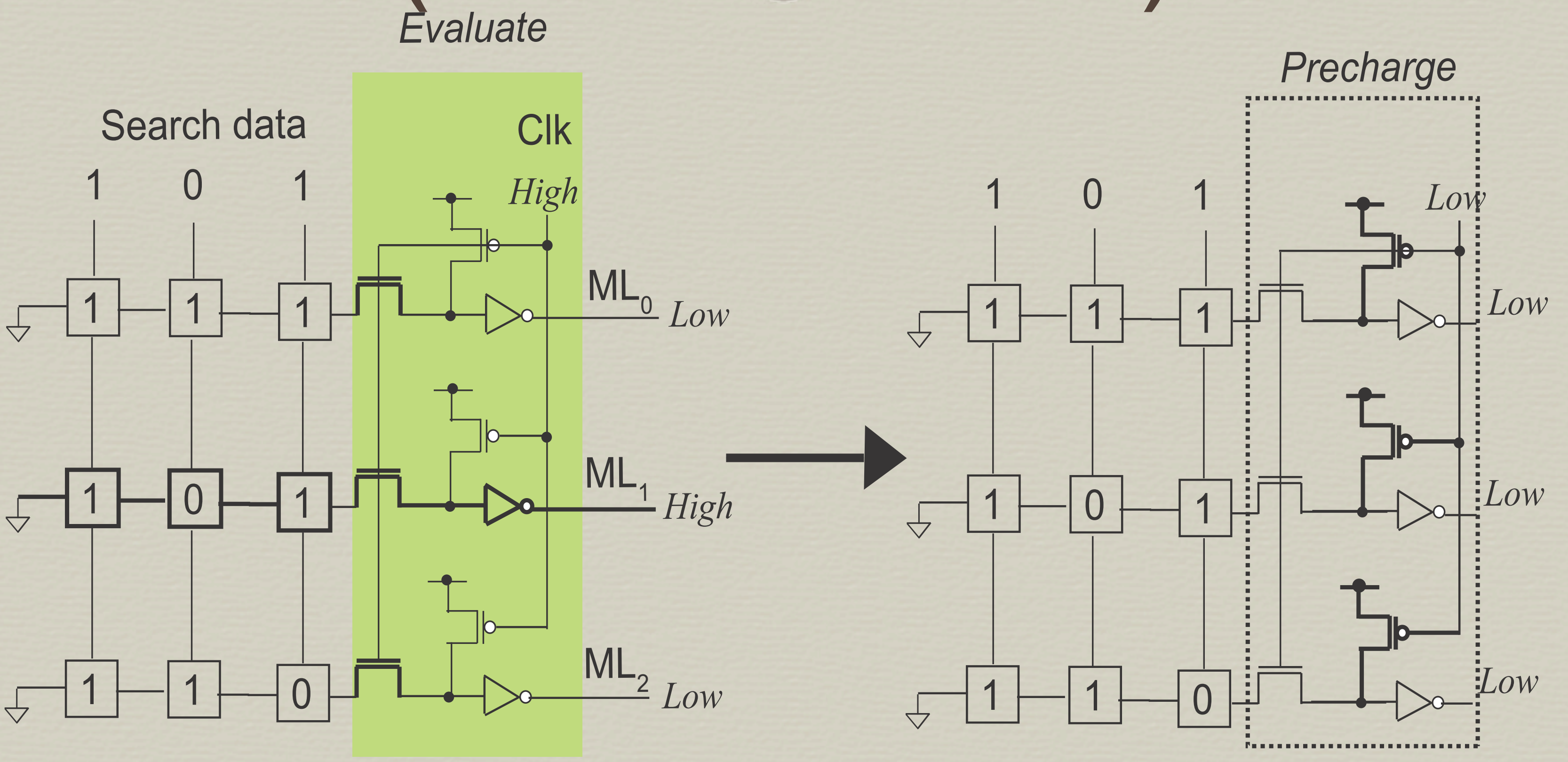


Not discharging

➢ Output remains low

Match line remains high in mismatched case

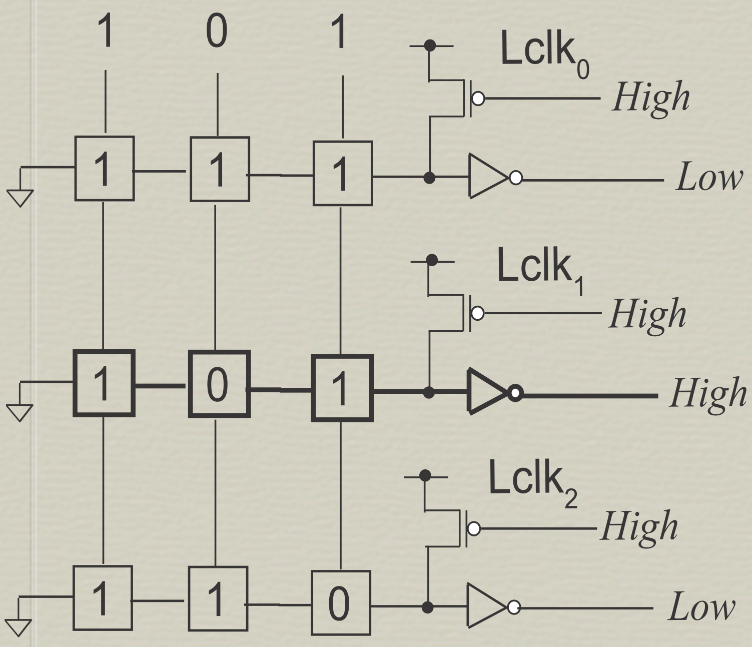
Synchronous Control (conventional)



All word circuits are controlled by a global clock signal

2 phases are required every search

Phase Overlapped Processing (POP)



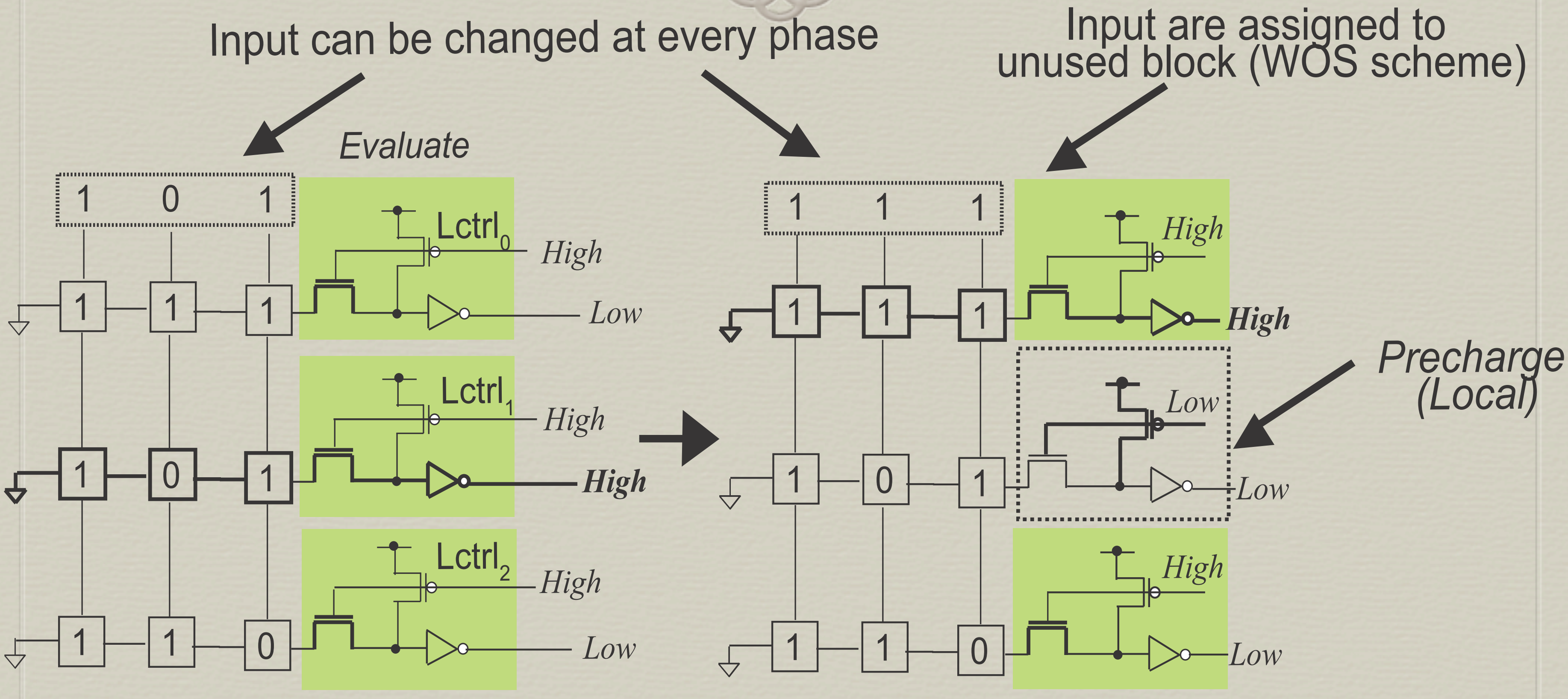
Each circuit is independently controlled using local control signals

- Matched word circuit
  Move on to precharge phase
- Mismatched word circuit
  Stay in evaluate phase

➔Lowering switching activity of pre-charging signals

Mismatched blocks always process new word

WOS based POP



Unused block can process without waiting precharge phase

Searching words requires just 1 phase

Throughput Ratio

Conventional $T_{CS} = 2T_{SS} = 2(T_{reg} + T_{1st} + T_{2nd})$

Proposed

$$T_{CA} = T_{SA} = T_{1st}\left(1 - m\left(\frac{1}{2}\right)^{k}\right) + T_{slow}\left(m\left(\frac{1}{2}\right)^{k}\right)$$

$$\cong T_{1st}$$

$$Throughput \quad ratio = \frac{T_{CS}}{T_{CA}} = \frac{2(T_{reg} + T_{1st} + T_{2nd})}{T_{1st}}$$

T_{SS} Synchronous search delay (evaluate phase)

T_{SA} Asynchronous search delay

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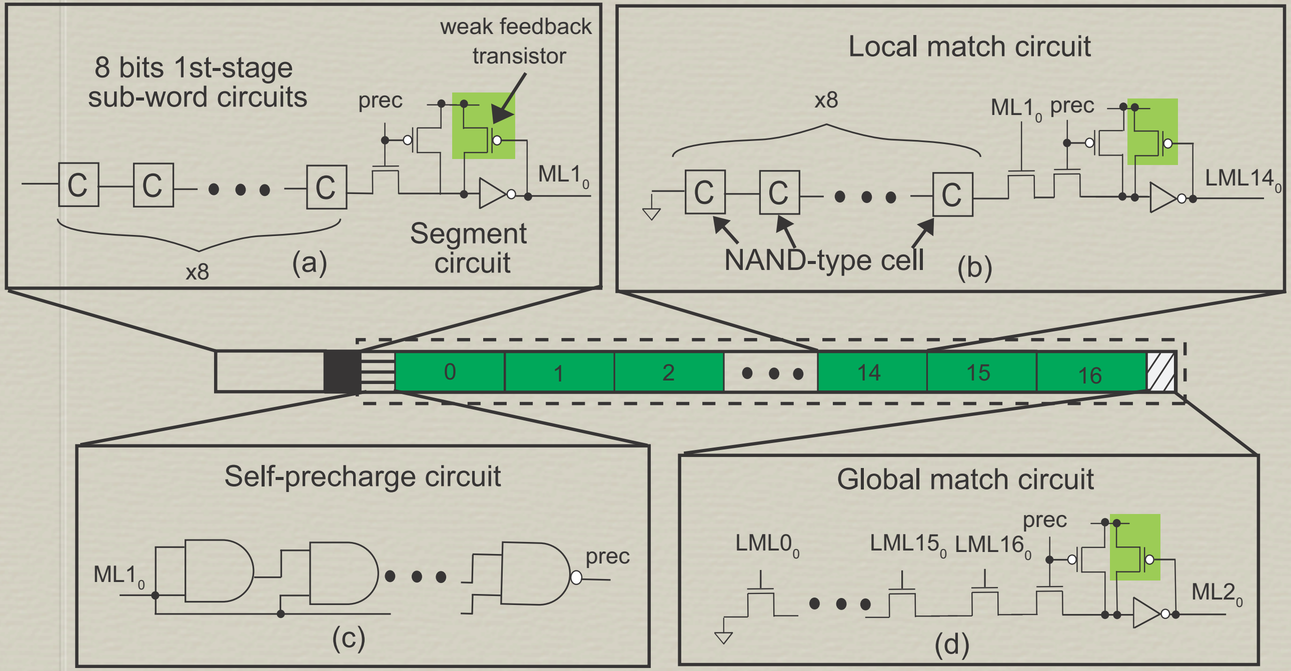
Circuit Implementation

- 144-bit CAM word block with self-precharge circuit
- Self-precharge circuit pre-charges after 2nd stage is complete.
- Hierarchical 2nd stage block (17 local and 1 global match circuit)



Store local matched result

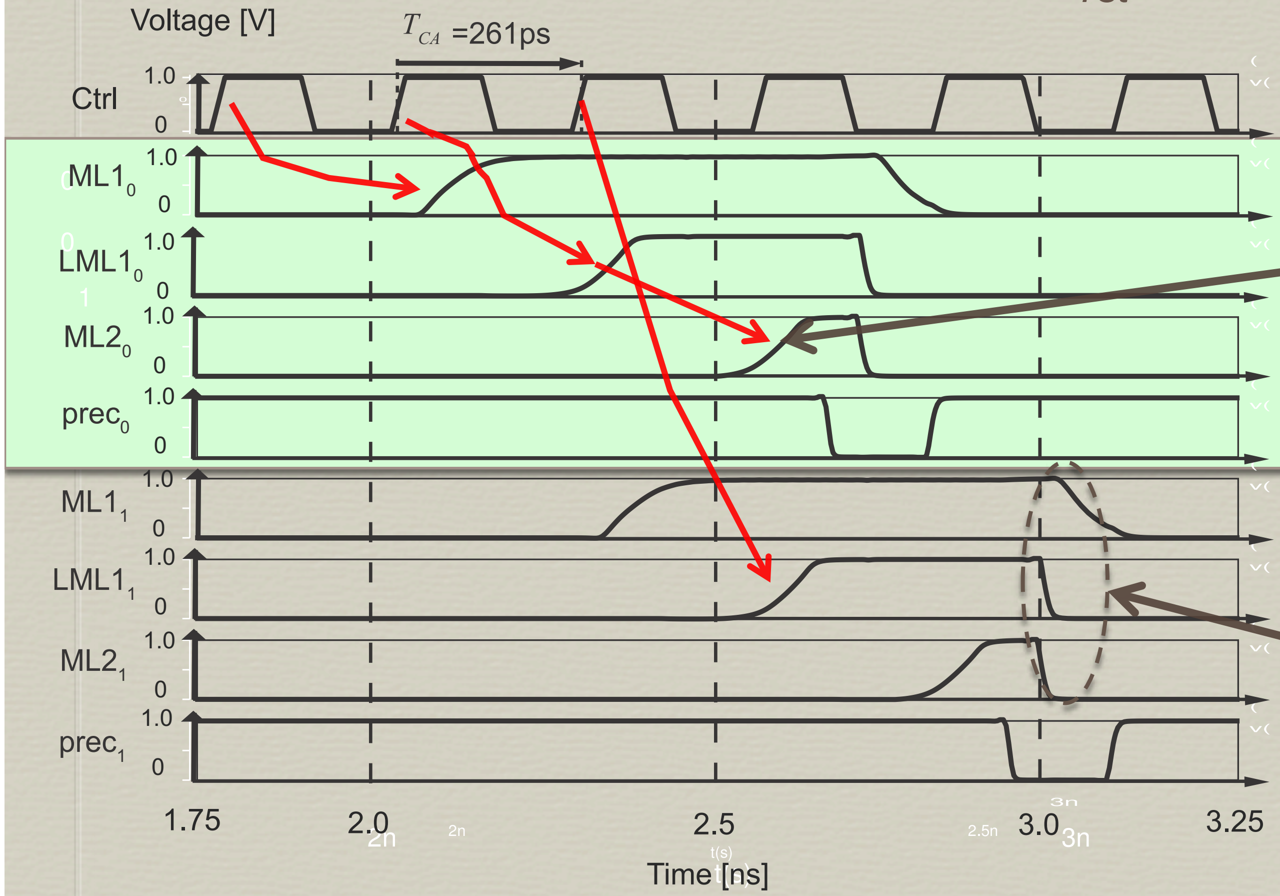
↓

It isn’t affected by input changing

Self-precharge circuit controls its word circuit

Simulated Waveforms

CAM operates based on T_{1st} (259ps)



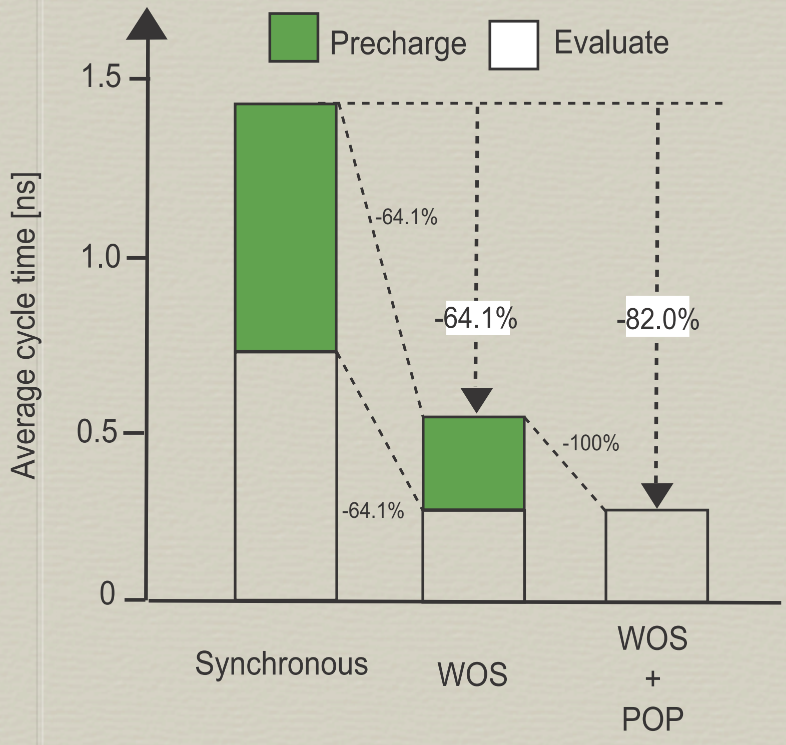
Global match circuit uses only local matched result.

After search is complete,
self pre-charging is locally done.

HSPICE simulation under a 90nm CMOS technology

Performance Comparison

256-word 144-bit binary CAM@90nm CMOS

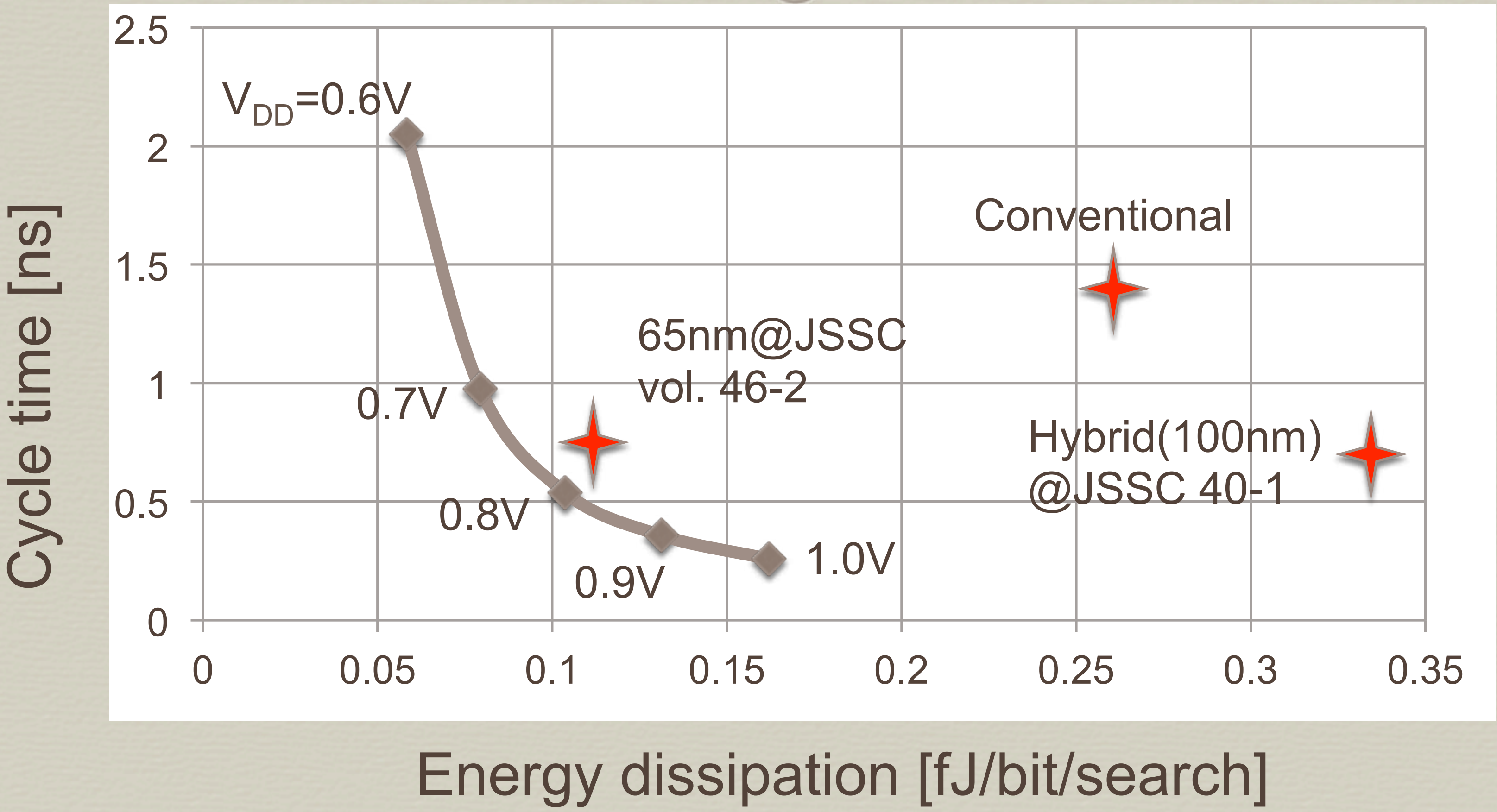


		Conventional	Proposed
Cycle delay [ps]		1454	261
Energy [fJ/bit/search]	Match	0.0003	0.0006
	Search	0.160	0.160
	Control	0.103	0.001
	Total	0.263	0.162
Area [Trs.]		372K	408K

Independent control reduces switching activity of pre-charging

5.57x throughput and 38% energy saving

Performance Comparison



Better energy-delay product

Conclusion

High-throughput low-energy CAM

- Word overlapped search
  - Use unused word block
  - Assign based on pre-computation
- Phase overlapped search
  - Independent control of each word block
  - Search without waiting for precharge
  - ➢ 5.57x throughput, 38% energy saving, 8% cost of area

Future Prospects

- Circuit design considerations
  - Number of partitions
  - Timing robustness
- Extend to Ternary CAM (TCAM)
  - Redesign input controller
- Application specific design
  - Cache (TLB), virus checker