A Digital Neurosynaptic Core Using Event-Driven QDI Circuits

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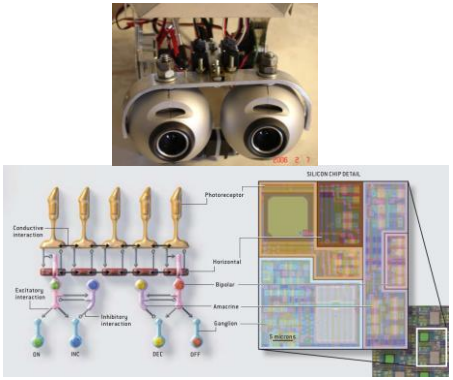
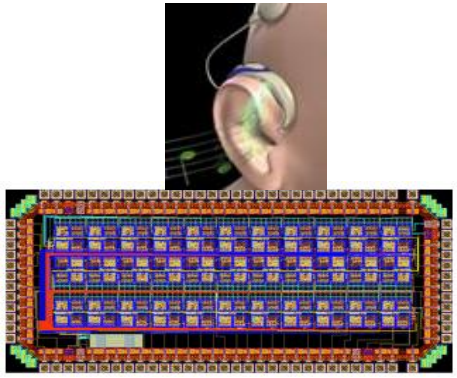
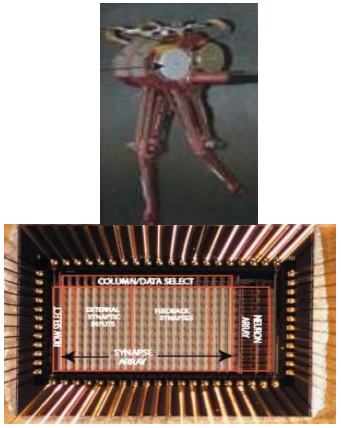
CSL

AVLSI

Neuromorphic VLSI



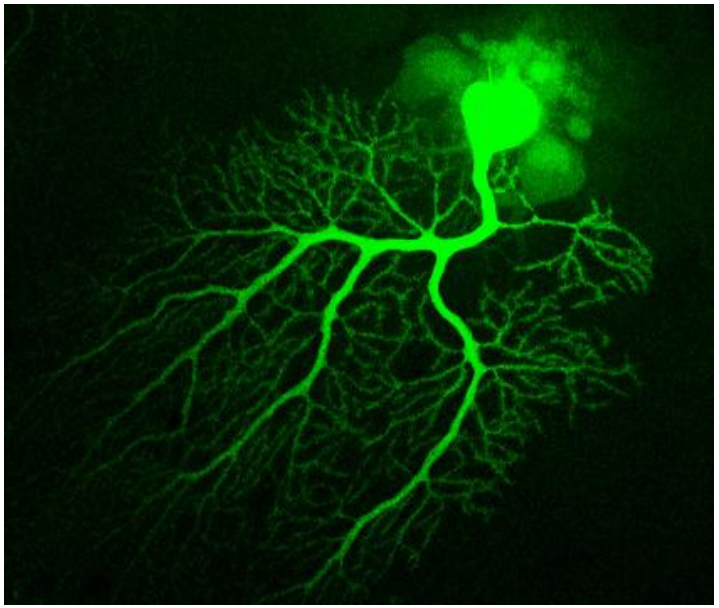




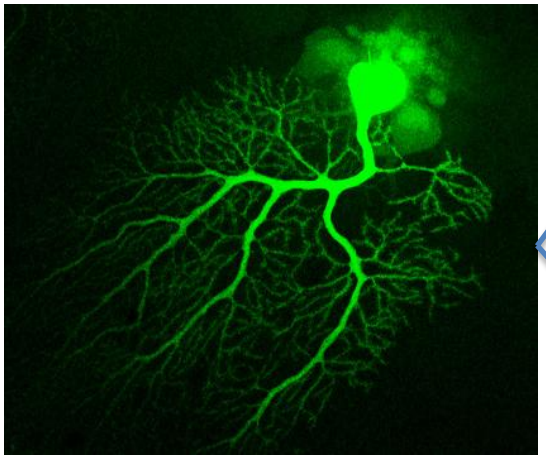
- Biological nerve cell models in silicon
- Real-time, low-power operation
  - Commercial and medical applications
  - Tools for brain science

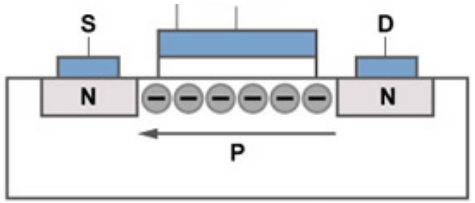
Spiking Neural Networks

- Neuron
- Dendrites (inputs)
- Axon (output)
- Synapses (connections)



Models in Silicon



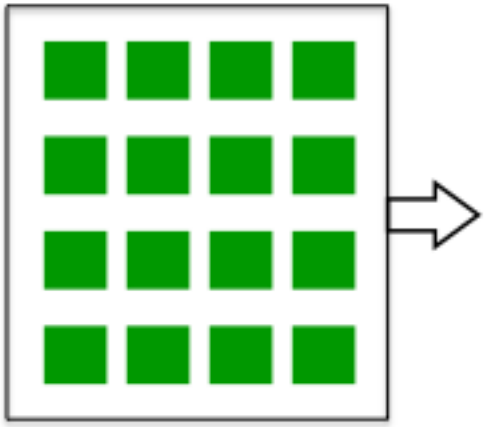


Analog Circuits

Differential Equations
(e.g. Hodgkin-Huxley,
Integrate-and-Fire, etc)

- Computatation
  - Intrinsic properties
  - Network connectivity
- Efficiency
  - ~100^9 neurons and ~100^{12} synapses in the human brain
  - 20 W Power
  - 2 L Volume

Implementation Challenges



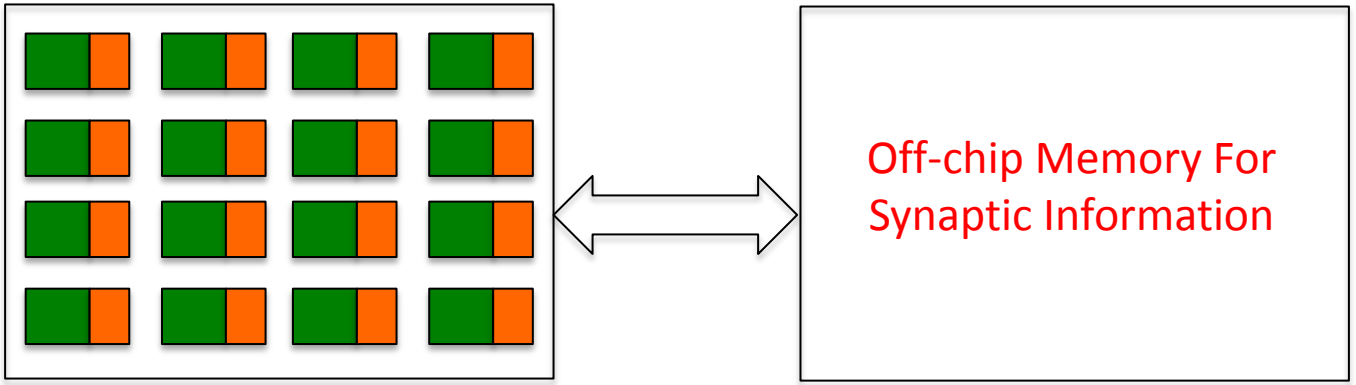
$$v' = 0.04v^2 + 5v + 140 - u + I$$
$$u' = a(bv - u)$$

$$\text{if } v \geq +30\ \text{mV}, \qquad \text{then } \begin{cases} v \leftarrow c \\ u \leftarrow u + d. \end{cases}$$

Communication

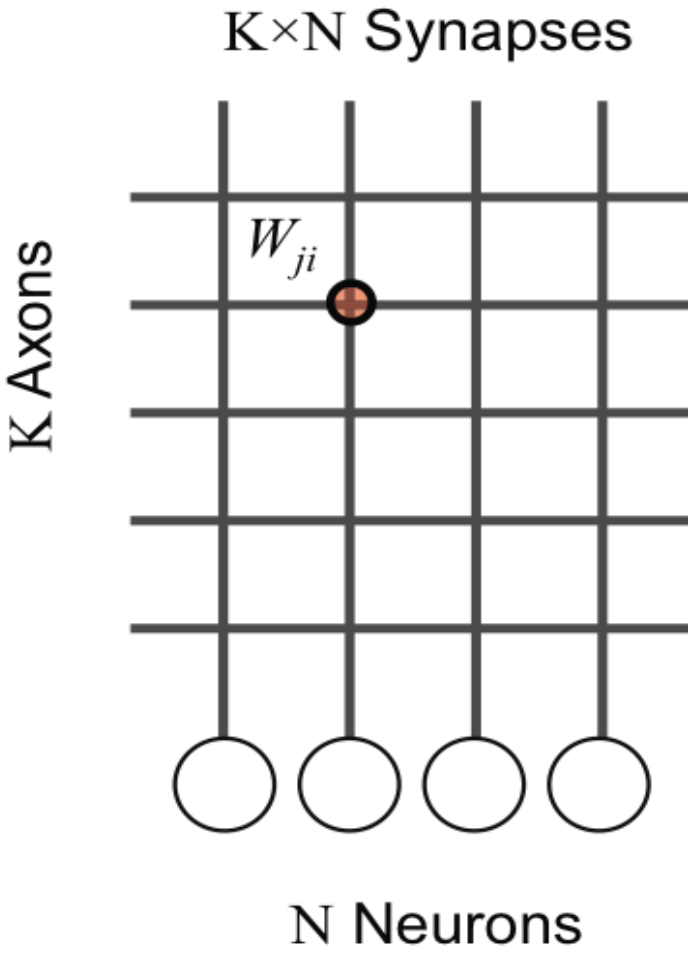
Computation

Memory



Crossbar Synapses

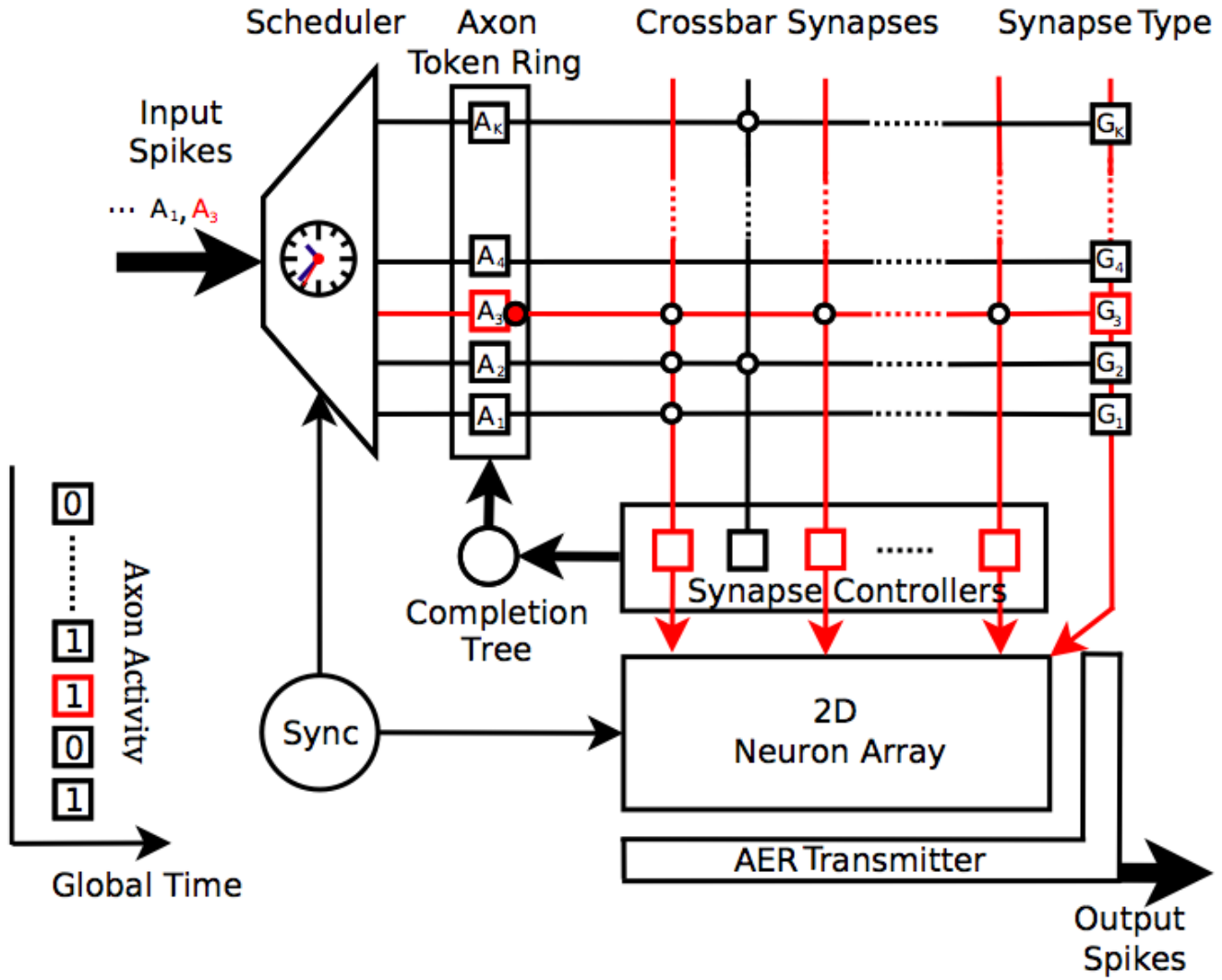
- Integrated Computation and Memory
- Crossbar
  - Rows: Axons
  - Columns: Dendrites
  - Junctions: Synapses
- Flexibility
- Efficiency: Large fanout in one operation



Scalable Neurosynaptic Core

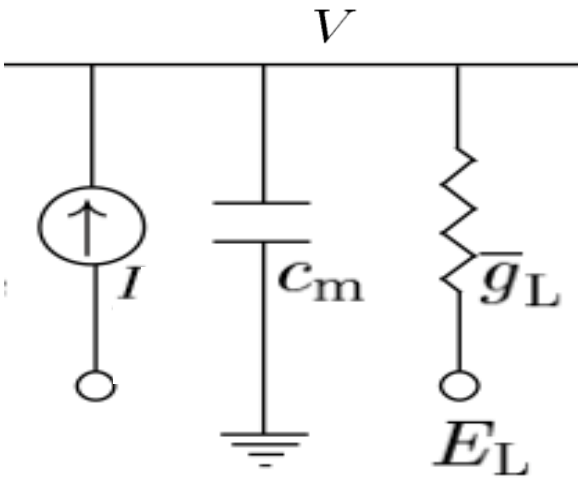
- Crossbar Synapses
- Digital Circuits
  - Deterministic
  - Scalable (45nm SOI)
- Asynchronous design
  - Minimal power dissipation when idle
  - Fast when active
  - Robust
- Scalable to a multi-core/multi-chip system

System Architecture



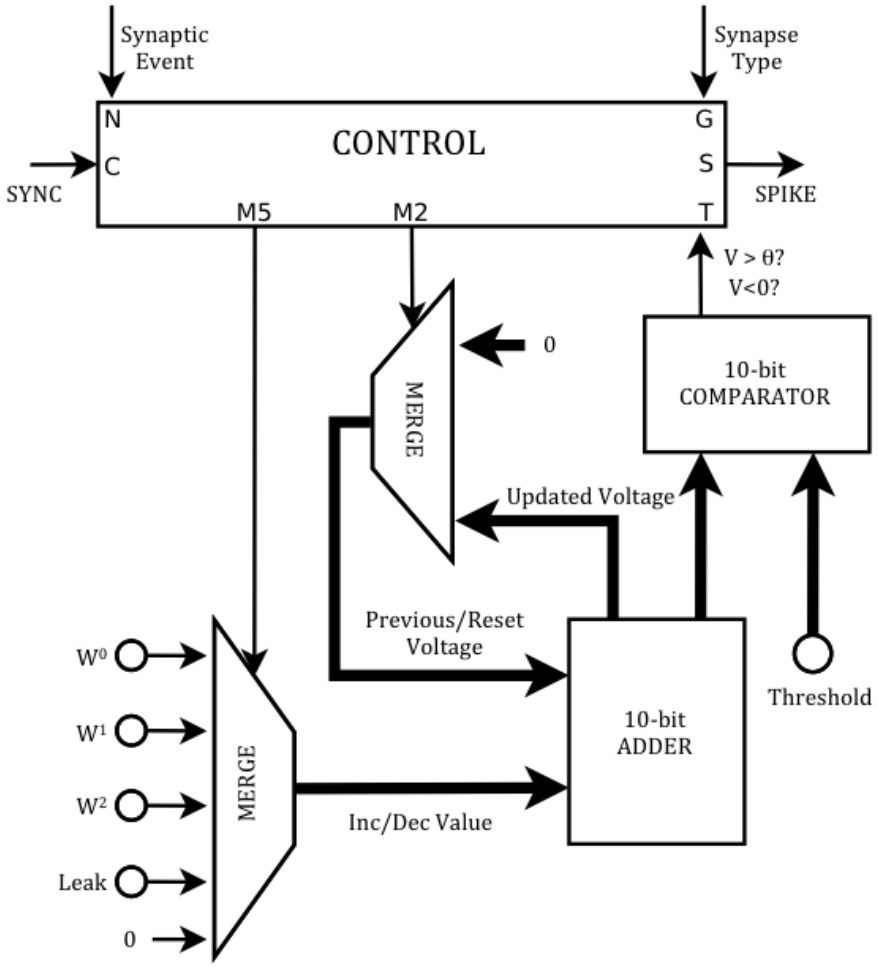
Neuron Model

Leaky Integrate-And-Fire



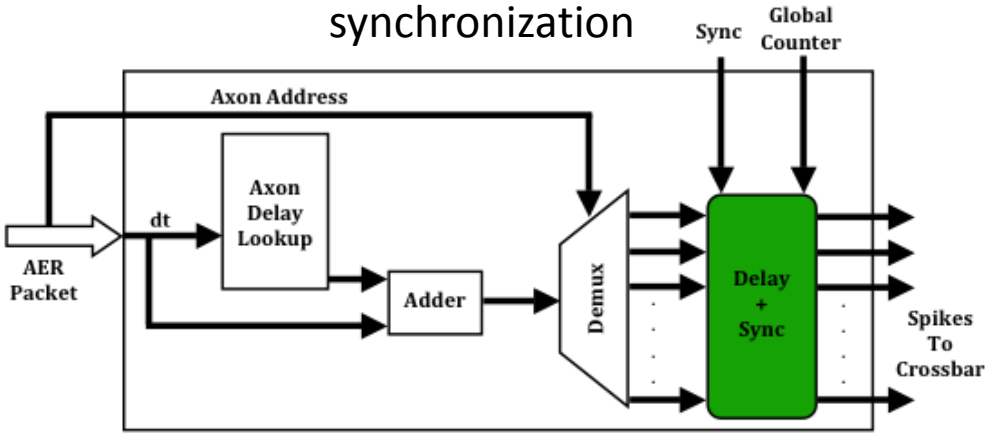
$$V(t+1) = V(t) - Leak + \sum_{j=1}^{k} [A_j(t) \times W_j \times S_j]$$

$$if\ V_i(t) > \theta$$
$$Spike = 1$$
$$V_i(t+1) = 0$$

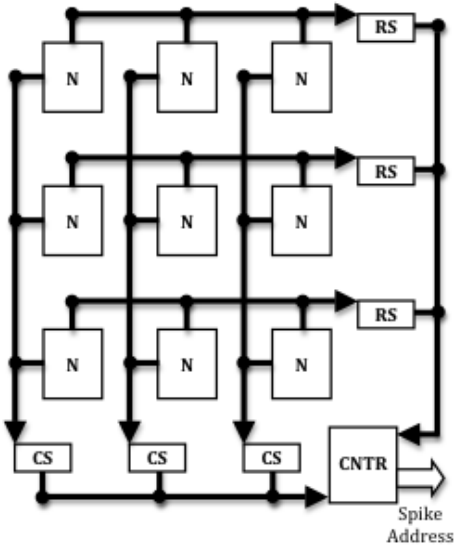


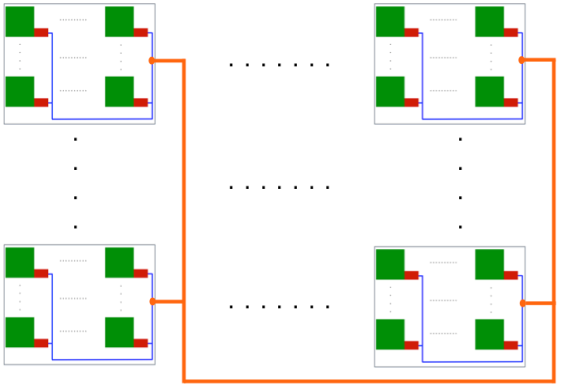
Communication Infrastructure

Scheduler for synchronization



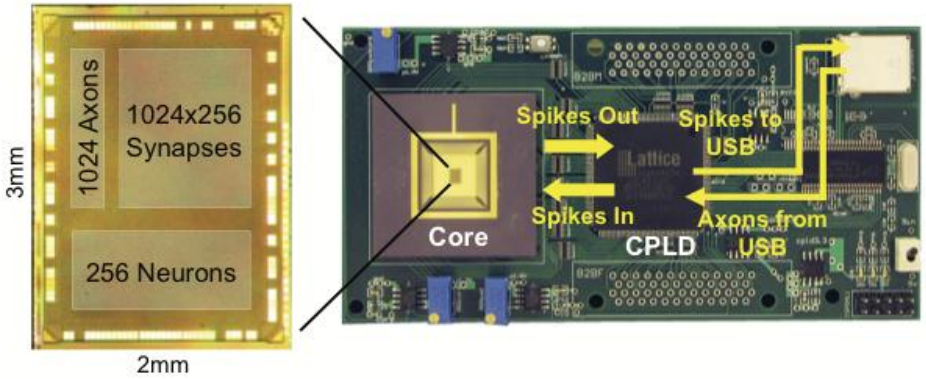
AER transmitter and receiver for fan-out

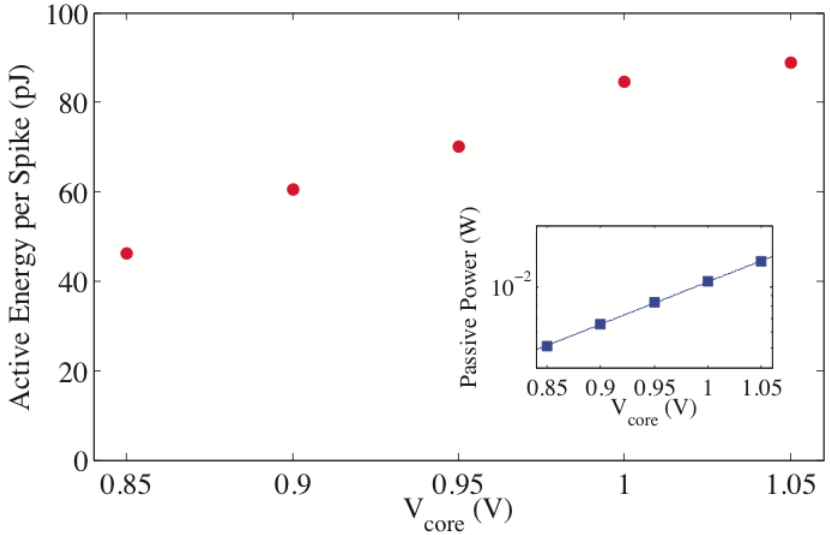


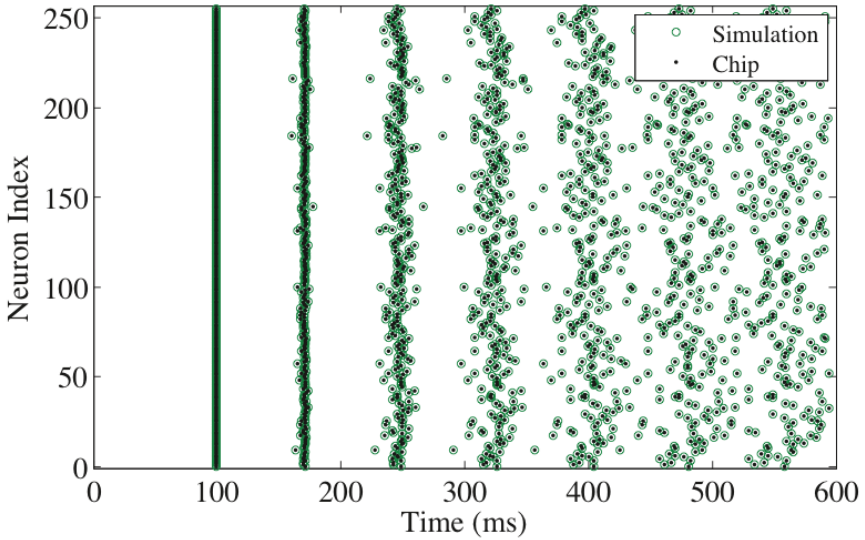


Routing fabric for multi-core communication

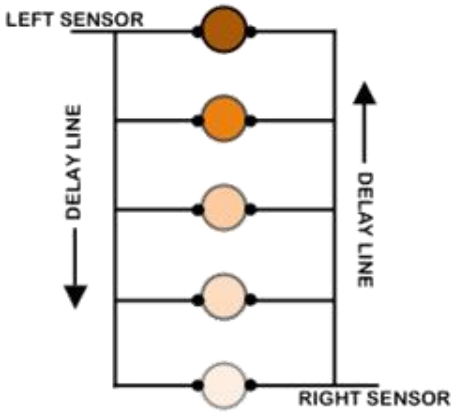
Chip Test

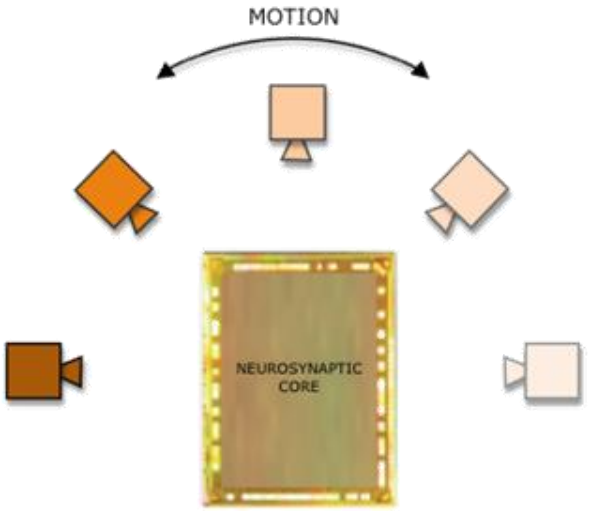

1024 Axons
1024x256
Synapses
256 Neurons
3mm
2mm
Core
Spikes Out
Spikes to
USB
Spikes In
Axons from
USB
CPLD

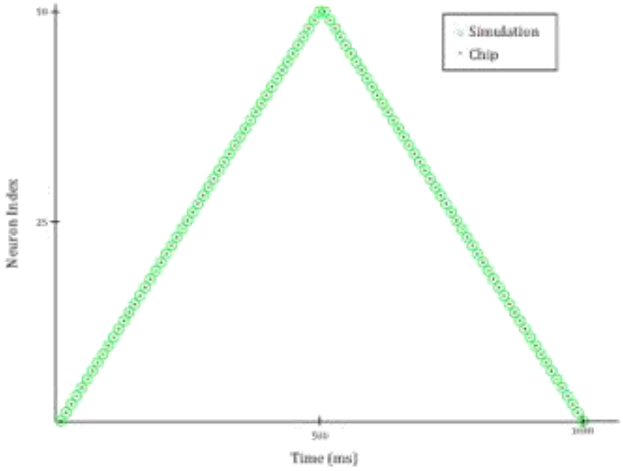

Active Energy per Spike (pJ)
V core (V)
Passive Power (W)
10^-2
V core (V)


Simulation
Chip
Neuron Index
Time (ms)

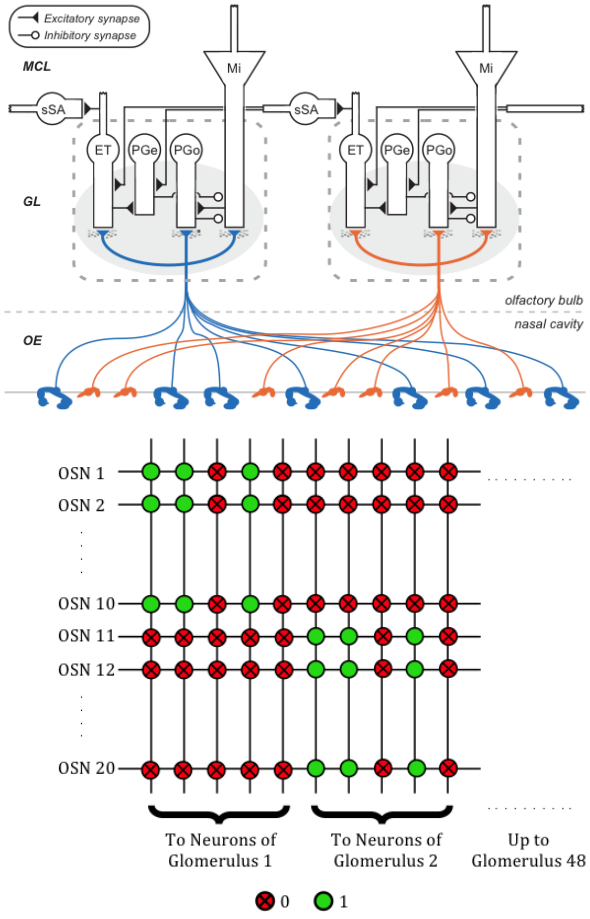
Example Application:
Sound Localization

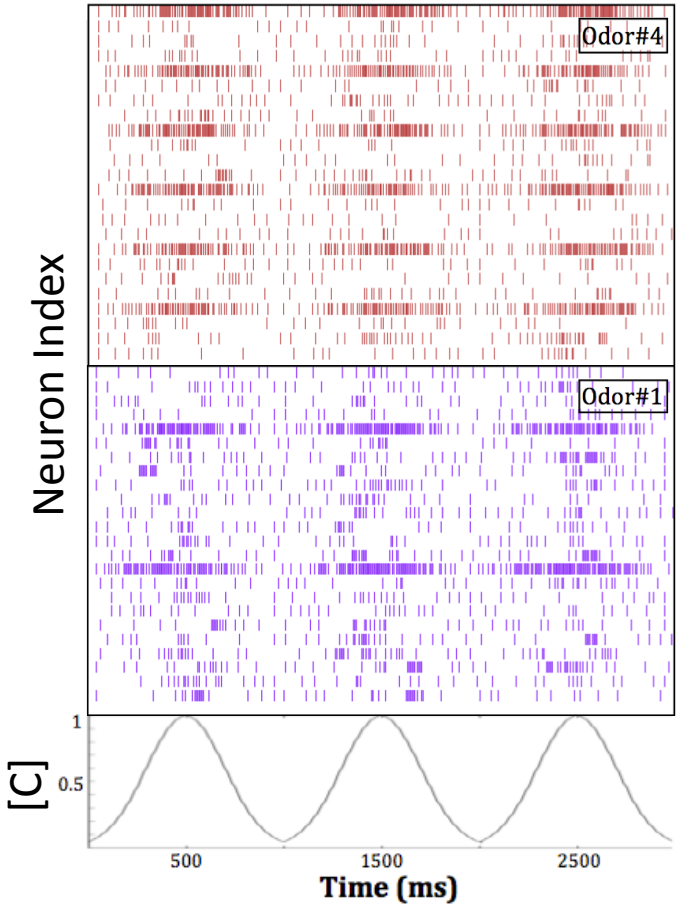






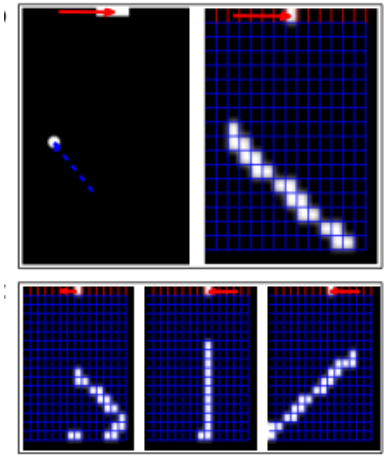
Example Application:
Odor Recognition



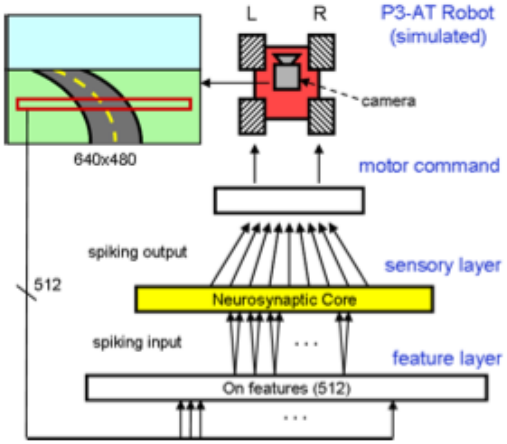


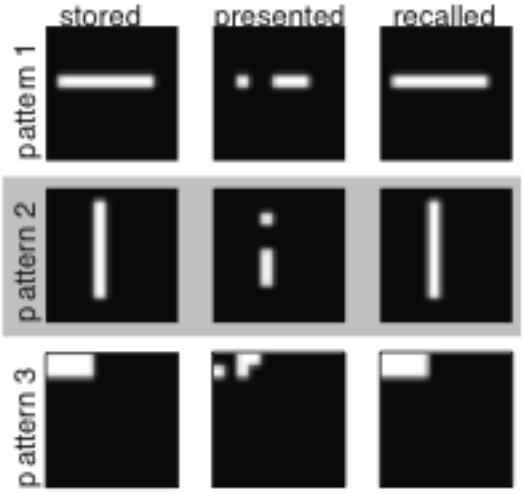
Example Applications

Pong!



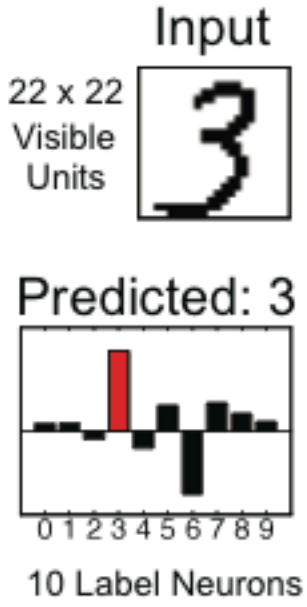
Motor Control





Auto-associative Memory

Visual Recognition



Conclusion

- Neurosynaptic Core
  - Digital Asynchronous Circuits
  - Crossbar synapses
  - Scalable to multiple cores and multiple chips
- Applications
  - 1-1 hardware-software correspondence
  - Sensory-motor activity
  - Bio-inspired solutions to technological problems

A Digital Neurosynaptic Core Using Event-Driven QDI Circuits

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