Statistical Analysis and Optimization of Asynchronous Digital Circuits

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Outline

• Motivation
• Variability model of CMOS digital circuit
• Performance model for different timing schemes
• Performance comparison
• Conclusion
Variability Continues to Increase as Technology and Voltage Scales Down

Device variability vs. Technology node

- Higher variability with finer design rules and larger wafers
- Higher variability with lower supply voltages

[Cao, ASU]
Circuit Performance Characteristics with Different Timing Schemes

- Self-timed circuit is a variation-monitoring circuit by itself
- Becomes advantageous when the variation is large ($B > A$)
- Statistical analysis framework is necessary

- Probability
- Computation Delay

- Self-timed circuit
- Original circuit
- Conventional synchronous circuit

- A: protocol circuit delay
- B: $3\sigma$ delay variation
Statistical Analysis Framework

Circuit Variability Model
- Supply voltage
- Logic depth
- Width and length
- Body bias

Performance Model
- Computation overhead
- Communication overhead
- Delay and energy performance

Determine the optimal timing strategy in the presence of variability
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Delay Model of CMOS Digital Circuit

- One unified current model across different operating regions
- Model error <2% from 0.3V to 1V
Delay Variability Model

\[ \frac{\sigma_{T_d}}{\mu_{T_d}} = \sqrt{\left( S_{T_d}^{V_{th}} \right)^2 \cdot \left( \frac{\sigma_{V_{th}}}{\mu_{V_{th}}} \right)^2 + \left( S_{T_d}^{K} \right)^2 \cdot \left( \frac{\sigma_{K}}{\mu_{K}} \right)^2} \]

\[ S_{T_d}^{V_{th}} = \frac{\partial V_{th}}{\partial T_d} \frac{V_{th}}{T_d} \]

\[ S_{T_d}^{K} = \frac{\partial K}{\partial T_d} \frac{K}{T_d} \]

Threshold voltage

Geometry

Within die variation (WID)
“Local mismatch”

Die-to-die variation (DTD)
“Global variation”
Delay Variability Model

Model error <8% from 0.3V to 1V
Local mismatch dominates at low supply voltages
Delay Variability Model with Different Logic Depths

- Use 4-stage inverter chain model as baseline model
- Model error <13% for n=8 and <15% for n=24
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• Assumption: Process variation follows Gaussian distribution
• Dual-rail approach: have only protocol overhead but no delay overhead
• Synchronous approach: have only delay overhead

For 99.7% yield: 
\[ D_{sync} = \frac{3\sigma_{logic,total}}{\mu_{logic,total}} \]
Bundled-Data Self-Timed Approach

Assume main data path and replica delay line exhibit similar statistics:

For 99.7% yield:  

\[ D_{\text{bundled-data}} = D_{\text{variation}}^2 \left( 0.5 + \sqrt{0.25 + \frac{2}{D_{\text{variation}}^2}} \right) \]

where  

\[ D_{\text{bundled-data}} = \frac{\mu_{\text{delay-line}} - \mu_{\text{logic}}}{\mu_{\text{logic}}} \quad \text{and} \quad D_{\text{variation}} = \frac{3\sigma_{\text{logic,WID}}}{\mu_{\text{logic,WID}}} \]
Bundled-Data Delay Overhead

\[ D_{\text{bundled-data}} \propto \begin{cases} \sqrt{2} \cdot D_{\text{variation}}, & \text{when } D_{\text{variation}} \to 0 \\ D_{\text{variation}}^2, & \text{when } D_{\text{variation}} \to \infty \end{cases} \]

*Delay overhead becomes much larger as process variability increases!*
**Performance Model under Variations**

**Original delay and energy model**

\[
\begin{align*}
T_{\text{comp}} &= T_{\text{delay}} \\
E_{\text{dynamic}} &= \alpha C_{\text{switch}} V^2 \\
E_{\text{leakage}} &= VI_{\text{leakage}} T_{\text{delay}} \\
E_{\text{total}} &= \alpha C_{\text{switch}} V^2 + VI_{\text{leakage}} T_{\text{delay}}
\end{align*}
\]

**Statistical delay and energy model**

\[
\begin{align*}
T_{\text{comp}} &= T_{\text{delay}} (1+P+D) \\
E_{\text{dynamic}} &= \alpha C_{\text{switch}} (1+P)V^2 \\
E_{\text{leakage}} &= VI_{\text{leakage}} (1+P) T_{\text{delay}} (1+P+D) \\
E_{\text{total}} &= \alpha C_{\text{switch}} (1+P)V^2 + VI_{\text{leakage}} (1+P) T_{\text{delay}} (1+P+D)
\end{align*}
\]

<table>
<thead>
<tr>
<th>Timing scheme</th>
<th>Synchronous</th>
<th>Bundled-Data</th>
<th>Dual-Rail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay Overhead (D)</td>
<td>$D_{\text{sync}}$</td>
<td>$D_{\text{bundled-data}}$</td>
<td>0</td>
</tr>
<tr>
<td>Protocol Overhead (P)</td>
<td>0</td>
<td>$P_{\text{bundled-data}}$</td>
<td>$P_{\text{dual-rail}}$</td>
</tr>
</tbody>
</table>

- Evaluate computation delay and energy under variations
- Overhead changes with supply voltage and logic depth
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Global variation affects only synchronous approach
Local mismatch dominates at low supply voltages
Local mismatch has less impact on longer critical path

4-stage FO4 INV chain

24-stage FO4 INV chain

- Global variation affects only synchronous approach
- Local mismatch dominates at low supply voltages
- Local mismatch has less impact on longer critical path
• Assumption: $P_{\text{bundled-data}} = 1T_{\text{FO4}}$; $P_{\text{dual-rail}} = 2T_{\text{FO4}}$
• Synchronous scheme is better for small critical path at high supply voltages
• Dual-rail scheme is better for large critical path at low supply voltages
Energy Performance Comparison

24-stage FO4 INV chain

- Synchronous scheme is better for high activity at high supply voltages
- Dual-rail scheme is better for low activity at low supply voltages
- Leakage dominates for low activity at low supply voltages
Conclusion

• A statistical analysis framework is proposed to evaluate performance of CMOS digital circuit in the presence of process variations.

• Designer can efficiently determine the optimal timing strategy, pipeline depth and supply voltage based on the proposed variability and statistical performance models.

• Asynchronous design exhibits better energy and delay characteristics for circuits with low activity and larger critical path delay under process variations.
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