02200 - Digital design and computer organization (Fall 2004)

SYLLABUS etc. (Version: 27 August 2004)

Introduction

The aim of the course is to provide the participants with: (1) in depth knowledge on basic computer organization and (2) structured and systematic design of digital circuits and systems using the hardware description language VHDL. The course is based on a textbook on computer organization and design, supplemented with a VHDL-textbook, lecture notes, journal articles, manuals, and data sheets.

In parallel with the lectures, participants will be working (in teams of 2-3 students) on a project in which they design and simulate a simple pipelined 32-bit RISC processor called Mini-MIPS. It is possible to synthesize, implement, and test this design in the subsequent 3-week laboratory course 02201 in January 2005.

Practicalities

Instructors **Hans Holten-Lund**,
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Jens Sparsø,
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Teaching assistants

Tuesday afternoon	NN1
Wednesday afternoon	NN2
Friday afternoon	NN3

For contact details see the course pages on campusnet.

Textbook The course textbook is:

- D.A. Patterson & J.L. Hennessy, "Computer Organization and Design - The Hardware/Software Interface (3rd edition, available august 2004)," Morgan Kaufmann. ISBN: 1-55860-601-1 (Pol. bookstore: 565 DKK - 10 % student discount).

In addition it is *highly recommended* that you get yourself a textbook on VHDL. A fine and comprehensive one is:

- Peter J. Ashenden, "The Designers Guide to VHDL, 2nd Edition" Morgan Kaufmann, 2001. ISBN 1-55860-674-2 (Pol. bookstore: 695 DKK - 10 % student discount).

NOTE: The university bookstore has a favorable offer. They are selling "Computer Organization and Design ..." and "The Designers Guide to VHDL" shrink wrapped into a single package, for a price of only 879 DKK - 10 % student discount.

Location Lectures are in building 308, auditorium 13.
NB: Mondays from 13:00 to 15:00 and Thursdays from **9:00** to 11:00
Labs. are in the E-Databar, building 341, room 003.

Homepage On Campusnet, course 02200, you will find all information about the course. We will update the campusnet-pages on a weekly basis.

Lecture notes The textbook will be supplemented by lecture notes and misc. handouts. You can buy the notes in the IMM bookshop in in the corridor between buildings 304 and 305. The opening hours are as follows: 1st week of the semester: each day from 9h:00 to 14h:00; 2nd week of the semester: each day from 12h:00 to 14h:00; following weeks: only Monday and Tuesday from 12h:00 to 13h:00. The price is 80 kr. (This is cheap. We are selling notes printed last fall or this spring, and we are not charging you for the many pages with copies of old exam problems, as they are also available on campusnet).

Homework Every week a set of homework problems will be posted. The solution will be discussed during the Thursday lecture in the following week.

Lab-sessions There will be no compulsory lab-sessions. You will have to work and think on your own.

For students who are not familiar with VHDL and the ModelSim VHDL simulator we will organize 3 introductory lab-sessions. These lab-sessions are highly recommended and we may not be prepared to offer help on VHDL later in the course if you did not complete these lab-sessions. Register your team for either Tuesday, Wednesday, or Friday afternoon (13h:00 to 17h:00). These lab sessions take place in weeks 38, 39 and 40, (see lecture plan on the following page).

Design project You will be working in teams of two students. Find a partner you like to work with. You must register your team no later than September 16, 2004. Room 003, in building 341 (the E-Databar) is reserved for course 02200 on Tuesday, Wednesday and Friday afternoons throughout the semester. You may also install the free Xilinx ISE WebPACK and ModelSim XE Starter VHDL tools on your own PC and work at home. These tools can be downloaded from the Xilinx webpage free of charge. Go to: `www.xilinx.com` – Products – ISE Design Tools Center – ISE Logic Design Tools – Free ISE WebPACK, and register for the download. Remember to also get the MXE Simulator. For debugging and testing MIPS and Mini-MIPS assembler programs (for example related to Task 1 & 2 of the Mini-MIPS project) the SPIM MIPS simulator is used, see Appendix A in the textbook. PCSpim is available for download at http://www.cs.wisc.edu/~larus/spim.html. In addition is is included in the CD which comes along with the new 3rd edition of the textbook.

Deadlines:

1. The behavioral specification of the Mini-MIPS (Task 1) should be completed as early as possible and no later than Friday, October 22, 2004.
2. The final report describing and documenting your Mini-MIPS design is due on Friday, December 3, 2004, at 16h:00. Two-person teams are supposed to complete Task 1 and 2 of the Mini-MIPS design project. NB: Three-person teams are expected to also complete Task 3.

Exam (E2-B) Tuesday, December 14, 2004.

The final grade is based on a 4 hour written exam (50%) and a report on the design project (50%). The report and the examination have to be passed separately.

Lecture plan

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02201: Lab Course in January 2005

Following this course (02200) you may continue your Mini-MIPS project in the subsequent 3-week course 02201, which runs in January 2004. In this lab course you will implement and test your Mini-MIPS processor in an FPGA. You will gain experience in logic synthesis and design of real digital systems, and learn how to use FPGAs.

Advanced computer architecture course at DIKU, Spring 2005

If you are interested in learning more about modern/advanced computer architecture, the Computer Science Department (DIKU) at the University of Copenhagen usually offers a course in the spring semester. This course uses Hennessy and Patterson's advanced textbook, "Computer architecture, a quantitative approach", 3rd ed. For information about the spring 2004 version of the course check: http://www.diku.dk/undervisning/2004f/303/

Lecture plan

This is a tentative lecture plan. Check the course on Campusnet regularly for updates.

Week	L#	Date	Topic	Prof.	Reading	Lab
36	1	30/8	Introduction	JS	[1] Ch. 1	
	2	2/9	Control Structures and Disciplines	JS	[3] Ch. 7	
37	3	6/9	Performance measures and Trade-offs	JS	[3] Ch. 8	
	4	9/9	Introduction to VHDL	HaHL	[2,4]	
38	5	13/9	VHDL simulation and modeling	HaHL	[2,4]	Lab
	6	16/9	VHDL simulation and modeling	HaHL	[2,4]	VHDL
39	7	20/9	Computer Performance	HaHL	[1] Ch. 1, Ch. 4	Lab GCD
	8	23/9	RISC concepts, MIPS ISA + Mini-MIPS project	HaHL	[1] Ch. 2 (briefly)	
40	9	27/9	The processor, single- & multiple cycle	HaHL	[1] Ch. 5.1-4	Lab GCD
	10	30/9	Implementing the Control Unit	HaHL	[1] Ch. 5.5, Ap.C	DUE
41	11	4/10	Pipelining: basics and data hazards	JS	[1] Ch. 6.1-3	Lab Task 1
	12	7/10	Pipelining: Control hazards	JS	[1] Ch. 6.3-7	
42			**Fall break**			
43	13	18/10	Pipeline Interrupts & Performance	JS	[1] 6.8-11	Task 1
	14	21/10	Integer Arithmetic (multiplication and division)	HaHL	[1] Ch. 3.3-5	DUE
44	15	25/10	Floating Point Arithmetic	HaHL	[1] Ch. 3.6-3.7	Lab Task 2
	16	28/10	Memory Systems: The basics of caches	JS	[1] Ch. 7.1-2	
45	17	1/11	Memory Systems: Caches (continued)	JS	[1] Ch. 7.3,7.5	
	18	4/11	Memory systems: Virtual Memory	JS	[1] Ch. 7.4-7.6	
46	19	8/11	Virtual Memory (O.S. related issues)	JS	[1] Ch. 7.4-7.6	
	20	11/11	Interfacing processors and peripherals	HaHL	[1] Ch. 8.1-4	
47	21	15/11	Interfacing processors and peripherals	HaHL	[1] Ch. 8.4-8	
	22	18/11	Extra 1: Parallel Processors	JS	[1] Ch. 9.1-9.4	
48	23	22/11	Extra 2: Multi-processor SoC's using NoC's	JS	Notes	
	24	25/11	Extra 3: FPGA technology	HaHL	Notes	
49	25	29/11	Extra 4: Low-power application-specific processors	JS	Notes	Task 2
	26	1/12	**Course Evaluation, old exam problems**			rep. DUE

Literature:

[1] D.A. Patterson & J.L. Hennessy, "Computer Organization and Design - The Hardware/Software Interface (Third Edition, August 2004)," Morgan Kaufmann.

[2] S.A. Ward & R.N. Halstead, "Computation Structures," MIT Press, McGraw-Hill, 1990. (Chapters 7 and 8, included in the lecture notes.)

[3] Peter J. Ashenden, "The Designer's guide to VHDL, (Second Edition)" Morgan Kaufmann.
(Or equivalent text)

[4] Jan Madsen & Steen Pedersen, "An Introduction to VHDL," ID-U:1993-65. (Included in the lecture notes).

Required reading for the exam (danish: Pensumliste)

Announced later ...