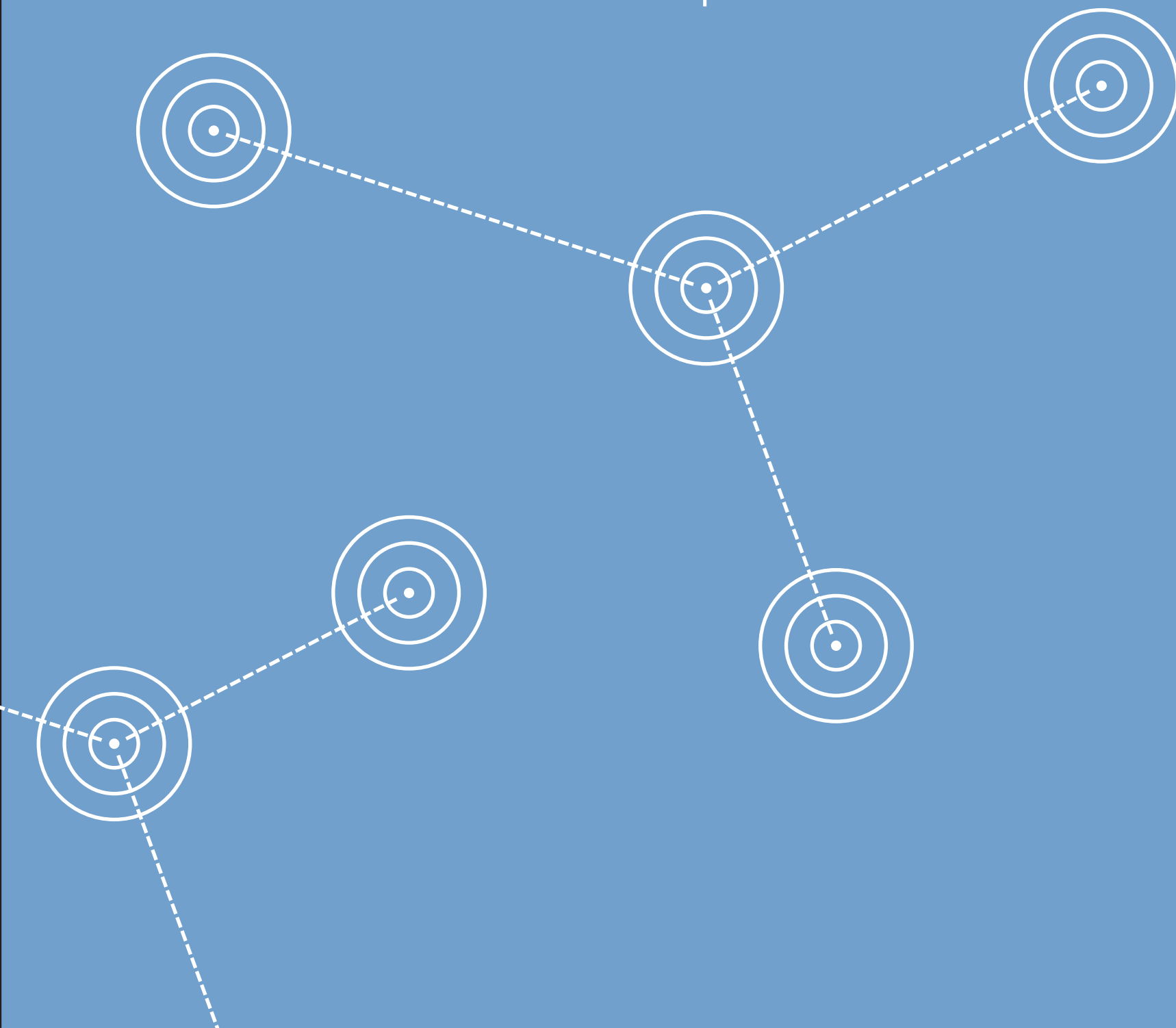


The Thomas B. Thrige Centre for Microinstruments

Report 1997-2002



After more than two years of hard work the chip is finally taped out. Özgün Paker checks the layout and enjoys the feeling of a job well done. Read more on page 4.



Report 1997 - 2002

Purpose The Thomas B. Thrige Centre for Microinstruments is an externally funded research project at DTU hosted by Informatics and Mathematical Modelling. The purpose of the centre is to perform research into methods and technologies for the design of electronic systems which integrate digital, analog and micromechanical components and embedded software in a single chip – a so-called “microinstrument” – which can accomplish signal acquisition, signal processing, data processing, communication and actuation. By now, terms such as “microsystem” or “system-on-chip” have been accepted as denominations for this area of research. Two examples of microinstruments are (1) a hearing aid, complete with microphone, loudspeaker, electromechanical clock-oscillator etc., implemented on a single chip, and (2) an intelligent pill, which can perform analyses and transmit results on its way through the human digestive system.

Funding The centre was originally set up as a result of a donation of 5 million Danish crowns from the Thomas B. Thrige Foundation and further donations from the companies Oticon, Widex, GN Resound and Microtronic (now Sonion MEMS). Subsequently, a number of companies, institutions, university departments and some research projects have contributed to the co-funding of a series of Ph.D. projects. In addition to those companies already mentioned, the contributors involved have been B-K Medical, the Center for Fast Ultrasound Imaging at Ørsted•DTU, Mikroelektrocentret, 3D Lab, Århus Kommunehospital, the IT University of Copenhagen, the Royal Veterinary and Agricultural University and the Graduate School in Microelectronics, which has co-funded 5 Ph.D. projects via a grant from the Danish Research Training Council (FUR). In total, the activities of the centre have involved funding and running 8 Ph.D. projects and a series of related activities, and the overall budget has been 10 million Danish crowns.

Centre Management and Board As a large proportion of the activities have been funded through private donations, the centre was organised as an institution with an external board. When the centre was founded in 1997, its management was in the hands of:

Board members:

Per Borggaard, Senior Vice President, Terma Elektronik
(chairman of the board 1997-1999)

Nikolai Bisgaard, Senior Vice President, GN ReSound
Professor Knut Conradsen, Pro-rector, DTU

Head of centre:

Professor Jørgen Staunstrup

Board members:

Nikolai Bisgaard, Senior Vice President, GN ReSound
(chairman of the board 1999-2002)

Erik B. Rasmussen, M.Sc. EE.
Professor Knut Conradsen, Pro-rector, DTU

Head of centre:

Associate Professor Jens Sparsø, DTU

Research projects and results

The original plans for the centre were to focus on a small number of research areas and to establish an interdisciplinary demonstration project. It turned out to be difficult to man the demonstration project, amongst other things because in 1997-98 the microelectronics and IT industries were in a period of expansion. At the same time, the so-called "1/3 Ph.D. scholarships", where the Danish Research Training Council, a private company and (for example) a research project all collaborate to fund a Ph.D. project, turned out to be a great success.

As time went by, it was therefore decided to focus more on carrying out a series of Ph.D. projects which attack a number of the problems associated with the implementation of microinstruments. Thus in the end the centre's activities consisted of the following 8 Ph.D. projects, which fall into two main areas:

- Digital integrated circuits and computer-based systems with focus on optimisation of speed, energy consumption and effective use of resources.
 1. Özgün Paker, *Low power digital signal processing*.
 2. Hans Holten-Lund, *Techniques for medical 3D visualization, image-processing and simulation*.
 3. Ken Friis Larsen, *Programming Languages for Embedded Software*.
 4. Borislav Tomov, *Integrated Circuits in Medical Ultrasound*.

- Design and manufacturing techniques for micro-electro-mechanical systems (MEMS).

5. Jacques Jonsmann, *Technology development for micro-actuators*.
6. Morten Ginnerup, *CAD tools for Microsystems*.
7. Ras Kaas Vestergaard, *High-aspect-ratio microstructures*.
8. Arda Deniz Yalcinkay, *Microelectromechanical resonators for low-power, low-voltage systems*.

Most of these projects have now been successfully concluded, or are close to being so. On the following pages, more details are given on the Ph.D. projects which have been carried out.

Apart from the individual Ph.D. projects and their specific results, it is relevant to emphasise that the co-funding model for Ph.D. scholarships has worked extremely well. This in itself represents a considerable success for the centre. Of the 8 projects mentioned above, 5 have been carried out using this funding model. Because the company's contribution is modest, the funding model makes it possible to carry out research which is freer of bindings and which has more long-term aims than would typically be the case with industrial Ph.D. projects, while preserving the application-oriented aspect of such projects.

The projects carried out under the auspices of the centre have demonstrated that companies and universities can profit considerably by collaboration on research projects.

The Future Every research project has a starting and a finishing date. The Thomas B. Thrige Centre for Microinstruments terminates at the end of 2002. As can be seen from the detailed project descriptions on the following pages, the centre's activities involve a number of departments, institutions and companies. Thus the centre has contributed to a strengthening of inter-disciplinary activities and an increase in collaboration in the area of microelectronics in a broad sense.

Experience shows that it is difficult to establish this type of inter-disciplinary project – each individual research worker tends to focus on his own field. This has at times been a challenge, not least during a period with considerable or-

ganisational changes (a new departmental structure at DTU and the foundation of the IT University in Copenhagen). All this is now in place and "the new DTU" intends to go on expanding this area of research: MEMS at Mikroelektronikcentret, analog electronics and RF electronics at Ørsted•DTU and computer-based systems and system-on-chip at the Computer Science and Engineering section at IMM. These DTU departments also collaborate on Ph.D. education in the area of "Microsystems". Thus the future looks quite bright, and the collection of activities which have been carried out under the auspices of the Thomas B. Thrige Centre for Microinstruments has made a significant contribution to our getting this far.

Conclusion The Thomas B. Thrige Centre for Microinstruments has, as stated above, made a strong contribution to the establishment of inter-disciplinary activities within microelectronics in a broad sense, and to the establishment of fruitful relations between DTU on the one hand and external collaborators on the other. This combination of inter-disciplinary activity and collaboration between industry and academia is here to stay!

As the lifetime of the centre reaches its end, there is thus every reason to thank the Thomas B. Thrige Foundation for the very large donation which was the basis for the establishment of the centre. We should also like to use this opportunity to thank the numerous companies, institutions and individual persons who have contributed to the concrete activities which have been carried out.

Jens Sparsø
*Associate Professor, Head of Centre
Informatics and Mathematical Modelling, DTU*

Low Power Digital Signal Processing

Project data

Ph.D. student

Özgün Paker

Period

September 1998 - June 2002

In collaboration with

Oticon A/S

Sponsors

The Danish Research Training Council (FUR), Oticon A/S, and the Thomas B. Thrige Foundation

Host institution

Informatics and Mathematical Modelling, DTU

Supervisor

*Associate Professor
Jens Sparsø*

Project description

This Ph.D. project is concerned with the architecture and design of a platform (i.e. a chip) for digital signal processing at audio frequencies. The aim has been to develop a solution which is programmable and which at the same time has a very low energy consumption. These two targets cannot normally be reached simultaneously. Thus a standard signal processor (DSP) which is programmed to perform a given algorithm has an energy consumption which is several orders of magnitude larger than a dedicated circuit which implements the same algorithm.

In the Ph.D. project, a solution has been developed which can be characterised as a heterogeneous multiprocessor on a chip. The solution is made up of a number of small algorithm-domain specific processors, one or more standard processors and/or signal processors, and a packet switched

communication network. The idea is that computationally intensive tasks are run on the domain specific processors, while the less computationally demanding and more non-regular tasks are run on the general-purpose processors.

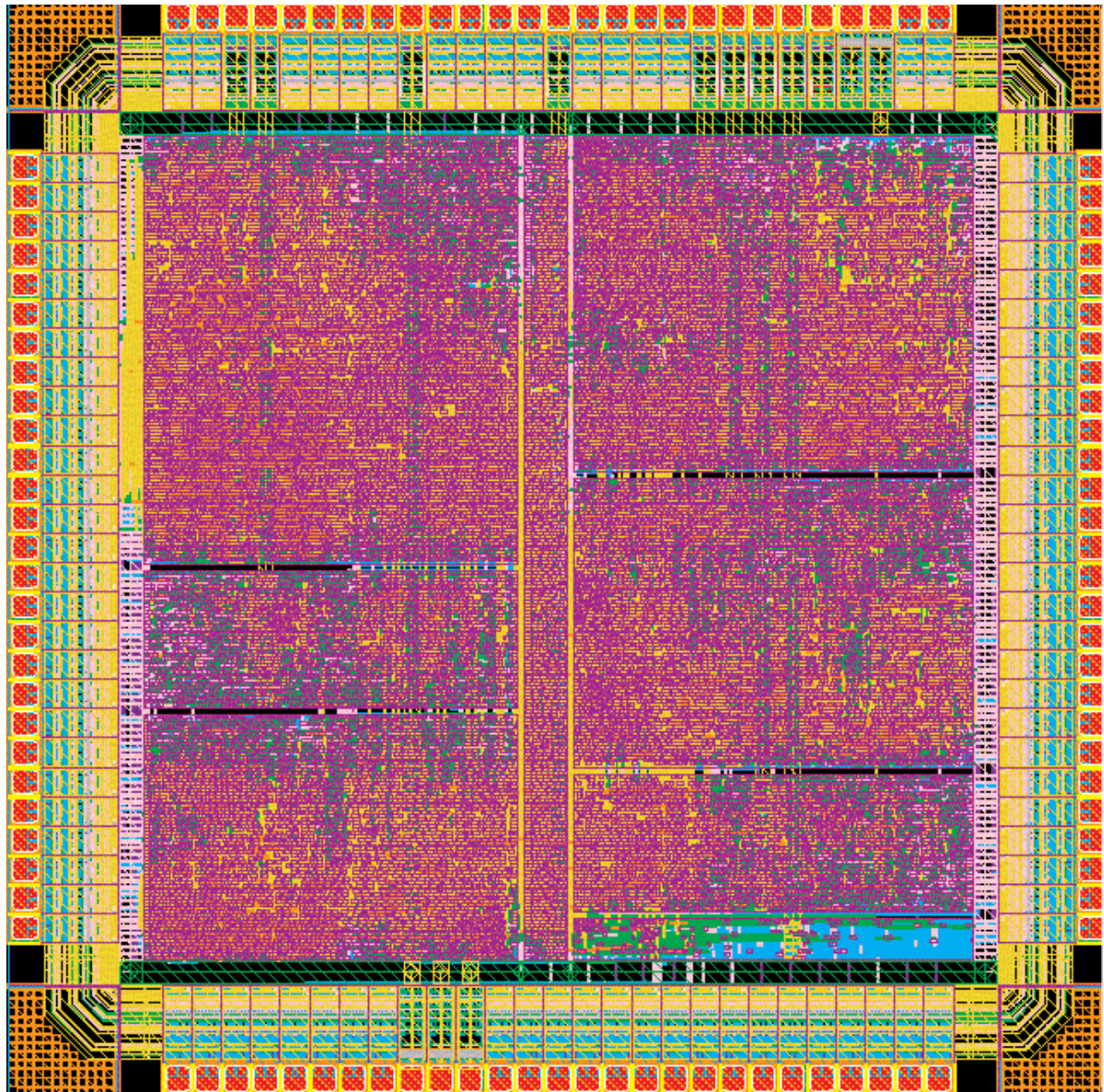
During the project, a prototype chip has been developed which for typical signal processing tasks has an energy consumption which is only 50% larger than for a dedicated circuit and which is more than an order of magnitude lower than for a general purpose signal processor. The picture on the opposite page shows the layout of the prototype chip produced.

The project has thus contributed noteworthy results within the areas known as 'system-on-chip', 'network-on-chip' and 'Application domain Specific Processors (ASP)'.

Publications

1. Ö. Paker, "Low Power Digital Signal Processing", PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, June 2002. IMM-PHD-2002-107.
2. Ö. Paker, J. Sparsø, M. Isager, N. Haandbæk, and L. S. Nielsen. "A heterogeneous low-power multiprocessor architecture for audio signal processing." *Journal of VLSI Signal Processing*, 2003. (Accepted for publication).
3. Ö. Paker, J. Sparsø, N. Haandbæk, M. Isager, L. S. Nielsen. "A heterogeneous multi-core platform for low power signal processing." In *ESSCIRC 2002, 28th IEEE European Solid-State Circuits Conference*, September 2002.
4. Ö. Paker, J. Sparsø, "A heterogenous multi-core platform for low power signal processing in systems-on-chip." In *Workshop on Heterogenous Reconfigurable Systems on Chip (SoC)*. RWTH Aachen, April 2002.
5. Ö. Paker, J. Sparsø, N. Haandbæk, M. Isager, L. S. Nielsen. "A heterogeneous multiprocessor architecture for low-power audio signal processing." In A. Smalagic and H. De Man, editors, *VLSI'2001, IEEE Computer Society Workshop on VLSI*, pages 47-53. IEEE Computer Society Press, April 2001.

The illustration shows the layout of the prototype chip produced. It contains a heterogeneous multiprocessor which is optimised for signal processing with low power consumption. The chip contains 6 small programmable and domain-specific signal processors (three on each side) and a communication network (in the middle). The chip is fabricated using a 0.25µm CMOS process, it measures 9 mm² and contains 400,000 transistors. It is synthesised from VHDL and implemented using standard cells. The chip has been manufactured and tested.



Techniques for medical 3D visualization, image-processing and simulation

Project data

Ph.D. student

Hans Holten-Lund

Period

July 1998 - June 2001

In collaboration with

*Århus Kommunehospital and
3D-Lab at Rigshospitalet*

Sponsors

*The Danish Research Training
Council (FUR), eksternal collabo-
rators, and the Thomas B. Thrige
Foundation*

Host institution

*Informatics and Mathematical
Modelling, DTU*

Supervisors

*Associate Professor Steen
Pedersen (principal supervisor),
and Professor Jan Madsen*

Project description

The main theme of this project is the design and implementation of efficient 3D visualisation systems. Various architectures for graphical systems are analysed and discussed in detail and a series of implementations for pure software and for mixed hardware/software systems are presented.

The theoretical aspects which have been considered in the course of the project have been illustrated via a series of speed- and resource-optimised implementations of parts of a graphical architecture, Hybris, developed by Hans Holten-Lund. This architecture has throughout the project formed the basis for testing and comparing various technologies, and it has furthermore been used in a series of Master's thesis projects. In addition, Hybris has been used as the basis on which a concrete 3D prototype system, 3D-Med, with the specific aim of processing 3D data from medical scanners, has been built up.

This prototype system has been developed in collaboration with 3D-Lab and doctors from Rigshospitalet and with Professor Niels Egund, dr.med., from the Århus Kommunehos-

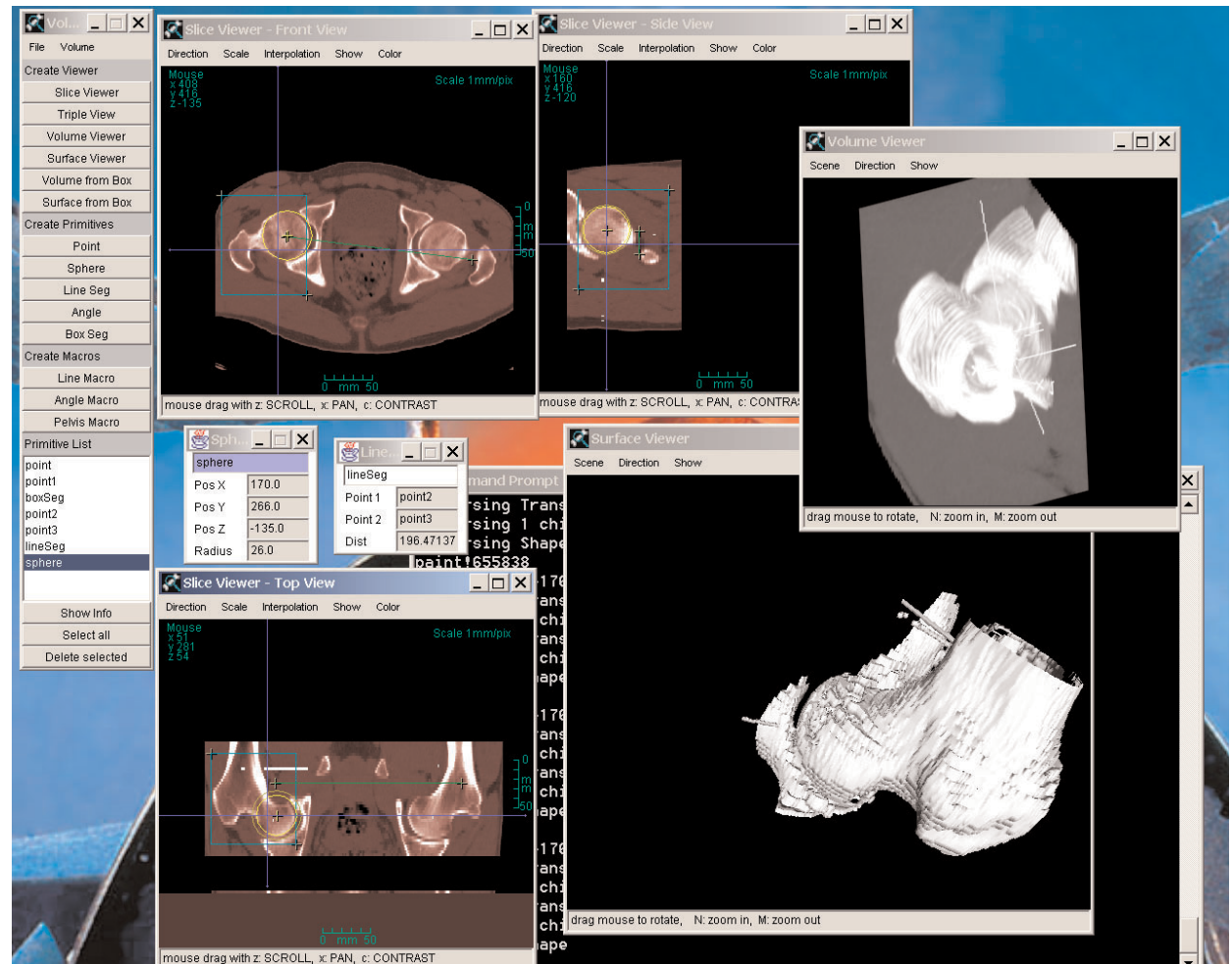
pital. The project has resulted in the successful production of a prototype of a 3D visualisation and measurement system of a type which is not available from other suppliers of 3D systems.

The 3D-Med project has been supported by Erhvervsfremmestyrelsen, initially through a preliminary investigation carried out partly by Carl Bro, Innotech/RHFU, and Informatics and Mathematical Modelling, DTU. Hans Holten-Lund took part in this investigation during a period of leave from his Ph.D. studies. A further 5.8 million Danish crowns have just been granted for further work on the project in the form of concrete 3D measurement and visualisation systems for orthopaedic surgery. The final target of this project is to build up a 3D "toolbox" which can be used for building and configuring concrete 3D systems for other specific medical applications.

Publications

- Holten-Lund, Hans: "Design for Scalability in 3D Computer Graphics Architectures", Ph.D. thesis, Informatics and Mathematical Modelling, Technical University of Denmark, July 2001. IMM-PHD-2002-100.
- Holten-Lund, Hans: "FPGA-Based 3D Graphics Processor with PCI-bus Interface, an Implementation Case Study", NORCHIP 2002 Proceedings, pp. 316-321, Copenhagen, Denmark, November 2002.
- Gleerup, Thomas Møller; Holten-Lund, Hans; Madsen, Jan; Pedersen, Steen: "Memory Architecture for Efficient Utilization of SDRAM: A Case Study of the Computation/Memory Access Trade-Off". CODES 2000, 8th International Workshop on Hardware/Software Codesign, pp. 51-55, San Diego, USA, May 2000.
- Holten-Lund, Hans; Hvidtfeldt, Mogens; Madsen, Jan; Pedersen, Steen:

Screenshot of the 3D-Med Medical
3D Visualization Workstation



- "VRML Visualization in a Surgery Planning and Diagnostics Application". Web3D-VRML 2000 Fifth Symposium on the Virtual Reality Modeling Language, pp. 111-118, Monterey, California, USA, February 2000.
5. Holten-Lund, Hans; Lütken, Martin; Madsen, Jan and Pedersen, Steen: "Virtual Prototyping, a Case Study in Dataflow Oriented Codesign". NORCHIP '98 Proceedings, pp. 222-229, Lund Sweden, November 1998.
6. Holten-Lund, Hans; Madsen, Jan and Pedersen, Steen: "A Case Study of a Hybrid Parallel 3D Surface Rendering Graphics Architecture", SASIMI '97 Workshop on Synthesis and System Integration of Mixed Technologies, pp. 149-154, December 1997.

Programming Languages for Embedded Software

Project data

Ph.D. student

Ken Friis Larsen

Period

April 1999 - December 2002

In collaboration with

GN ReSound A/S

Sponsors

The Danish Research Training Council (FUR), GN ReSound, the IT University of Copenhagen, and the Thomas B. Thrige Foundation

Host institution

Informatics and Mathematical Modelling, DTU and the IT University of Copenhagen

Supervisors

Professor Jørgen Staunstrup, DTU (1999), Associate Professor Jens Sparso, DTU (1999-2002), and Associate Professor Peter Sestoft, IT University of Copenhagen and Royal Veterinary and Agricultural University

Project description

Most software for PCs and servers is written in high-level languages such as Java, C++ or Visual Basic. Such languages have type systems which prevent the programmer from making certain mistakes, such as confusing integers with memory addresses.

Software for embedded systems and devices, on the other hand, is often written in a low-level language, for example assembler (symbolic machine language). This is especially the case in systems with limited resources, where the energy consumption or physical size must be modest. Assembler gives the programmer better possibilities than high-level languages do for predicting the number and sequence of the machine instructions which are performed in order to solve a given task in a program. However, such low-level languages lack the type systems which make high-level languages convenient and safe to program in.

The aim of this project is to show that embedded software can be written in typed assembler language. A typed assembler language is a symbolic machine language with type annotations whose correctness can be checked mechanically. This makes it possible to achieve security against a number of errors, without the programmer losing control over the details of how the program will be executed. The project focusses on embedded software for hearing aids, which are subject to predictable performance requirements and strict resource limitations. Typed assembler language has previously been proposed with the aim of ensuring that

an assembler program generated by an ordinary compiler does not perform illegal operations.

In this project, on the other hand, it is the intention that the programmer is to write typed assembly language himself. The type system which has been developed is adapted to the application area. Hearing aid software mainly performs digital signal processing, which is dominated by simple loops and array manipulations. Thus a type system has been developed which ensures the safety of pointer-based array lookup without loss of run-time efficiency. Even though assembler language lacks the data structures and type facilities which characterise high-level languages, it is in fact possible via type annotations to detect a large range of typical programming errors at compile time. This is for example the case for (1) indexing errors in array lookup, (2) incorrect or missing initialisation of variables, (3) breaches of the calling conventions in procedure calls, and (4) stack overflow, either on the procedure call stack or the do-loop stack.

Competent and disciplined assembler programmers will normally document the interfaces to procedures, typically by inserting program comments. In this project, it is demonstrated that type annotations can just as well be used to provide this documentation, with the considerable advantage that the consistency of the type annotations with the code can be checked mechanically, whereas the comments can not.

A rule from the type system for finding errors in assembler programs for doing signal processing. The rule is checked by a type-checker, not by the programmer.

$$\begin{array}{c}
 \Psi; R_1 \vdash v : \text{int}(e) \quad \phi_1 \models e > 0 \\
 R_1(\text{dsp}) = S \\
 k_1 \in \mathbf{dom}(\phi_2) \quad \phi_2 \models 0 \leq k_1 < e - 1 \\
 R_2(\text{dsp}) = \text{int}(k_1) :: S \\
 \phi_1 \vdash \theta_1 : \phi_2 \\
 \Delta; \phi_1; R_1\{\text{dsp} : \text{int}(0) :: S\} \models_c R_2[\theta_1] \\
 \Psi; \Delta; \phi_2; R_2 \vdash B \Rightarrow \phi_3; R_3 \\
 R_3 = R'_3\{\text{dsp} : \text{int}(k_1) :: S\} \\
 \phi'_3 = \phi_3 \wedge \{k_2 : \text{int} \mid k_1 < e - 2 \wedge k_2 = k_1 + 1\} \quad k_2 \notin \mathbf{dom}(\phi_3) \\
 \phi'_3 \vdash \theta_2 : \phi_2 \\
 \Delta; \phi'_3; R'_3\{\text{dsp} : \text{int}(k_2) :: S\} \models_c R_2[\theta_2] \\
 \Psi; \Delta; \phi_3 \wedge k_1 = e - 1; R_3 \vdash B \Rightarrow \phi_4; R_4\{\text{dsp} : \text{int}(k_1) :: S\} \\
 \text{(do-oob)} \quad \frac{}{\Psi; \Delta; \phi_1; R_1 \vdash \text{do}(v) \{B\} \Rightarrow \phi_4; R_4\{\text{dsp} : S\}}
 \end{array}$$

Publications

1. Simon Mørk, Ken Larsen, Henrik Reif Andersen, Peter Sestoft, "PMC: A programming language for embedded systems." Fourth International Workshop on Formal Methods for Industrial Critical Systems, Trento, Italy, July 1999.
2. Mike Gordon and Ken Friis Larsen, "Combining the Hol98 Proof Assistant with the BuDDy BDD package", University of Cambridge Computer Laboratory Technical Report No. 481. December 17, 1999.
3. K. F. Larsen, "A Tutorial on Integrating C Libraries into Moscow ML", The IT University of Copenhagen, March 2001. (To appear in forthcoming PROSPER book).

Integrated Circuits in Medical Ultrasound

Project data

Ph.D. student

Borislav Tomov

Period

November 1999 - October 2002

In collaboration with

B-K Medical A/S

Sponsors

The Danish Research Training Council (FUR), B-K Medical A/S, and the Thomas B. Thrige Foundation

Host institution

Center for Fast Ultrasound Imaging at Ørsted•DTU

Supervisor

Professor Jørgen Arendt Jensen (principal supervisor), and Associate Professor Jens Sparso

Project description

In this project, architectures and implementations for compact ultrasound scanners are being developed. Traditional ultrasound scanners are difficult to transport round the hospital or clinic, which makes it hard to use them in an emergency department, a maternity ward or out in the field. In recent years, a number of compact scanners have been introduced, where special chips have been developed in order to achieve a compact implementation. The aim of this project is to develop a simpler and more compact chip, where the entire signal processing activity can be performed in a single integrated circuit.

Modern digital ultrasound scanners sample data in 64 channels at a frequency of 20 to 40 MHz. Thus about 5 Gbytes of data are generated per second, and these data have to be processed in real time. A signal processing task of this magnitude at such high frequencies is difficult to perform and implement on a single chip. The idea in the project is therefore to change the structure of the signal processing so that all the processing can be dealt with in a single, simple circuit. The structure developed is based on 1 bit signals collected by using sigma-delta analog to digital conversion at 140 MHz. The time delay for focussing the ultrasound is calculated parametrically, after which the correct bit stream of

data is selected from the input signal. This is done for all the measured channels and data from these are summed together.

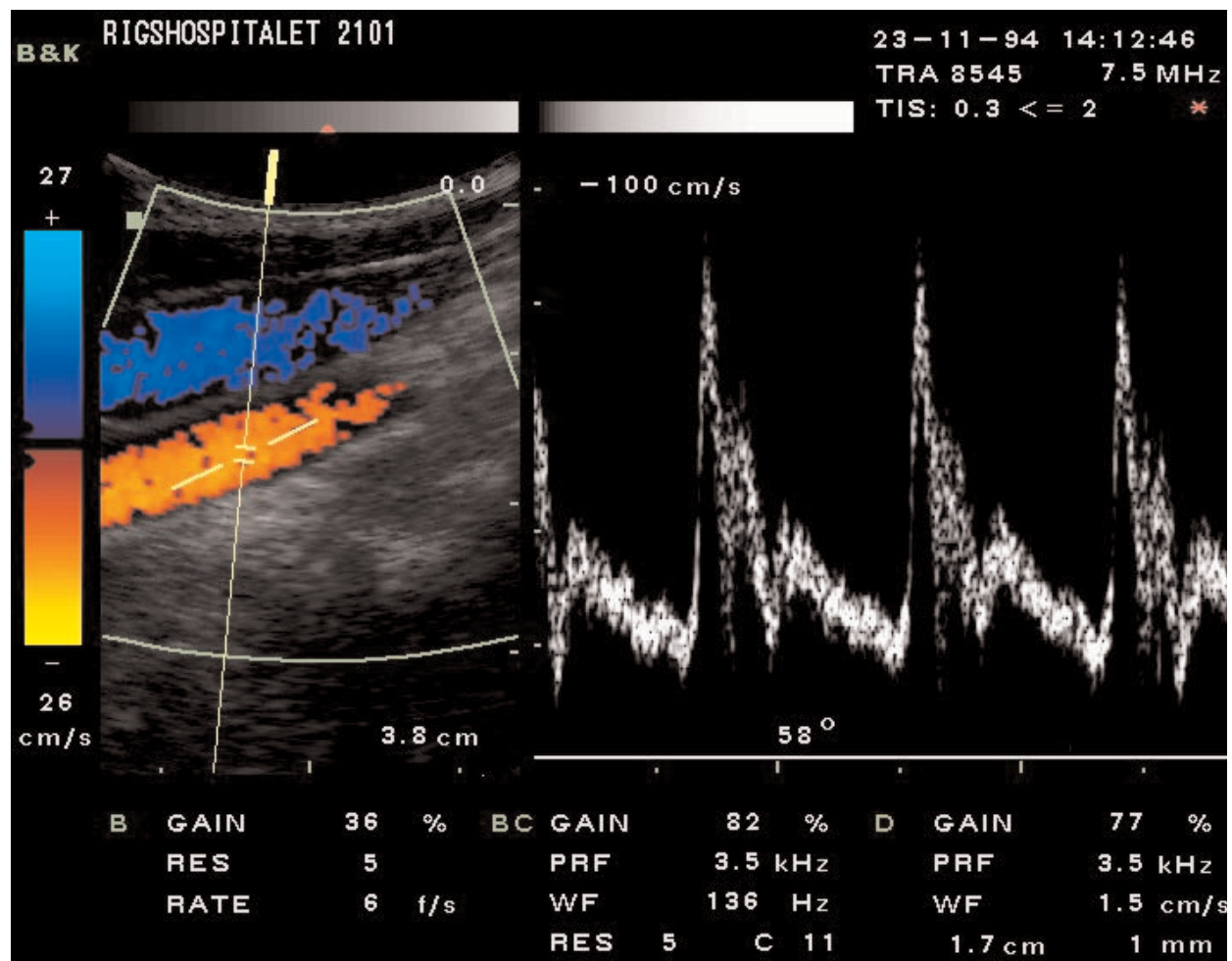
After this, an adapted filtering with a complex filter is used to give the complex signal for a point in the image. With this method, data only needs to be evaluated for points in the image, and this gives a very marked reduction in the amount of data. A prototype of the design has been developed in VHDL and the signal processing is so compact that it can be tried out in a standard FPGA chip. A complete beam former for a 64 channel ultrasound scanner can in this way be held in a Xilinx XCV2000E chip with 2.3 million gates, whereas a normal implementation would require a large number of specially developed chips.

Thus the project has made it possible to develop very compact ultrasound scanners. Its results can also be used directly in the development of normal scanners. Last but not least, the results form the basis for a new type of ultrasound scanner based on synthetic aperture techniques, which pave the way to completely new methods for generating images. The project is now continuing as a post doc. project in collaboration with B-K Medical.

Publications

1. B. G. Tomov and J.A. Jensen: A new architecture for a single-chip multi-channel beamformer based on a standard FPGA, In Proc. IEEE Ultrason. Symp., page 1529-1532, 2001.
2. B. G. Tomov and J.A. Jensen: Compact FPGA-based beamformer using oversampled 1-bit AD converters, Submitted to IEEE Biomedical Engineering.
3. B. G. Tomov and J.A. Jensen: Delay generation methods with reduced memory requirements, Proceedings of SPIE, To be published, 2003.

Ultrasound image of blood flow in the carotid artery (left-hand colour picture), together with speed in the blood vessel as a function of time for two heart beats (right-hand picture).



Technology Development for Topology Optimised Thermal Microactuators

Project data

Ph.D. student

Jacques Jonsmann

Period

July 1996 - December 1999

Sponsors

The Thomas B. Thrige Foundation

Host institution

*Mikroelektronikcentret (MIC),
DTU*

Supervisors

*Associate Professor Siebe
Bouwstra (principal supervisor),
and Professor Ole Sigmund*

Project description

Microactuators exploit the same physical mechanisms as "traditional" actuators, but certain special properties of microactuators are associated with their small size. In addition, physical phenomena scale differently with size, and fabrication techniques favorise production of planar structures – the starting point is normally a metallic layer deposited on a silicon wafer.

The initial idea for this project was to exploit topology optimisation, and in particular the topology optimisation system TopOpt™, developed by Professor Ole Sigmund, in connection with the fabrication of microactuators. Topology optimisation can be used when the desired behaviour is well-defined, and the optimum topology for achieving this behaviour is sought. Topology optimisation takes place iteratively by finite element analysis and material relocation.

The Ph.D. project has included fabrication, characterisation and theoretical aspects. After an initial investigation, a decision was made to use thermal actuation – i.e. to exploit the expansion of materials when they are heated. Passive actuators are based on external heating of the entire actuator together with the silicon wafer. Active thermal actuators are based on local heating, typically caused by an electric cur-

rent. A fabrication process was then developed for rapid prototyping of metallic actuators. The metal structures are electroplated in silicon moulds produced by laser micromachining and reactive ion etching. This process is very flexible and can be used for all available topology optimised actuators. Using this process, it only takes 2-3 days to produce a new actuator. In order to characterise these actuators, extremely precise methods for measurement of static and dynamic movement have been developed. A system based on image analysis of microscope images has given exceptionally fine measurements of static movement.

In the course of the project, 15-20 different actuators have been designed and manufactured. Two of the most advanced of these are a micropositioning unit with two degrees of freedom and a micromanipulator with three degrees of freedom. For controlling these, a computer system was developed which permits direct control via a joystick. The actuators, which were manufactured typically deliver forces of the order of 10 mN and movements of the order of 20 µm, which makes them some of the strongest microactuators to date. This is partly due to the optimised design and partly a result of using the strong thermal actuation.

Publications

1. J. Jonsmann. Technology Development for Topology Optimised Thermal Microactuators, Ph.D. Thesis, Mikroelektronik Centret, September 1999, ISBN 87-89935-03-9.
2. J. Jonsmann, S. Bouwstra. Material considerations for topology optimised thermal microactuators, Proc. Eurosensors 2000, p. 171-172, 2000.
3. J. Jonsmann, O. Sigmund, S. Bouwstra. Compliant thermal microactuators, Sensors & Actuators, vol. 76, p. 463-469, 1999.
4. J. Jonsmann, O. Sigmund, S. Bouwstra. Multi degrees of freedom electrothermal microactuators, Proc. Transducers '99, p. 1372-1375, 1999.

The figure shows a SEM image of a topology-optimised 2D electro-thermal micro-positioner fabricated in nickel on silicon. An applied potential across the bottom and top left electrodes will move the positioner (far right end) in the horizontal direction, whereas a potential applied across the bottom and top right electrodes will move the positioner in the vertical direction.



5. J. Jonsmann, S. Bouwstra, Thermal microactuator characterisation, Proc. SPIE Proc. Design, Test, and Microfabrication of MEMS/MOEMS, p. 1046-1055, 1999.

6. J. Jonsmann, O. Sigmund, S. Bouwstra, Compliant electro-thermal microactuators. Proc. MEMS '99, p. 588-593, 1999.

7. J. Jonsmann, O. Sigmund, S. Bouwstra, Compliant thermal microactuators, Proc. Eurosensors '98, p. 395-398, 1998.

CAD tools for Microsystems

Project data

Ph.D. student

Morten Ginnerup

Period

July 1998 - February 2003

Sponsors

The Thomas B. Thrige Foundation

Host institution

*Mikroelektronikcentret (MIC),
DTU*

Supervisor

Associate Professor Siebe Bouwstra (1998 - January 2000), and then Associate Professor Ole Hansen (principal supervisor), and Professor Ole Sigmund

Project description

Effective exploitation of the possibilities offered by MEMS technologies requires extensive use of CAD/CAE tools to assist the designers in the very complicated multi-disciplinary process that a MEMS design involves. Unfortunately, the necessary tools are not available, partly because this field is not yet mature, and partly because of the very high complexity which a set of tools must deal with. Ideally, the collection of tools must deal with everything from a behavioural description at a high abstraction level – as known from HDLs for digital design – to detailed modelling of non-linear, anisotropic, physical phenomena in coupled physical domains – such as piezoelectricity in crystalline materials, where the simultaneous solution of a dynamic elastic and a dynamic electromagnetic problem is necessary.

In this project existing tools (ANSYS, Coventor, FloTran, SUPREM, SPICE, SUGAR, FastCap etc.), which solve parts of the problem have been implemented at MIC and their limitations identified. Important auxiliary tools, which render the use of the tools for MEMS applications more efficient,

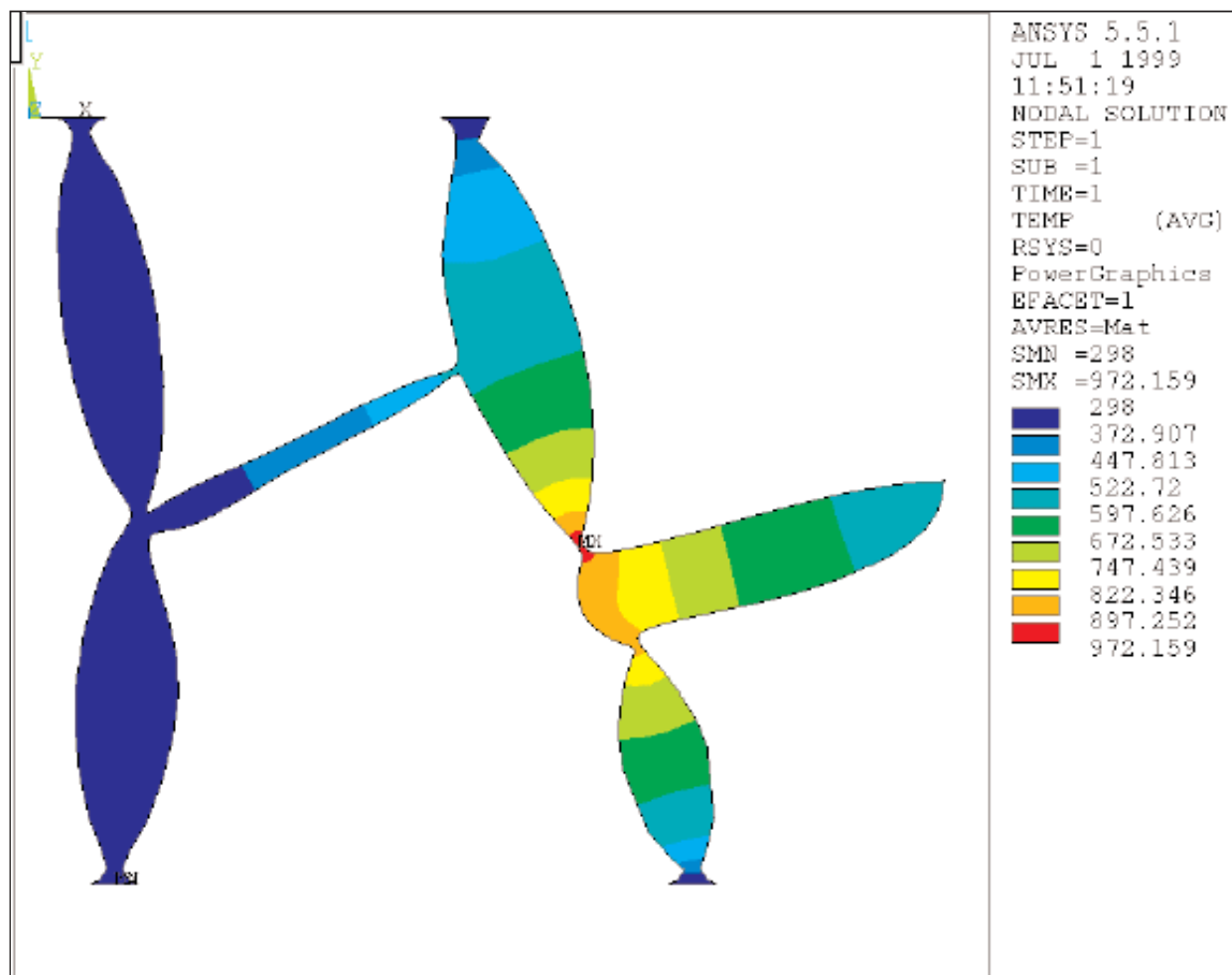
have then been developed. A tool which exploits SPICE and ANSYS has been developed for dynamic analysis of MEMS systems; in SPICE, the electronic part of the system can be directly simulated, while the electromechanical part of the system is modelled with the help of a combination of analytical models and automatic calls of ANSYS, with subsequent extraction of SPICE models which can then be inserted into a full SPICE model of the system.

Another tool has been developed for automatic investigation of parameter variation induced by the fabrication process into topology- optimised structures generated using TopOpt™. This tool uses mask information, fabrication process information and process parameter variation to calculate the variation in key parameters of the final structure via automatic calls of ANSYS and SPICE. In the long term, it would be possible to incorporate such calculations into TopOpt™ so that structures can be synthesised directly, in order to achieve minimal sensitivity to variations in the fabrication process.

Publications

1. Kristian P. Larsen, Anette A. Rasmussen, Jan T. Ravnkilde, Morten Ginnerup and Ole Hansen. "MEMS device for measurements of fatigue and creep of electroplated nickel", *Sensors and Actuators A* 103, pp 156-164, 2003.
2. Kristian P. Larsen, Jan. T. Ravnkilde, Morten Ginnerup, Ole Hansen. Devices for Fatigue Testing of Electroplated Nickel Proceedings of MEMS 2002, pp. 443-446, Las Vegas, January 2002.
3. L. S. Johansen, M. Ginnerup, J.T. Ravnkilde, P. T. Tang and B. Lochel. "Electroforming of 3D microstructures on highly structured surfaces", *Sensors and Actuators A: Physical*. 83 (1-3), pp. 156-160, 2000.
4. L. S. Johansen, M.Ginnerup, P.T. Tang, J.T. Ravnkilde and B. Löchel. "Fabrication of electroplated 3D microstructures combining KOH etching, electrodeposition of photoresist, and selective etching", in *Transducers '99, 10th International Conference on Solid-State Sensors and Actuators*, The Institute of Electrical Engineers of Japan, Sendai, Japan, 1999.

The figure shows the calculated temperature profile of an electro-thermal topology-optimised actuator during actuation. The temperature profile is calculated using the finite element analysis tool ANSYS, for a situation where current is passed between the two right-most terminals of the structure.



High-aspect-ratio microstructures

Project data

Ph.D. student

Ras Kaas Vestergaard.

Period

November 1997 - September 2001

Sponsors

The Thomas B. Thrige Foundation

Host institution

Mikroelektronikcentret (MIC), DTU

Supervisor

Associate Professor Siebe Bouwstra (1997- January 2000), Associate Professor Ole Hansen (January 2000 – 2001)

Project description

Many micromechanical designs, if they are to perform in an optimal manner, make heavy demands on the aspect ratio which can be achieved in the fabrication process. Very large aspect ratios, i.e. a large thickness (height) and a small width, can be implemented by using the LIGA process. Here, a very thick X-ray resist is illuminated through an X-ray mask by an intense, collimated X-ray beam. The resist pattern is subsequently used as a mould for electrolytic deposition of metal. However, due to the costs of X-ray lithography, this process is so expensive that there are only extremely few applications for which the procedure is economically viable. In this project, an alternative process based on more traditional lithography has been developed. As UV lithography is orders of magnitude cheaper than X-ray lithography, the opportunities for industrial use of this process are much greater than for LIGA.

In the project, a LIGA-like technology based on epoxy-UV-resist SU-8 has been developed. The SU-8 resist is bleached

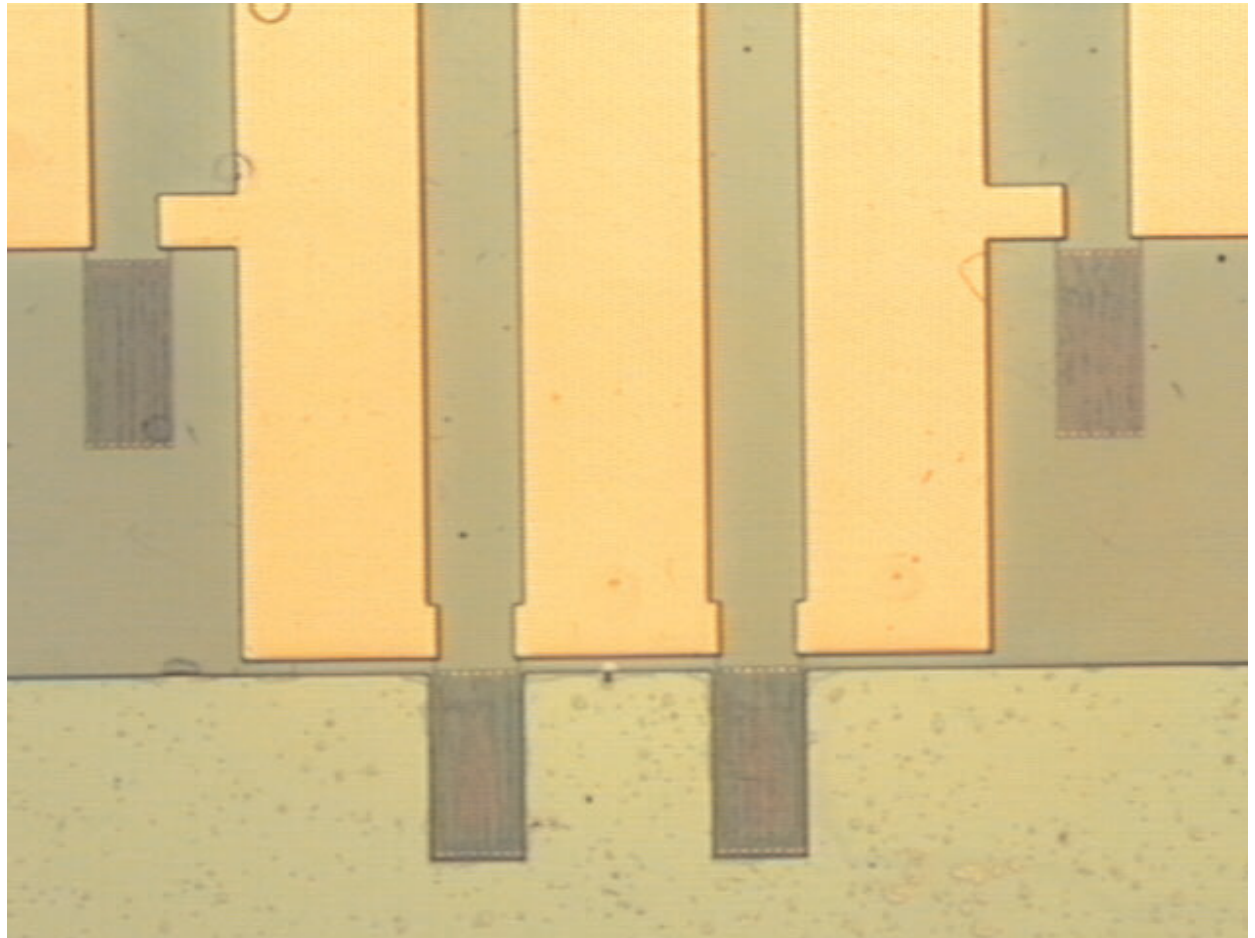
and increases its refractive index when illuminated, and for this reason a much higher aspect ratio can be achieved than would be expected from an analysis of Fresnel diffraction at a mask edge. The process technology which has been developed makes it possible to fabricate structures with aspect ratios of 20-30 with structure heights up to 100 μm . Further work will make it possible to increase the structure height to 2 mm.

The possibilities offered by this technology have been demonstrated via fabrication of structurally optimised electrothermal actuators and multi-layer coils. In addition, the SU-8 resist, which is chemically an extremely stable material, has turned out to be a useful construction material. This has been exploited in several sensor designs; including a biosensor based on an SU-8 beam with a built-in gold strain gauge. The low Young's modulus of SU-8 helps here to increase the sensitivity of the sensor. As SU-8 is also biocompatible, such sensors show great potential.

Publications

1. Jacob Thaysen, Arda D. Yalcinkaya, Ras K. Vestergaard, Søren Jensen, Peter Vettiger and Aric K. Menon. "SU-8 Based Piezoresistive Mechanical Sensor", 15th IEEE International Micro Electro Mechanical Systems Conference (MEMS'02), Las Vegas, USA, 2002.
2. Vestergaard, R.K. and Bouwstra, S. "Electroplated compliant metal microactuators with small feature sizes using a removable SU-8 mould" *Microsystem Technologies*, 6, 6. 214-217, 2000.
3. Vestergaard, R.K. and Bouwstra, S. "Electroplated compliant metal microactuators with small feature sizes using a removable SU-8 mould" *HARMST 99, Book of Abstract*, 96-97, 1999.
4. Vestergaard, R.K. and Bouwstra, S. "Removable SU-8 mould with small feature size for electroplating compliant metal micro actuators" *Proceedings Transducers 99*, vol 1, 480-483, 1999.

The figure shows a SU-8 cantilever sensor with integrated gold piezoresistors. The device consists of an SU-8 support structure holding two thin cantilevers with embedded gold resistors and two reference gold resistors forming a full Wheatstone bridge. The sensor is intended for biochemical measurements in a wet ambient. One cantilever, the measurement cantilever, is sensitized with a specific surface coating whereas the other serves as a reference; thus background interference from thermal and liquid fluctuations is filtered out and the true biochemical response remains.



Microelectromechanical resonators for low-power, low-voltage systems

Project data

Ph.D. student

Arda Deniz Yalcinkaya

Period

April 2000 - March 2003

In collaboration with

Sonion MEMS A/S, Otvidan

Sponsors

The Danish Research Training Council (FUR), Sonion MEMS A/S, and the Thomas B. Thrige Foundation

Host institution

Mikroelektronikcentret (MIC), DTU

Supervisor

Associate Professor Ole Hansen

Project description

Many electronic systems require integration of the electronics with frequency-selective components. The Q-factor requirements for the frequency-selective components are often so high that purely electronic solutions are impossible, and discrete electromechanical components therefore have to be used. These discrete electromechanical components – crystal oscillators and filters – occupy a very large volume compared with the remainder of the electronic system.

In this project, attempts have been made to implement the electromechanical components by fabricating MEMS structures directly onto a CMOS chip which implements the electronic part of the system. As MEMS structures can be fabricated in very small sizes – typically with edge lengths of some few hundred micrometers and structure heights of a few micrometers – a compact overall solution is attained. In

principal, this monolithic integration of MEMS components with CMOS can take place in two ways, either as an integrated part of the fabrication of the IC, which seriously limits the number of possible suppliers, or by building the electromechanical structures on finished CMOS wafers.

In this project, the technique of fabricating metallic microstructures on finished CMOS wafers has been used, as this offers the advantage that any CMOS process supplier can be chosen, while at the same time the subsequent fabrication of the metallic microstructures is relatively cheap. In the course of the project, oscillators, filters and variable capacitors have been designed, analysed and fabricated. In addition, the limitations of the components with respect to process variation sensitivity and temperature sensitivity have been analysed theoretically and experimentally.

Publications

1. Arda D. Yalcinkaya, Jan T. Ravnkilde and Ole Hansen. "Fabrication of integrated metallic MEMS devices", IEE Electronics Letters 38, no. 24, pp1526-1527, 2002.
2. Jacob Thaysen, Arda D. Yalcinkaya, Peter Vettiger, and Aric Menon. "Polymer based stress sensor with integrated read-out " Journal of Applied Physics D, 35, Issue 21, pp. 2698-2703, 2002.
3. Jacob Thaysen, Arda D. Yalcinkaya, Ras K. Vestergaard, Søren Jensen, Peter Vettiger and Aric K. Menon. "SU-8 Based Piezoresistive Mechanical Sensor", 15th IEEE International Micro Electro Mechanical Systems Conference (MEMS'02), Las Vegas, USA, 2002.
4. Arda D. Yalcinkaya, Jan T. Ravnkilde, Leif S. Johansen and Ole Hansen. "Methods for Fabrication of Released Nickel Comb-Drive Devices on CMOS", Proceedings of TRANSDUCERS '01/ EUROSENSORS XV, pp. 600-603, Munich, June 2001.
5. Ravnkilde Jan T., Yalcinkaya Arda D., Johansen Leif S. and Hansen Ole. "Fabrication of Electroplated Nickel Micromechanical Resonators", 196th Meeting of the Electrochemical Society, Vol. 99-2, Abstract no. 943, Honolulu, Hawaii, October 1999.
6. Johansen Leif S., Ravnkilde Jan T., Yalcinkaya Arda D. and Hansen Ole. "Electroplated Ni Comb Accelerometers for CMOS Post Processing", EUROSENSORS XIII, pp.799-802, The Hague, The Netherlands, September 1999.

The figure shows a SEM image of an electroplated comb-resonator fabricated on top of a CMOS wafer. The resonator comprises three parts, a movable shuttle in the center suspended by folded beam springs and two static parts at the top and the bottom coupled to the moveable part by comb capacitors. Below the moveable part, the CMOS devices are clearly visible. The moveable part is actuated electrically by an AC-signal on the lower comb-capacitor and the motion sensed at the upper comb-capacitor, thus forming a high quality factor band-pass filter.

